

MxL93515 and MxL93516

Product Brief 100G PAM4 DSP SoC

General Description

The MxL93515 and MxL93516 are highly integrated PAM4 DSP devices that enable a 100Gbps optical interconnect using 100Gbps over a single optical wavelength $100G/\lambda$.

Both are optimized for four-level pulse amplitude modulation (PAM4) and non-return-to-zero (NRZ) applications and are available in a 7mm x 8.5mm package.

The MxL93515 has a differential pair of optical outputs.

The MxL93516 has a single-ended laser driver that is required for the EA-EML optics.

The devices have a high-speed electrical interface with four transmit (Tx) and receive (Rx) input/output (I/O) paths for NRZ applications and two Tx and Rx I/O paths for PAM4 applications that connect electrically through a module connector to the host ASIC. They also have a high-speed optical side interface that has one Tx and Rx that connect through the optical components to the optical fibers.

The electrical interface supports 25Gbps NRZ or 50Gbps PAM4 signaling over an electrical channel with up to 14dB channel loss, including the host connector.

The optics interface supports 100Gbps PAM4 signaling to enable 500m DR, 2km FR, and 10km LR use cases.

The devices support DSP functions including Tx digital predistortion (DPD), transmit pre-emphasis (Tx FIR), receive feed-forward equalization (Rx FFE), and decision feedback equalization (DFE) that is required for 56 Gbaud optics.

They have exceptional signal integrity for 56Gbaud signals in a compact footprint, suitable for next generation optical module form factors.

Applications

- QSFP28 optical modules
- SFP-DD optical modules
- DSFP optical modules

Features

- 100G capacity enables 100G DR, FR, and LR requirements.
- The MxL93516 has a single EA_EML driver with a 1.8V PP SE swing and required connect to the TOSA.
- The MxL93515 has a differential pair output with 0.7V differential PP swing feeding to the TOSA.
- Tx equalization includes pre-emphasis, digital predistortion, and reflection cancellation.
- Rx equalization includes continuous time linear (CTLE), multi-tap FFE and DFE, and reflection cancellation.
- Integrated crystal oscillator eliminates the need for a costly reference clock source.
- Digital I/O compatibility with the host processor. This removes the need for level shifters and saves valuable module board space.
- Small package size to enable the QSFP28, SFP-DD and DSFP space requirements.
- Bit error rate (BER) monitoring.
- Signal-to-noise ratio (SNR) reporting for each receiver on both electrical and optical interfaces.
- Diagnostic loop-backs and test pattern generation and checking.
- SPI and I²C slave interface to communicate to module micro-controller unit (MCU).
- SPI master for flash memory interface.
- I²C master interface for TIA direct control.
- Embedded CPU for real-time control.
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected.
- Error correcting code (ECC) in the CPU memories provide 2-bit error detection and a single-bit error correction

Supported Standards

- IEEE Std 802.3-2015, Sections 4, 5, and 6
- OIF-CEI-56G-VSR
- IEEE Std P802.3cd
- IEEE Std P802.3bs

Block Diagram

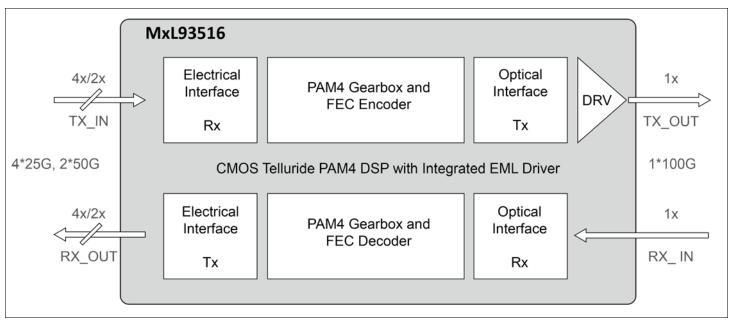


Figure 1: MxL93516 Functional Block Diagram

Note: The MxL93515 block diagram is the same without the driver block.

Ordering Information

Marketing Part Number	Ordering Part Number	Package	Shipping
MxL93515	MxL93515-AY-T	FCFBGA 7mm × 8.5mm ×1.67mm	Tray
MxL93516	MxL93516-AY-T		



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