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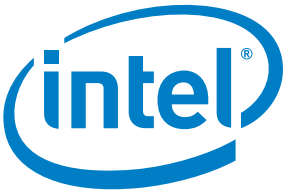

Intel® Ethernet Switch

GSW150, PEB7084MV11
GSW150, PEB7084MV12

Data Sheet

Revision 1.3, 2017-03-20
Intel Confidential
Reference ID 617908

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Revision History

Current:	**Revision 1.3, 2017-03-20**
Previous:	**Revision 1.2, 2016-11-17**

Page	Major changes since previous revision
All	The following devices/families have been renamed: • F25G Family to Intel® Ethernet Switch • PEB 7084 to GSW150
247	**Physical Layer Control 2** register description updated for **LSADS** bit field.

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1 Product Overview

Intel® Ethernet Switch is a highly integrated, non-blocking seven-port Gigabit Ethernet switch with five tri-speed Ethernet PHY and two tri-speed RGMII or one tri-speed GMII interfaces. GSW150 uses a very small package MRQFN 9 mm x 9 mm to minimize PCB size.

Each Gigabit-Ethernet (GbE) PHY supports 10BASE-Te, 100BASE-TX and 1000BASE-T standards. Support of Energy-Efficient Ethernet allows for reduction in idle mode power consumption. Power savings at system level are introduced using the Wake-on-LAN feature. Low-EMI line driver with integrated termination facilitates a simplified PCB design.

The 6th port and the 7th port of Intel® Ethernet Switch support a tri-speed (10/100/1000 Mbps) RGMII interface each for connecting with external PHY or MAC. The 6th port also supports GMII interface mode and the 7th port can be used for packet insertion and extraction via management interface in this configuration.

GSW150 is configurable via pin-strapping, MDIO interface, UART interface, SPI interface or optionally by connecting an external EEPROM.

Intel® Ethernet Switch supports up to three LEDs per GbE PHY. Smart LED brightness control logic is integrated for power saving. LED brightness can be adjusted either by a push-button or varies dynamically depending on the intensity of the light with an external light sensor.

The 128 KB embedded packet storage SRAM is integrated and 9 KB jumbo frames are supported. Intel® Ethernet Switch integrates a 4K entry VLAN table for 802.1Q port-based, tag-based and protocol based VLAN operation. It also supports double VLAN tagging, insertion, removal and translation. Intel® Ethernet Switch features 2048 MAC addresses with 4-way hashing algorithm for address searching, auto-learning and auto-aging.

Programmable parsing and powerful classification engine allow future-proof designs that enable various data traffic types. Intel® Ethernet Switch supports IPv4 and IPv6 multicast forwarding, including IGMPv1/v2/v3 and MLD v1/v2 snooping.

Intel® Ethernet Switch features an advanced QoS architecture which prioritizes switch traffic for different classes of applications based on multiple fields of the packet. Multiple queues per port with strict or weighted round robin scheduling and rate shaping are supported. VLAN PCP and IP DSCP can be remarked. Intel® Ethernet Switch also supports Precise Time Stamping indication according to IEEE 1588v2 and IEEE 802.1AS.

Several degrees of application complexity are covered, from a basic stand-alone switch, set-top boxes to complex home gateways. The Intel® Ethernet Switch is intended for Video/Audio applications in the Digital Home such as IP-TV, ADSL2+/VDSL2/PON IAD, Gateway, Wireless Router, Cable, Storage and HomePlug AV applications.

1.1 Features

This chapter provides an overview of the basic Intel® Ethernet Switch functionality.

Interfaces

- Five multiple speed Ethernet PHY interfaces, compliant with:
  - 10BASE-Te
  - 100BASE-TX
  - 1000BASE-T
  - Auto-MDIX
  - Auto-Downspeed
  - Auto-Negotiation with Next Page Support
  - Cable Diagnostics: Cable Open/Short Detection and Cable length estimation
  - Test Loops and Analog Self Test
  - Power Down Modes
  - 802.3az Energy-Efficient Ethernet
  - Support of Transformer-Less Ethernet for Backplane Applications
- One set of GMII interface or two sets of RGMII interfaces:
  - 10 Mbit/s, full and half duplex
  - 100 Mbit/s, full and half duplex
  - 1000 Mbit/s, full duplex
- MDIO master interface to control external devices:
  - Support auto polling of registers of external PHY devices
  - Support indirect access by command to registers of external PHY devices
  - Support programmable MDC clock up to 25 MHz
- SPI master interface connecting to a serial external E2PROM:
  - Support programmable SPI clock up to 50 MHz
  - Supports automatic switch configuration from an external E2PROM memory
  - Support write access to E2PROM by an external controller
  - Supports different E2PROM sizes from 1 kbits to 1024 kbits
- SPI Slave, MDIO slave or UART interface to allow control from an external microcontroller:
  - Maximum MDIO interface clock: 25 MHz
  - Maximum SPI interface clock: 50 MHz
  - Minimum SPI interface clock: 2.5 MHz
  - UART Baudrate from 4800 to 921600
- JTAG boundary scan, test and debug interface
  - Share pins with LED
- PHY status indicating LEDs:
  - Directly attached
  - Up to three LEDs per internal PHY port
  - Configurable LED functions per LED (link/activity, duplex/collision, link speed etc)
  - Steady/blinking indication
  - LED brightness controlled by an external push button
  - Up to 16 level LED brightness controlled by an external light sensor
- Two external interrupts
- Twenty six general purpose IO: share pins with MDIO master interface, external interrupts, general purpose clock, SPI master interface, SPI slave interface, UART interface, MDIO slave, LED, JTAG functions

Clocking

- Reference clock:
  - 25 MHz or 40 MHz

  - Crystal or direct input
- Two external clock outputs

Ethernet MACs

- Seven Ethernet MACs, complying with IEEE 802.3:
  - Three rates, that is, 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s operation speed
  - Half-duplex operation mode for 10 Mbit/s and 100 Mbit/s
  - Full-duplex operation mode for all speed
- Auto-negotiation for speed, duplex, flow control support, LPI support and link status
- Enhanced frame size support (“Jumbo frames”, programmable limit up to 9 Kbyte)
- Flow control:
  - Pause frame transmission/reception in full duplex mode
  - Forced collisions in half-duplex mode

Layer-2 Switching

- Store-and-forward architecture
- 1 Mbit on-chip segmented frame buffer
- 256 byte buffer segment size
- Up to 2048 MAC addresses:
  - Multiple-bucket HASH algorithm storage
  - Automatic learning and aging (1 s to 24 h)
  - Manual learning (static entries)
  - MAC learning limitation (configurable per port)
  - MAC port locking and spoofing detection (configurable per port)
  - MAC table freezing
- VLAN-unaware switching
- VLAN-aware switching:
  - Shared VLAN learning
  - Independent VLAN learning
  - Up to 4096 VLAN IDs
  - Port based VLAN
  - MAC based VLAN with automatic learning
  - Protocol-based VLAN based on flow classification result
  - Double VLAN or VLAN QinQ, addition/removal/translation of Service Tag VLAN ID and Customer Tag VLAN ID
  - Double VLAN or VLAN QinQ, port filtering based on both Service Tag VLAN ID and Customer Tag VLAN ID
- Multicast
  - Up to 64 multicast groups
  - Hardware IGMP mode: hardware based Join/Leave for IGMPv1/IGMPv2 mode, report suppression support
  - Software IGMP mode: IGMPv1/v2/v3 and MLDv1/v2 Snooping
  - Unknown IP multicast data stream forwarding or discard
  - Any Source Multicast and Source Specific Multicast forwarding

Layer-2/3/4 Flow Classification

- Multi-field parsing and classification, for example based on:
  - MAC source address
  - MAC destination address
  - Service Tag VLAN ID and Customer Tag VLAN ID
  - Ethertype
  - IPv4 header (DSCP, IP SA, IP DA)

  - IPv6 header (DSCP, IP SA, IP DA)
  - TCP source port/port range
  - TCP destination port/port range
  - UDP source port/port range
  - UDP destination port/port range
  - IGMP
  - MLD
  - ARP/RARP
  - ICMP
  - PPPoE, up to 16 session IDs
  - 64 ACL rules

Quality of Service

- Up to 32 CoS (Class of Service) queues
- Configurable egress queue scheduling
  - Strict priority
  - Weighted fair queueing, with configurable weights
  - Combination of strict priority and weighted fair queuing
- Flexible assignment of queues to egress ports
  - Multiple queues can be assigned to a single port (as far as available from the global pool of queues)
  - Maximum 16 queues per port
- Scalable egress rate shaping
  - 32 rate shapers
  - Up to 2 rate shapers can be assigned to a single queue (as far as available from global pool of rate shapers)
- Ingress traffic policing
  - 16 traffic policers
  - Standard single-rate Three Color Marker algorithm (srTCM)
  - Color-aware/-unaware operation
  - Policer can be assigned based on ingress port, egress port and flow classification result
  - Remarking, Drop or Flow Control for non-conforming traffic
- Flexible QoS handling based on any flow classification result, for example (but not limited to)
  - Service TAG VLAN PCP (Priority Code Point)
  - Customer TAG VLAN PCP (Priority Code Point)
  - IP DSCP
  - Ingress port
  - Source/destination IP address
  - TCP/UDP port/port range
- Service Tag VLAN PCP and DEI remarking
- Customer Tag VLAN PCP remarking
- DSCP remarking
- Congestion management
  - WRED algorithm (Weighted Random Early Discard)
  - Buffer reservation
  - Ingress port congestion based flow control
  - Ingress port metering based flow control
  - Three drop precedences
  - Configurable thresholds
- AVB support
  - Supports Precise Time Stamping indication according to IEEE P802.3bf for support of IEEE 1588v2, and IEEE 802.1AS
  - Rate shaper can work either at Token Bucket Mode or Credit Based Mode

Security

- Access Control List (ACL)
  - Use L2/L3/L4 flow classification results
  - Blacklist
  - Whitelist
- Access control actions
  - Accept
  - Discard
  - Redirect
  - Port Filtering
  - Cross-state forwarding
  - Cross-VLAN forwarding
  - QoS classification
  - VLAN Service Tag VLAN ID and Custom VLAN ID translation
- Broadcast, unknown multicast and unknown unicast storm control
- Authentication support (IEEE 802.1X Port Authentication)

Other Features

- Spanning Tree/Rapid Spanning Tree and 16 STP instances per port
- Port trunking of any two ports
- Port mirroring
- 802.3az Energy Efficient Ethernet
- Wake-on-LAN
  - Detection of “magic packets”
  - Check WoL password (optional)
  - Wake-up interrupt to external device
- Special Tag
  - Provides in-band packet control and status communication with an internal or external controller
- RMON counters
- Boundary Scan

Power Supply

- Supply voltage domains
  - 3.3 V for digital PAD except RGMII PAD
  - 3.3 V for analog GPHY
  - 1.1 V for digital core
  - 1.1 V for analog GPHY
  - 3.3 V or 2.5 V for digital RGMII PAD

1.2 Applications

The following figures show application examples.

Figure 1 and **Figure 2** show standalone switch applications. An optional external EEPROM is used for switch configuration. In **Figure 1** an optional low cost brightness sensor can also be integrated allowing LED brightness controlled by Gigabit Ethernet Switch to save the system power consumption. In **Figure 2** an optional brightness on/off switch is integrated allowing LED brightness controlled by the switch button to save the system power consumption.

Figure 3 shows an application of home gateway. An external SoC can manage the switch via management interface (eg UART, SPI or MDIO interface). The SoC can also transmit and receive the Ethernet packets via RGMII/GMII interfaces.

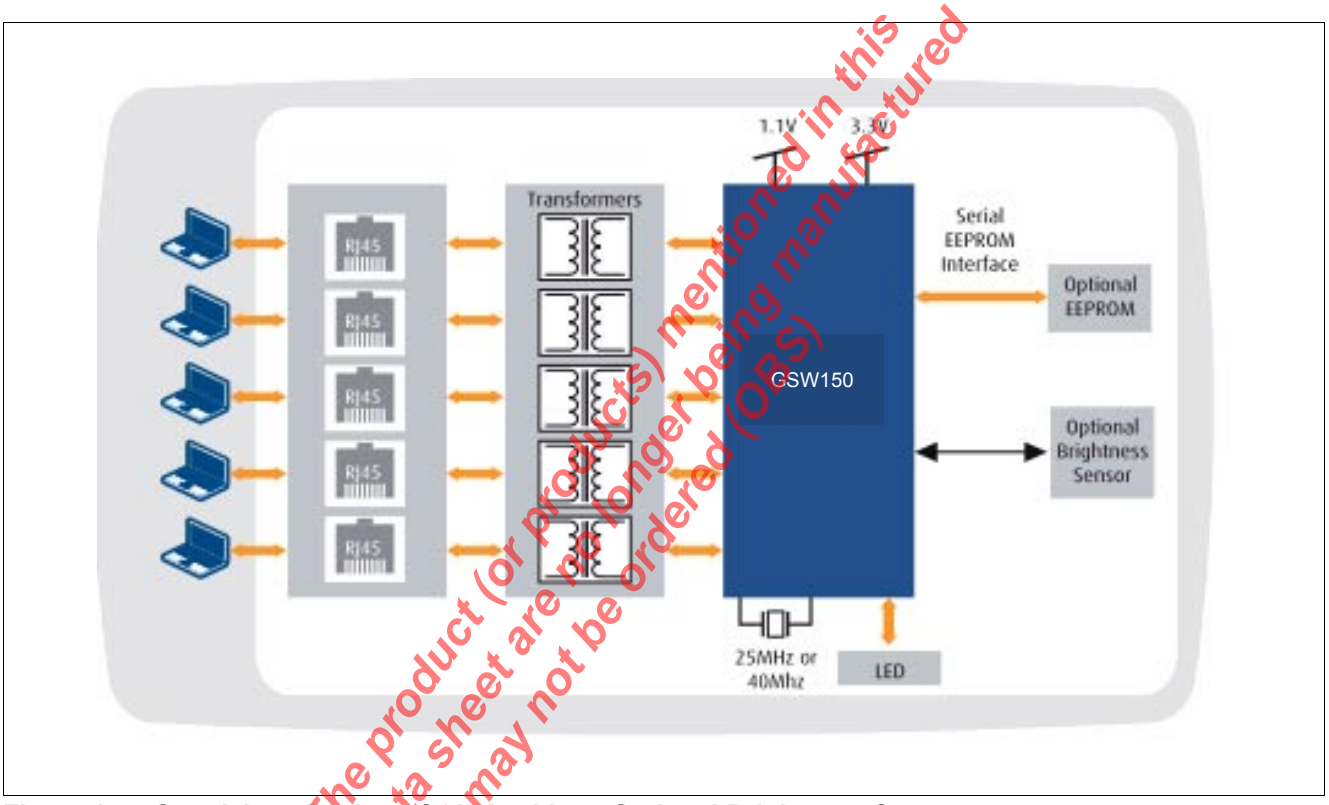


Figure 1 Standalone Desktop Switch with an Optional Brightness Sensor

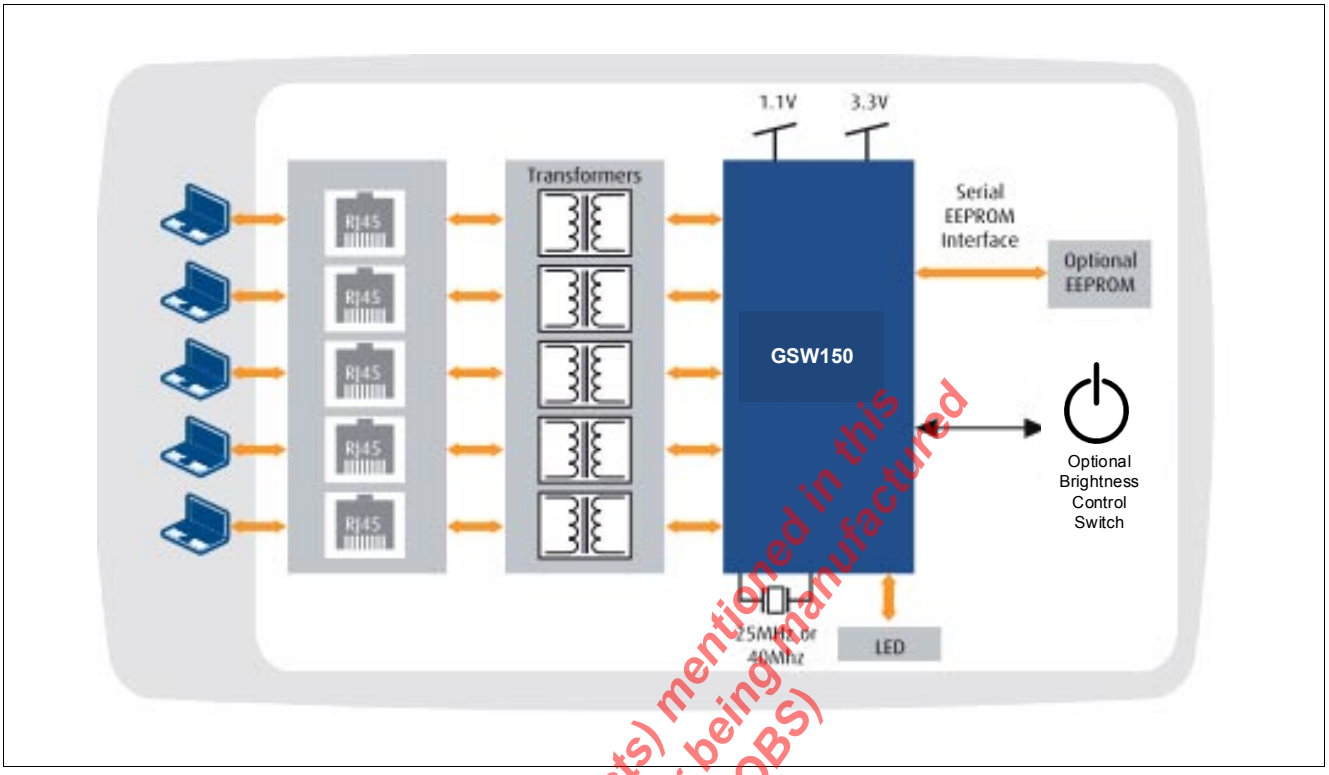


Figure 2 Standalone Desktop Switch with an Optional Brightness On/Off Switch

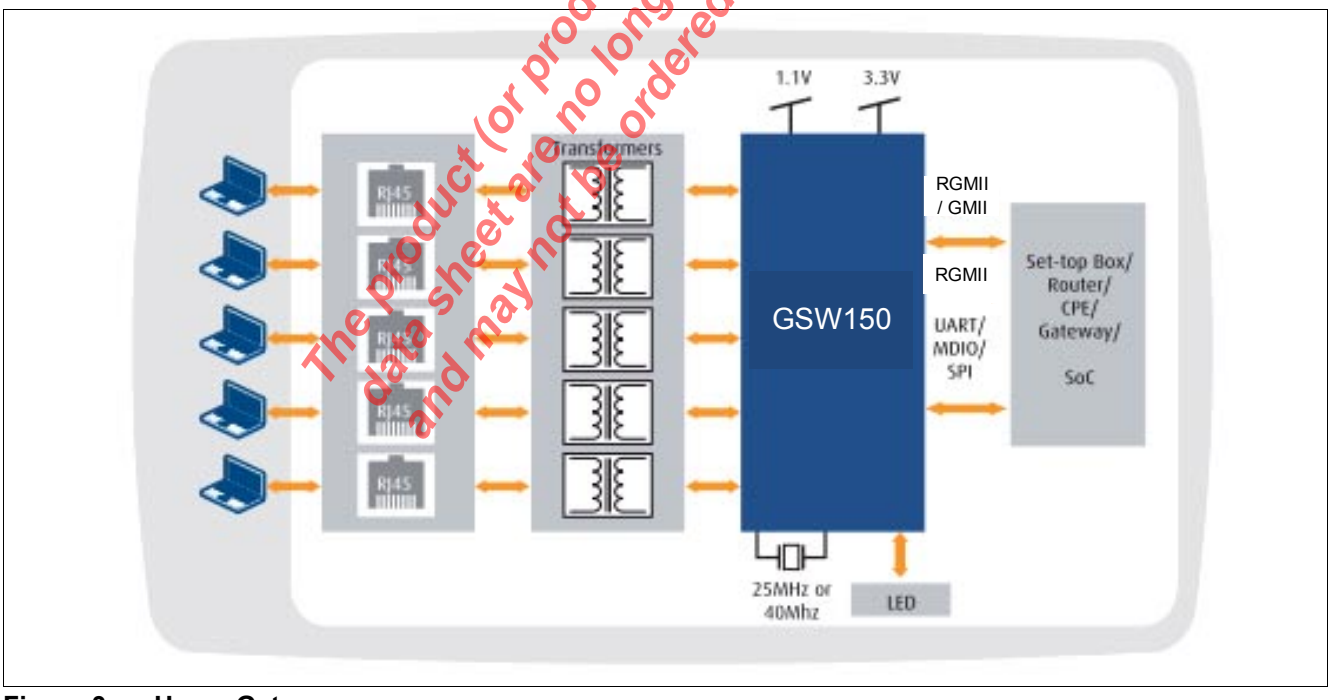


Figure 3 Home Gateway

1.3 Block Diagram

The block diagram is shown in **Figure 4**.

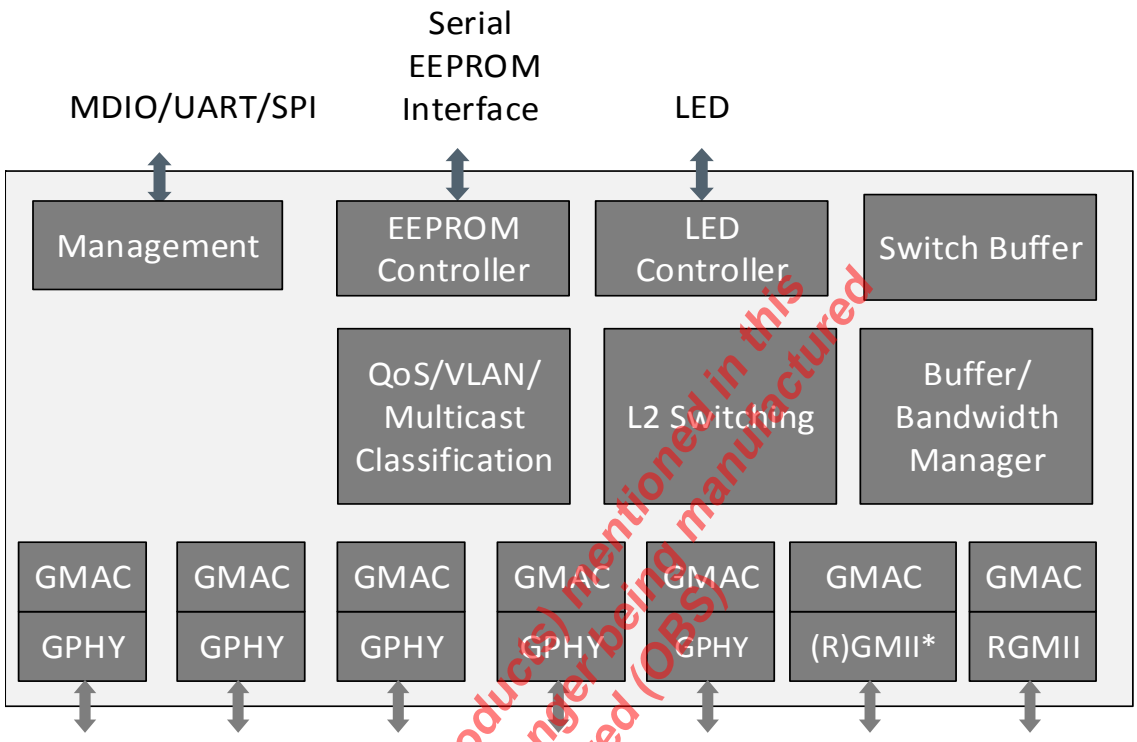


Figure 4 Block Diagram

2 External Signals

This chapter describes the signal mapping to the package.

2.1 Logic Symbol

The figure below gives a global overview of the device's external interfaces.

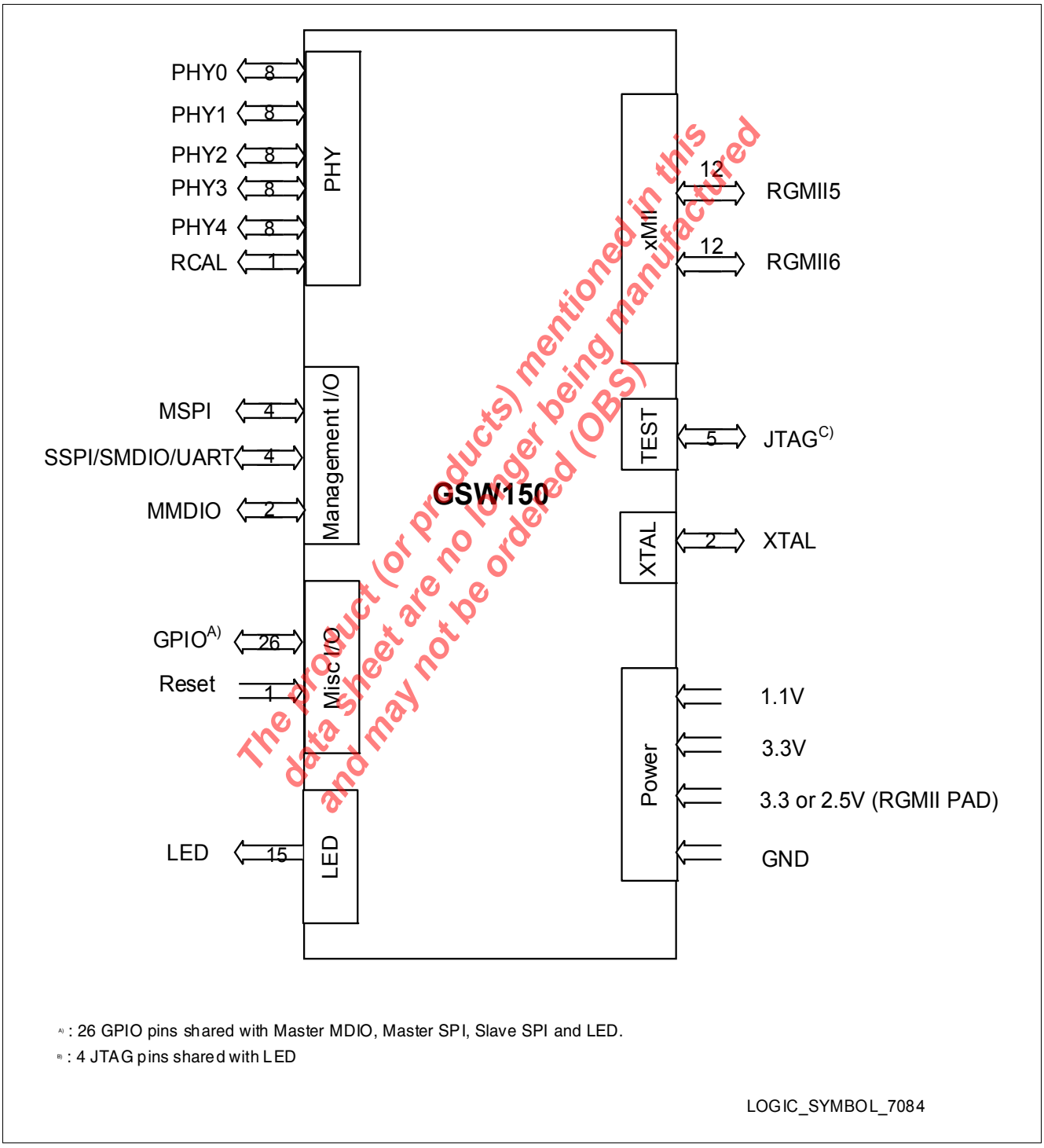


Figure 5 GSW150 Logic Symbol

2.2 External Signal Description

This chapter provides in detail the pin diagrams, abbreviations for pin types and buffer types, as well as the table of input and output signals.

2.2.1 Pin Diagram

The pin layout of the package is shown in **Figure 6**.

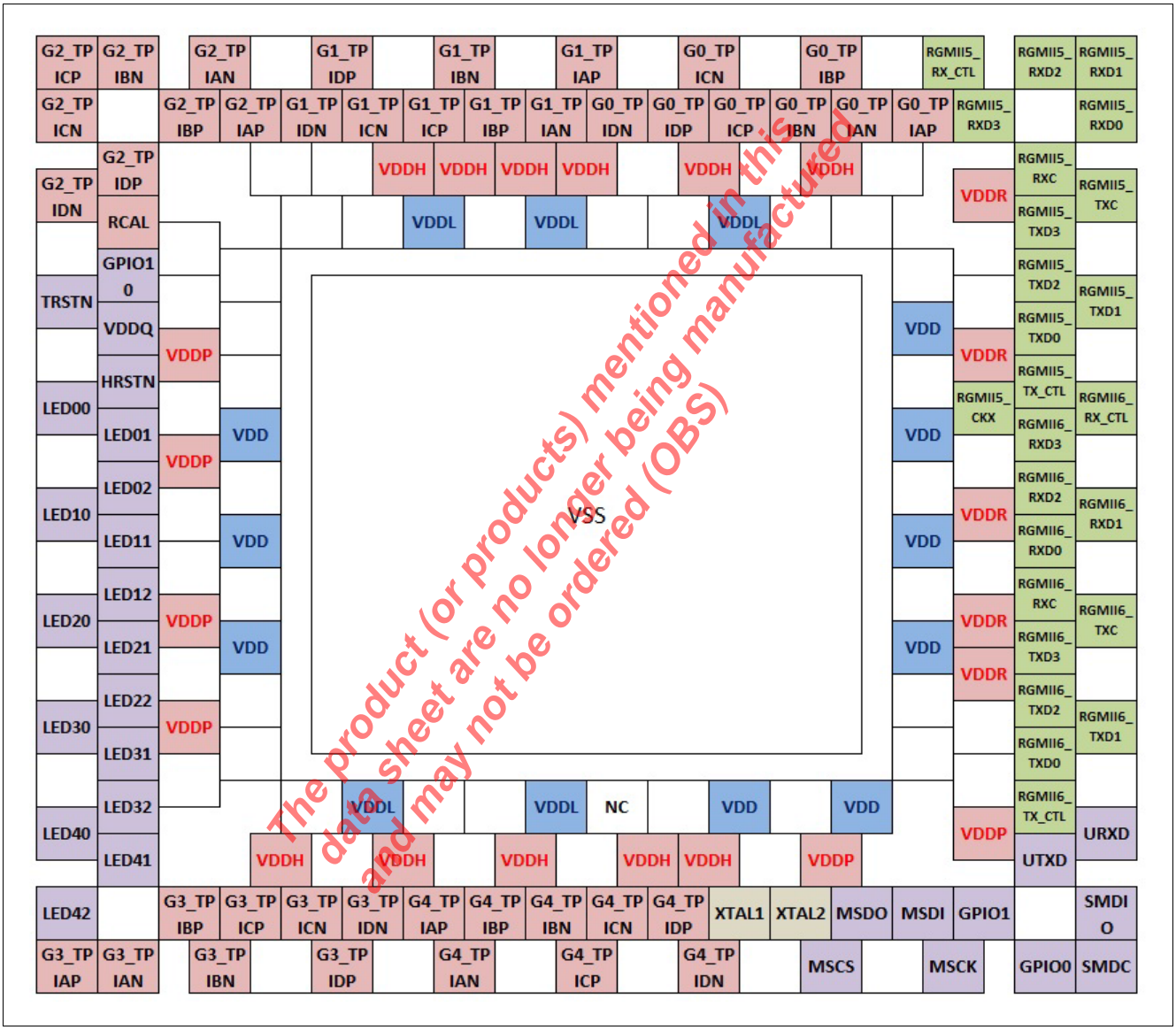


Figure 6 Pin Layout

2.2.2 Abbreviations

Abbreviations that are used in the signal tables are summarized in Table 1 and Table 2.

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Input-only, digital levels
O	Output-only, digital levels
I/O	Bidirectional input/output signal, digital levels
Prg	Bidirectional pad, programmable to operate either as input or output, digital levels
AI	Input-only, analog levels
AO	Output-only, analog levels
AI/O	Bidirectional, analog levels
PWR	Power
GND	Ground

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
LVTTL n	LVTTL characteristics, n = A, B, or C (driver strength)
LVTTL n PU m	LVTTL characteristics with weak pull-up device; n = A, B, or C (driver strength); m = A, B, or C (pull-up strength)
LVTTL n PD m	LVTTL characteristics with weak pull-down device; n = A, B, or C (driver strength); m = A, B, or C (pull-down strength)
LVTTL n OD	LVTTL characteristics with open-drain characteristic, n = A, B, or C (driver strength)
LVTTL n PP	LVTTL characteristics with push-pull characteristic, n = A, B, or C (driver strength)
I2C	I2C bus characteristics, open drain, see the AC/DC specification for more detail.
A	Analog characteristics, see the AC/DC specification for more detail.

2.2.3 Input/Output Signals

A detailed description of all pins is shown in Table 3 to Table 8.

2.2.3.1 Ethernet Media Interface

Table 3 Ethernet Media Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 0 Ethernet Media Interface				
B44	**G0_TPIAP**	AI/AO	A	**Port 0 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
B45	**G0_TPIAN**	AI/AO	A	
A49	**G0_TPIBP**	AI/AO	A	
B46	**G0_TPIBN**	AI/AO	A	
B47	**G0_TPICP**	AI/AO	A	
A51	**G0_TPICN**	AI/AO	A	
B48	**G0_TPIDP**	AI/AO	A	
B49	**G0_TPIDN**	AI/AO	A	
Ethernet Port 1 Ethernet Media Interface				
A53	**G1_TPIAP**	AI/AO	A	**Port 1 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
B50	**G1_TPIAN**	AI/AO	A	
B51	**G1_TPIBP**	AI/AO	A	
A55	**G1_TPIBN**	AI/AO	A	
B52	**G1_TPICP**	AI/AO	A	
B53	**G1_TPICN**	AI/AO	A	
A57	**G1_TPIDP**	AI/AO	A	
B54	**G1_TPIDN**	AI/AO	A	
Ethernet Port 2 Ethernet Media Interface				
B55	**G2_TPIAP**	AI/AO	A	**Port 2 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
A59	**G2_TPIAN**	AI/AO	A	
B56	**G2_TPIBP**	AI/AO	A	
A60	**G2_TPIBN**	AI/AO	A	
E1	**G2_TPICP**	AI/AO	A	
A1	**G2_TPICN**	AI/AO	A	
B1	**G2_TPIDP**	AI/AO	A	
A2	**G2_TPIDN**	AI/AO	A	

Table 3 Ethernet Media Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 3 Ethernet Media Interface				
E2	**G3_TPIAP**	AI/AO	A	**Port 3 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
A16	**G3_TPIAN**	AI/AO	A	
B15	**G3_TPIBP**	AI/AO	A	
A17	**G3_TPIBN**	AI/AO	A	
B16	**G3_TPICP**	AI/AO	A	
B17	**G3_TPICN**	AI/AO	A	
A19	**G3_TPIDP**	AI/AO	A	
B18	**G3_TPIDN**	AI/AO	A	
Ethernet Port 4 Ethernet Media Interface				
B19	**G4_TPIAP**	AI/AO	A	**Port 4 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
A21	**G4_TPIAN**	AI/AO	A	
B20	**G4_TPIBP**	AI/AO	A	
B21	**G4_TPIBN**	AI/AO	A	
A23	**G4_TPICP**	AI/AO	A	
B22	**G4_TPICN**	AI/AO	A	
B23	**G4_TPIDP**	AI/AO	A	
A25	**G4_TPIDN**	AI/AO	A	
Ethernet Port Calibration				
B2	**RCAL**	AI/AO	A	**Calibration for all GPHY Ethernet Ports**

2.2.3.2 Ethernet Media Independent Interface

Attention: The pin functionality in Table 4 highlighted in bold indicates the pin name.

Table 4 Ethernet Media Independent Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 5 Media Independent Interface				
C30	**NC**	I	PD	No Connection for RGMII and GMII Mode
A44	**RGMII5_TXC**	O	PD	RGMII Transmit Clock for pins RGMII5_TX*
	GMII5_TX_CLK	O		GMII Transmit Clock for pins GMII5_TX*
B39	**RGMII5_TXD0**	O		RGMII Transmit Data Bit 0
	GMII5_TXD4	O		GMII Transmit Data Bit 4
A42	**RGMII5_TXD1**	O		RGMII Transmit Data Bit 1
	GMII5_TXD5	O		GMII Transmit Data Bit 5
B40	**RGMII5_TXD2**	O		RGMII Transmit Data Bit 2
	GMII5_TXD6	O		GMII Transmit Data Bit 6
B41	**RGMII5_TXD3**	O		RGMII Transmit Data Bit 3
	GMII5_TXD7	O		GMII Transmit Data Bit 7
B38	**RGMII5_TX_CTL**	O		RGMII Transmit Control
	GMII5_TXD3	O		GMII Transmit Data Bit 3
B42	**RGMII5_RXC**	I	PD	RGMII Receive Clock for pins RGMII5_RX*
	GMII5_RX_CLK	I		GMII Receive Clock for pins GMII5_RX*, _CRS, _COL
A45	**RGMII5_RXD0**	I	PD	RGMII Receive Data Bit 0
	GMII5_RXD0	I		GMII Receive Data Bit 0
E4	**RGMII5_RXD1**	I	PD	RGMII Receive Data Bit 1
	GMII5_RXD1	I		GMII Receive Data Bit 1
A46	**RGMII5_RXD2**	I	PD	RGMII Receive Data Bit 2
	GMII5_RXD2	I		GMII Receive Data Bit 2
B43	**RGMII5_RXD3**	I	PD	RGMII Receive Data Bit 3
	GMII5_RXD3	I		GMII Receive Data Bit 3
A47	**RGMII5_RX_CTL**	I	PD	RGMII Receive Control
	GMII5_RX_DV	I		GMII Receive Data Valid
Ethernet Port 6 Media Independent Interface				
A36	**RGMII6_TXC**	O	PD	RGMII Transmit Clock for pins RGMII6_TX*
	GMII5_CRS	I		GMII Carrier Sense
B31	**RGMII6_TXD0**	O		RGMII Transmit Data Bit 0
	GMII5_TXER	O		GMII Transmit Error
A34	**RGMII6_TXD1**	O		RGMII Transmit Data Bit 1
	GMII5_TXD0	O		GMII Transmit Data Bit 0

Table 4 Ethernet Media Independent Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
B32	**RGMII6_TXD2**	O		RGMII Transmit Data Bit 2
	GMII5_TXD1	O		GMII Transmit Data Bit 1
B33	**RGMII6_TXD3**	O		RGMII Transmit Data Bit 3
	GMII5_TXD2	O		GMII Transmit Data Bit 2
B30	**RGMII6_TX_CTL**	O		RGMII Transmit Control
	GMII5_TX_EN	O		GMII Transmit Enable
B34,	**RGMII6_RXC**	I	PD	RGMII Receive Clock for pins RGMII5_RX*
	GMII5_COL	I		GMII Collision Signal
B35	**RGMII6_RXD0**	I	PD	RGMII Receive Data Bit 0
	GMII5_RXD4	I		GMII Receive Data Bit 4
A38	**RGMII6_RXD1**	I	PD	RGMII Receive Data Bit 1
	GMII5_RXD5	I		GMII Receive Data Bit 5
B36	**RGMII6_RXD2**	I	PD	RGMII Receive Data Bit 2
	GMII5_RXD6	I		GMII Receive Data Bit 6
B37	**RGMII6_RXD3**	I	PD	RGMII Receive Data Bit 3
	GMII5_RXD7	I		GMII Receive Data Bit 7
A40	**RGMII6_RX_CTL**	I	PD	RGMII Receive Control
	GMII5_RX_ER	I		GMII Receive Data Error

2.2.3.3 LED/UART/JTAG Interface

The LED interface is used to connect external LEDs for Ethernet status indication of the Ethernet PHY interfaces. Single and dual color LEDs are supported. There are three LEDs per port. JTAG interface share the pins with LED interface.

Attention: The pin functionality in Table 5 highlighted in bold indicates the pin name.

Table 5 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
LED Signals				
A6	GPIO16	Prg	Prg	**General Purpose IO 16** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED00	O		**LED0 for Port 0** LED control output, freely configurable, drives single-color or dual color LEDs.
A8	GPIO17	Prg	Prg	**General Purpose IO 17** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED10	O		**LED0 for Port 1** LED control output, freely configurable, drives single-color or dual color LEDs.
	TDO	O		**JTAG Serial Test Data Output** JTAG test data output
A10	GPIO18	Prg	Prg	**General Purpose IO 18** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED20	O		**LED0 for Port 2** LED control output, freely configurable, drives single-color or dual color LEDs.
	TDI	I	PU	**JTAG Serial Test Data Input**
A12	GPIO19	Prg	Prg	**General Purpose IO 19** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED30	O		**LED0 for Port 3** LED control output, freely configurable, drives single-color or dual color LEDs.
	TMS	I	PU	**JTAG Test Mode Select**

Table 5 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
A14	GPIO20	Prg	Prg	**General Purpose IO 20** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED40	O		**LED0 for Port 4** LED control output, freely configurable, drives single-color or dual color LEDs.
	TCK	I	PU	**JTAG Test Clock** The signals TDI, TDO and TMS are synchronous subject to this JTAG test clock. *Note: If JTAG Controller is held in reset state, i.e. Intel® Ethernet Switch operates in normal mode, this clock pin does not need to be clocked.*
B6	GPIO21	Prg	Prg	**General Purpose IO 21** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED01	O		**LED1 for Port 0** LED control output, freely configurable, drives single-color or dual-color LEDs.
B8	GPIO22	Prg	Prg	**General Purpose IO 22** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED11	O		**LED1 for Port 1** LED control output, freely configurable, drives single-color or dual-color LEDs.
B10	GPIO23	Prg	Prg	**General Purpose IO 23** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED21	O		**LED1 for Port 2** LED control output, freely configurable, drives single-color or dual-color LEDs.
B12	GPIO24	Prg	Prg	**General Purpose IO 24** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED31	O		**LED1 for Port 3** LED control output, freely configurable, drives single-color or dual-color LEDs.

Table 5 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
B14	GPIO25	Prg	Prg	**General Purpose IO 25** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED41	O		**LED1 for Port 4** LED control output, freely configurable, drives single-color or dual-color LEDs.
B7	GPIO26	Prg	Prg	**General Purpose IO 26** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	LED02	O		**LED0 for Port 0** LED control output, freely configurable, drives dual-color or single color LED.
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input
B9	GPIO27	Prg	Prg	**General Purpose IO 27** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	LED12	O		**LED0 for Port 1** LED control output, freely configurable, drives dual-color or single color LED.
B11	GPIO28	Prg	Prg	**General Purpose IO 28** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	LED22	O		**LED0 for Port 2** LED control output, freely configurable, drives dual-color or single color LED.
B13	GPIO29	Prg	Prg	**General Purpose IO 29** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	LED32	O		**LED0 for Port 3** LED control output, freely configurable, drives dual-color or single color LED.

Table 5 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
A15	GPIO30	Prg	Prg	**General Purpose IO 30** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	LED42	I/O		**LED0 for Port 4** LED control output, freely configurable, drives dual-color or single color LED. This pin is also used for the brightness control switch input.
A4	**TRSTN**	I	PD	**JTAG Test Reset** *Note: The integrated pull-down resistor holds the TAP controller in its reset state if the pin is left open. This is a difference to the JTAG specification given by IEEE 1149.1.*

2.2.3.4 Management Interfaces

Five types of serial management interfaces are provided: SPI master interface, SPI slave interface, MDIO slave interface, MDIO master interface and UART interface.

Attention: The pin functionality in Table 6 highlighted in bold indicates the pin name.

Table 6 Management Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
MDIO Master Interface				
A30	**GPIO0**	Prg	Prg	**General Purpose IO 0** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	GPC0			**General Purpose Clock 0** General Purpose clock for Synchronous Ethernet or external devices.
	EXINT0			**External Interrupt 0** The output characteristic can be selected to be open drain or push-pull.
	MMDIO	I/O		**MDIO Master Data Input/Output** Serial data input and output according to IEEE 802.3, clause 22.
B28	**GPIO1**	Prg	Prg	**General Purpose IO 1** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	GPC1			**General Purpose Clock 1** General Purpose clock for Synchronous Ethernet or external devices.
	EXINT1			**External Interrupt 1** The output characteristic can be selected to be open drain or push-pull.
	MMDC	O		**MDIO Master Clock Output** Serial clock output according to IEEE 802.3, clause 22.
SPI Slave, MDIO Slave Interface and UART Interface				
A32	GPIO2	Prg	Prg	**General Purpose IO 2** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSDI	I		**SPI Slave Data Input** SPI interface data input
	URXD	I		**UART Data Input** UART interface data input

Table 6 Management Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
B29	GPIO3	Prg	Prg	**General Purpose IO 3** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	SSDO	O		**SPI Slave Data Output** SPI interface data output
	UTXD	O		**UART Data Output** UART interface data output
E3	GPIO4	Prg	Prg	**General Purpose IO 4** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSCK	I		**SPI Slave Clock** SPI interface clock
	SMDC	I		**MDIO Slave Clock** The external controller provides the serial clock of up to 25 MHz on this input.
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input
A31	GPIO5	Prg	Prg	**General Purpose IO 5** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSCS	I		**SPI Slave Chip Select** SPI interface chip select
	SMDIO	I/O		**MDIO Slave Data Input/Output** The external controller uses this signal to address internal registers and to transfer data to and from the internal registers
	PWLED	O		**Power LED** LED for indicating power up
SPI Master interface				
B27	GPIO6	Prg	Prg	**General Purpose IO 6** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	MSDI	I		**SPI Master Data Input** SPI interface data input
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input

Table 6 Management Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
B26	GPIO7	Prg	Prg	**General Purpose IO 7** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	MSDO	O		**SPI Master Data Output** SPI interface data output
	PWLED	O		**Power LED** LED for indicating power up.
A29	GPIO8	Prg	Prg	**General Purpose IO 8** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	MSCK	O		**SPI Master Clock** SPI interface clock
A27	GPIO9	Prg	Prg	**General Purpose IO 9** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pinstrapping information during reset.*
	MSCS	O		**SPI Master Chip Select** SPI interface chip select. Active low signal.
B3	**GPIO10**	Prg	Prg	**General Purpose IO 10** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	GPC0			**General Purpose Clock 0** General Purpose clock for Synchronous Ethernet or external devices. It can be selected as input or output mode.
	EXINT0			**External Interrupt 0** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.

2.2.3.5 Miscellaneous Signals

Attention: The pin functionality in Table 7 highlighted in bold indicates the pin name.

Table 7 Miscellaneous Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Reset and Clocking				
B24	**XTAL1**	AI	A	**Crystal: Oscillator Input** A crystal must be connected between XTAL1 and XTAL2. Additional Load Capacitances must tie both pins to the GND.
	CLK	I		**Clock: Clock Input** Direct clock input.
B25	**XTAL2**	AO	A	**Crystal: Oscillator Output** A crystal must be connected between XTAL1 and XTAL2. Additional Load Capacitances must tie both pins to the GND.
B5	**HRSTN**	I	PU	**Hardware Reset** Asynchronous active low device reset.
D16	**NC**			**Not Connected** Leave it open

2.2.3.6 Power Supply

This section specifies the power supply pins.

Table 8 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
C12, C14, C16, C18, C19, C35, C37, C39, C40, C41, C42	**VDDH**	PWR		**High-Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the Line-Driver in the PMA of the GPHY. This supply has to provide a nominal voltage of $V_{DDH}=3.3V$ with a worst case tolerance ±5% at the corners, respectively.
C3, C5, C8, C10, C21, C22	**VDDP**	PWR		**Pad-Voltage Domain P Supply** This is the group of supply pins for the pad-supply of the Intel® Ethernet Switch (excluding RGMII). This supply has to provide a nominal voltage of $V_{DDP}=3.3V$ with a worst case tolerance ±5% at the corners, respectively.
C25,C26, C28, C31, C33	**VDDR**	PWR		**Pad Voltage Domain R Supply** This is the group of supply pins for the RGMII pad-supply of the Intel® Ethernet Switch. This supply has to provide a nominal voltage of $V_{DDR}=3.3V$ or $2.5V$ with a worst case tolerance ±5% at the corners, respectively.
D12, D15, D33, D36, D38	**VDDL**	PWR		**Low-Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the PMA of the GPHY. This supply has to provide a nominal voltage of $V_{DDL}=1.1V$ with a worst case tolerance ±5%.
D4, D6, D8, D18, D20, D23, D25, D27, D29	**VDD**	PWR		**Core-Voltage Domain Supply** This is the group of supply pins for the core voltage domain. It supplies the digital core blocks of the Intel® Ethernet Switch. This supply has to provide a nominal voltage of $V_{DDC}=1.1V$ with a worst case tolerance ±5%.
B4	**VDDQ**	PWR		**Fusing Domain Supply** This pin can be tied to the ground.
EPAD[1)]	**VSS**	GND		**General Device Ground**

1) The EPAD is the exposed pad at the bottom of the package. This pad must be properly connected to the ground plane of the PCB.

3 Functional Description

3.1 Clock and Reset

3.1.1 Clock Generation Unit

A single clock source connects to the system, the internal clock circuit will generate all required clocks through the internal PLL circuits. The clock source shall be 25 MHz or 40 MHz, selected via pin strapping of pin UTXD.

3.1.2 General Purpose Clock Output

There are two general purpose clocks supported. General purpose clock share the pins with other functions.

The general purpose clock output has frequency of 125/N MHz, where N is configurable via register **SYSCLK_CONF** field **SYS3_DIV** and **SYS2_DIV**.

3.1.3 Reset Generation Unit

There are the following reset sources that can bring chip or partial of chip into reset:

- Hardware Reset Input
- Global Software Reset
- Module Software Reset

Hardware input resets all hardware modules and loads pin strapping information into the register. Hardware input reset is the most “thorough” reset among the reset choices. Driving HRSTN pin low causes an asynchronous reset of the entire device. Driving HRST pin high deasserts the reset. The configuration input pin(s) are sampled and latched at the rising edge of HRSTN signal. Hardware reset resets all logics in digital and analog domains.

Global software reset (SRST) is issued by the external controller or by boot loader to reset the whole chip. A global software reset will not latch boot strapping information again. The following registers are not affected by global software reset.

- All clock generation configuration registers
- Pin strapping registers

Individual module software Reset is another type of reset. If software detects a condition which requires the individual module to be reset, a software reset can be performed by writing to a special register, the Reset Request register. Write ‘1’ to **RST_REQ** register to assert software reset and write ‘0’ to **RST_REQ** register to de-assert software reset. The duration of reset is controlled by the software.

3.1.4 Power Up Sequence

VDDP/VDDH must be up before VDDL/VDD.

3.2 Management Interface Functional Description

3.2.1 Management Interface Subsystem Features

The Management Interface Subsystem supports the following features:

- Four concurrent types of management interface:
  - MDIO slave interface or SPI slave interface (share pins with GPIO)
  - UART interface or SPI slave interface (share pins with GPIO)
  - SPI master interface (share pins with GPIO)
  - MDIO master interface (share pins with GPIO)
- MDIO master interface to control PHY devices
  - Support auto polling of internal and external PHY devices registers
  - Support indirect access by command to internal and external PHY devices registers
  - Support programmable MDC clock up to 25 MHz
- SPI master interface connecting to a serial EEPROM
  - Support clock up to 50 MHz
  - Supports automatic switch configuration from external EEPROM memory
  - Support write access to EEPROM by an external controller
  - Supports different EEPROM sizes from 1 Kbit to 1024 Kbit
- SPI slave interface to allow control by an external master (such as router or microcontroller)
  - Maximum SPI interface clock 50 MHz and Minimum SPI interface clock is 2.5 MHz
- MDIO slave to allow control by an external master (such as router or microcontroller)
  - Maximum MDIO interface clock 25 MHz
- UART interface connecting to serial terminal
  - Support various baudrate: 4800, 9600, 19200, 38400, 57600, 115200 (default), 230400, 460800, 921600
  - Supports 8-bit data frame, LSB first
  - Support even parity and no parity mode
  - Support 1 or 2 stop bits
  - Support single read access and single write access via serial terminal
  - Support access abort via special characters

3.2.2 MDIO Master Module

The Management Data Input/Output (MDIO) master module provides the register interface to access external or internal PHY registers. The access is triggered by an internal bus master access or by an automatic PHY status polling function (see **Figure 8**).

This interface is used to configure internal and external PHYs and to read status information (speed, duplex, pause, EEE capability). Access to the MDIO master registers automatically starts a serial access to the internal or external component that is addressed by the PHY address given with the command.

The interface uses the serial protocol defined by IEEE 802.3, clause 22. Up to 32 external devices can be addressed through a 5-bit PHY address (PHYADR). Each of these devices can have up to 32 16-bit registers, selected by a 5-bit register address (REGADR). PHY and register address are given in the command word. Each data transfer covers a 16-bit data word.

High Speed Operation

MDIO master interface configuration is through **MMDC_CFG_1**. The standard MDIO protocol uses a clock rate of 2.5 MHz on MDC, which is also the default setting. To speed up the data exchange, the clock generated on MDC can be increased (if the connected PHY is able to support this). See the AC characteristics for more detail.

MDIO Master Interface Address Assignment

The MDIO address for PHY can be configured through **PHY_ADDR_0**/1/2/3/4/5/6.

Table 9 Default Master MDIO Address Assignment

	Default Address	Configuration Register
Port 0 Internal PHY	0	**PHY_ADDR_0**
Port 1 Internal PHY	1	**PHY_ADDR_1**
Port 2 Internal PHY	2	**PHY_ADDR_2**
Port 3 Internal PHY	3	**PHY_ADDR_3**
Port 4 Internal PHY	4	**PHY_ADDR_4**
Port 5 External PHY	5	**PHY_ADDR_5**
Port 6 External PHY	6	**PHY_ADDR_6**

Automatic Polling State Machine

An automatic polling state machine is implemented to dynamically read the internal and external PHY registers which reflect the status of the link, the link speed, duplex mode, pause capabilities and 802.3az EEE capabilities. If automatic polling state machine is enabled on a port (through **MMDC_CFG_0**), the PHY status is read out and corresponding MAC module is configured accordingly.

When MDIO Master interface is accessed by the management action (using the dedicated indirect MDIO register access) it has the higher priority over the auto-polling state machine.

If the MDIO auto-polling state machine is disabled, the link speed, link duplex mode, link status, the pause settings and 802.3az EEE settings hold the previous polled values and can also be configured by the explicit management action.

The port loop of the auto-polling FSM is shown in **Figure 7**. The auto-polling FSM goes sequentially over all ports that are enabled for auto-polling and applies the auto-polling main loop. The gap between each auto polling main loop is programmable via register **MMDC_CFG_0** field **GAP**. Ports that are disabled for auto-polling will be skipped. The polling sequence is repeated constantly in an infinite loop.

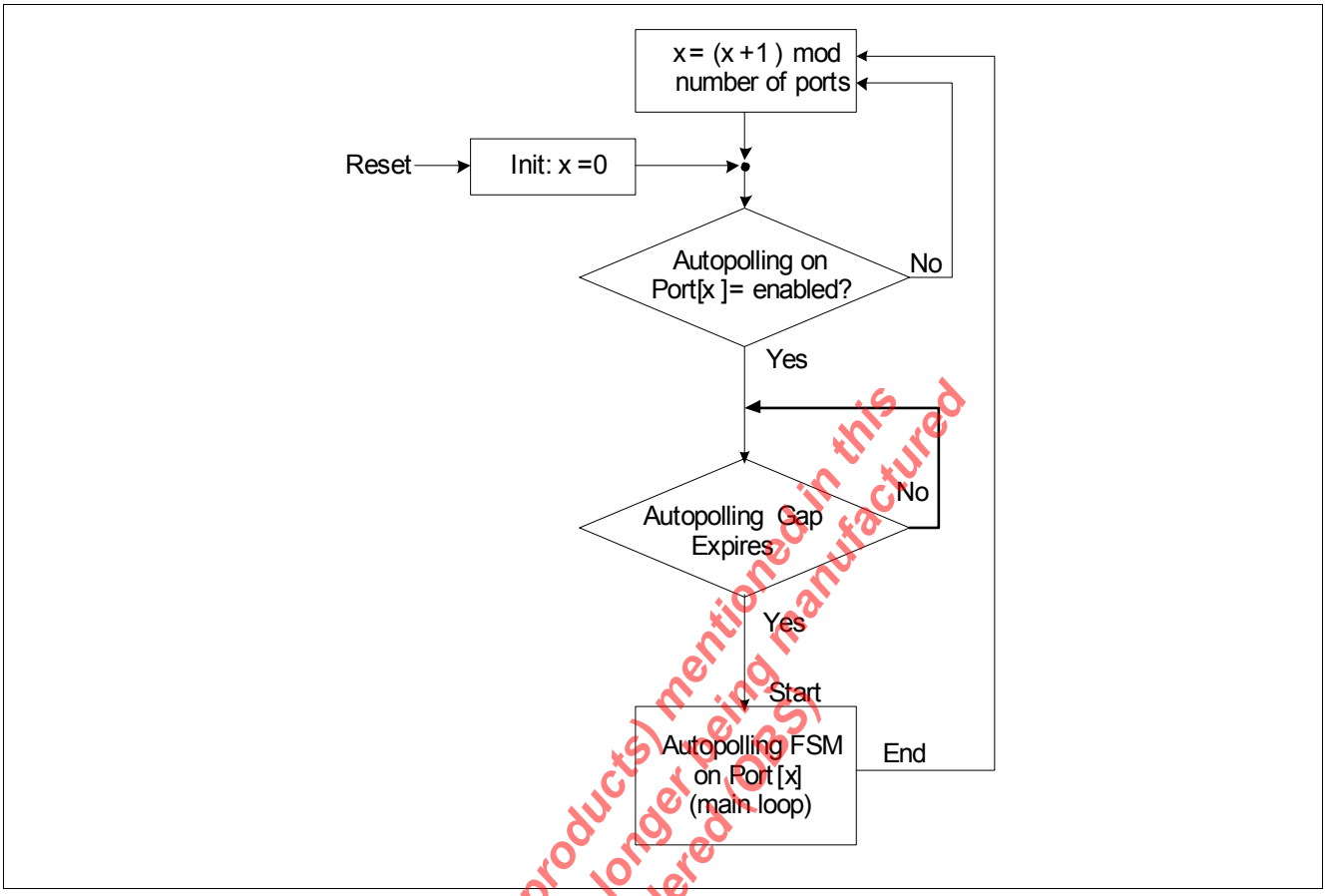


Figure 7 Auto-polling FSM - Port Loop

Figure 8 describes the main loop of the auto-polling state machine. The state machine reads the PHYs' registers in the following sequence:

1. Read REG0 and check if the PHY is connected. If the value of the register is all ones, no PHY is assumed to be connected and PHY Inactive status is reported.
2. PHY support of the autonegotiation (ANEG) is checked in Bit 12 of the REG0. If PHY doesn't support ANEG, duplex and speed are based on REG0 settings. Link is based on the bit 2 of REG1. Pause capability is set to the maximum (support symmetric and asymmetric pause).
3. Bit 5 of the REG1 is checked for ANEG status. If ANEG is not complete - current FSM cycle for this port breaks and the Link Status reported as zero. Status of this port will be checked again in the next round.
4. If ANEG is complete, the FSM branches based on the bit 8 in REG1. In case there is no extended status supported, the attached PHY is a FE PHY. In case extended status is supported (REG1.8=1_B) the PHY is GE PHY.
5. For FE PHY, REG5 (partner) and REG4 (local) are fetched for the speed/duplex/pause autonegotiation result.
6. For GE PHY REG10 (partner) and REG9 (local) are fetched in addition to the FE abilities. REG15 bit 12 to 15 are checked for the 1000BASE-X or 1000BASE-T capability.
7. If bit 1 in REG6 for GE PHY doesn't indicate reception of the next page, the PHY considered to perform parallel detection and speed/duplex/pause will be based on the REG4 and REG5 as in the FE PHY case.
8. EEE capability and advertising registers are fetched.
9. Auto resolution function is applied in the end, based on the fetched result and appropriate status info is reported to the MAC module.

Note: If automatic polling is enabled, PHY status registers are regularly read. This causes the latching status bits to be reset. If the software needs to read out the latched status information, the automatic polling must be disabled.

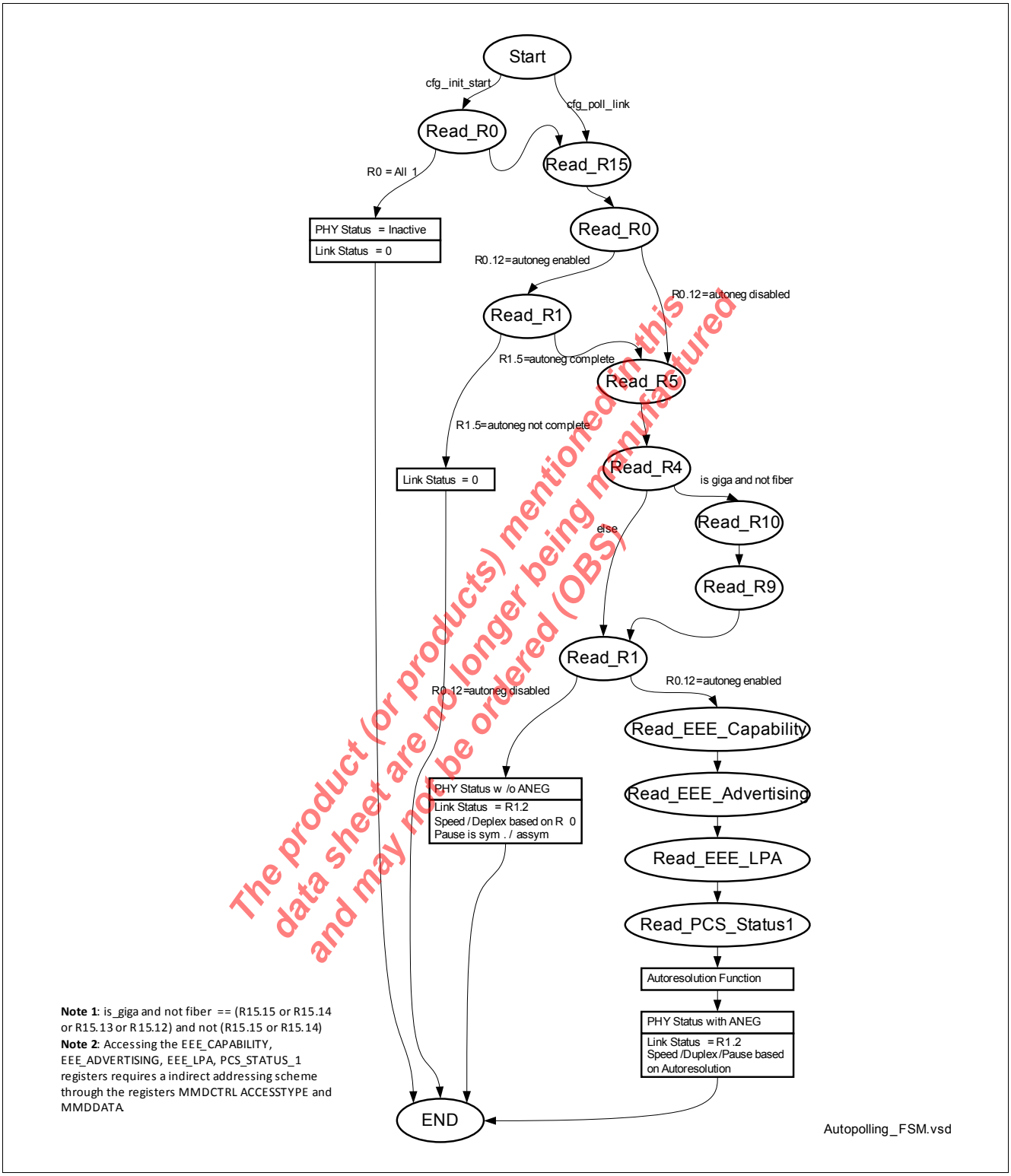


Figure 8 Auto Polling FSM - Main Loop

MDIO Master Indirect Access

When MDIO Master interface is accessed by the management action (using the dedicated indirect MDIO register access through **MMDIO_CTRL**, **MMDIO_READ** and **MMDIO_WRITE**). It has the higher priority over the auto-polling state machine.

Only single access is supported.

Single Read Access:

Reading data from a PHY register through indirect access is performed in following steps:

The first step can be skipped for the following consecutive access.

1. Read status **MMDIO_CTRL**.
2. If **MMDIO_CTRL.MBUSY** is 0_B, write “operation mode”, “target PHY address” and “target register address” to **MMDIO_CTRL**.
   a) **OP** = 10_B (read)
   b) **PHYAD** = Target PHY Address
   c) **REGAD** = Target Register Address
3. Read status **MMDIO_CTRL**
4. If **MMDIO_CTRL.MBUSY** is 0_B, read data from **MMDIO_READ**.
   a) **RDATA**= [result from target register]

Single Write Access:

Writing data to a PHY register through indirect access is performed in following steps:

1. Read status **MMDIO_CTRL**
2. If **MMDIO_CTRL.MBUSY** is 0_B, write the target data to **MMDIO_WRITE**.
   a) **WDATA** = [data to be written]
3. Write “operation mode”, “target PHY address” and “target register address” to **MMDIO_CTRL**.
   a) **OP** = 01_B (write)
   b) **PHYAD** = Target PHY Address
   c) **REGAD** = Target Register Address

3.2.3 MDIO Slave Module

An external controller can be connected to the switch’s slave MDIO interface. The chip behaves as MDIO slave similar to an PHY as shown in **Figure 9**. Via indirect addressing the external controller is able to access all internal registers. MDIO Slave module is a master of internal bus. Read and write requests of MDIO slave are translated to read and write requests to internal bus.

For the access to the external or internal PHYs the chip serves as a proxy for the external controller. The external controller has to write the PHY address, the PHY register address, the command (read/write) and the corresponding data into internal registers. Based on the information which has been written, the information is translated into an MDIO frame and sent via the MDIO master interface to the destination PHY.

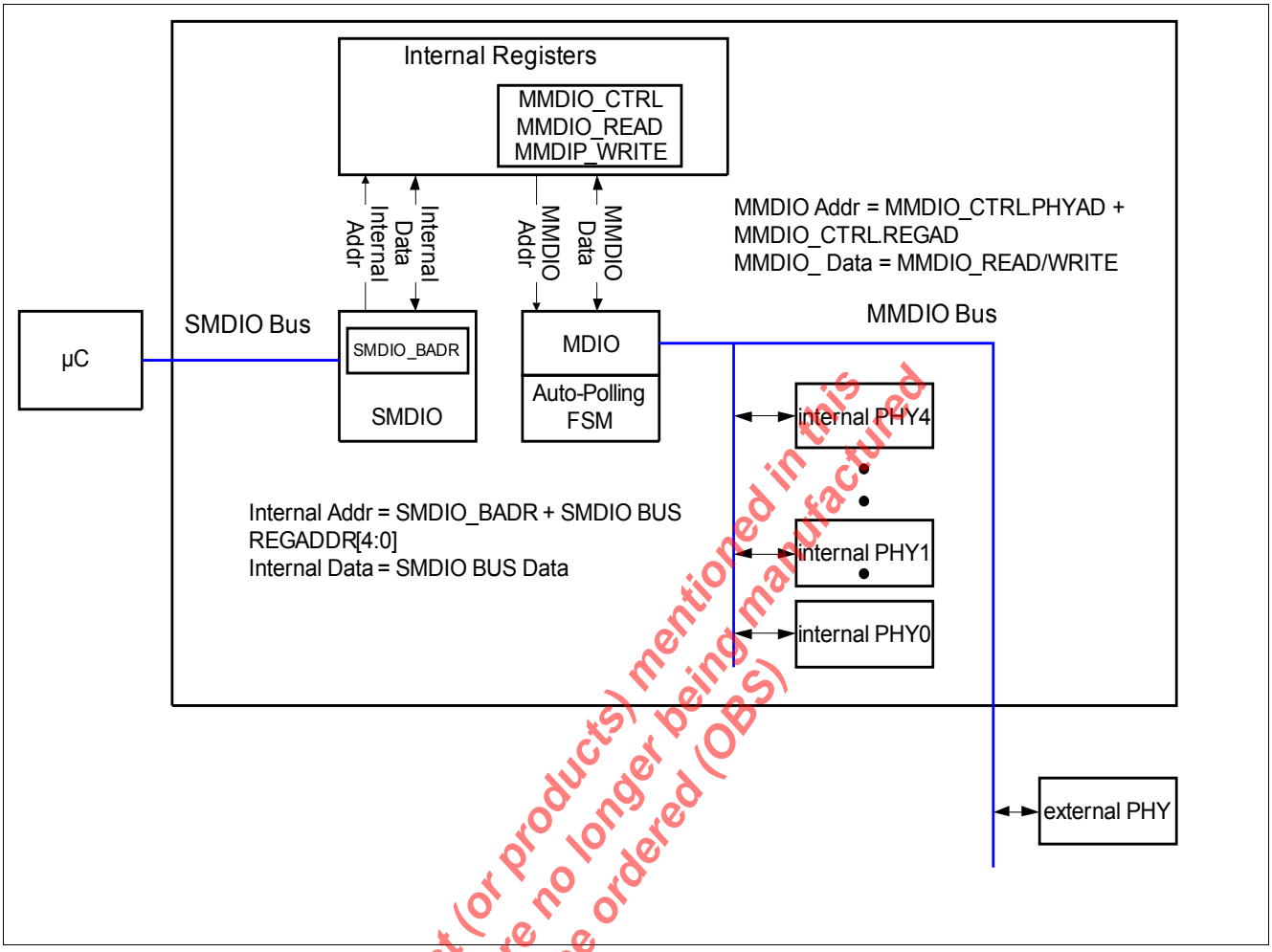


Figure 9 MDIO Proxy in Switching Mode

If other devices in the system need to be configured through MDIO, they shall either be connected to the MDIO master interface or, if connected to the MDIO slave interface, must be configured such that no addressing conflict arises.

The interface can uses the standard MDIO protocol which provides vendor-specific registers in the upper 5-bit REGADR range. Within this range there are certain registers which allow an indirect access to multiple internal configuration and status registers.

The standard MDIO protocol requires a 32-bit preamble at the beginning of each read or write access. To speed up the data exchange, the preamble can be reduced down to 1 bit for the second and following subsequent accesses.

The standard MDIO protocol uses a clock rate of 2.5 MHz on MDC. To speed up the data exchange, the clock applied on SMDC can be increased to maximum 25 MHz. See the AC characteristics for more detail.

The bus protocol used for the MDIO slave interface is the same as defined for MDIO master interface. The PHY address (PHYADR) range usage is shown in **Table 9**. Internal registers can be read or written in single or sequential access mode. In sequential access mode, multiple accesses are possible to registers that are located at subsequent internal addresses.

The SMDIO address used for indirect access is configurable through pin-strapping. The SMDIO address can be reconfigured via **SMDIO_CFG.ADDR**.

After hardware reset, MDIO slave interface is enabled. MDIO slave interface is multiplexed with SPI slave interface. MDIO and SPI slave cannot be enabled at the same time. If both are enabled, MDIO slave interface is used. If both interfaces are disabled and all the 4 pins used for MDIO slave and SPI slave are input only.

Single Read Access

Reading data from an internal register through indirect access is performed in following steps:

The first step can be skipped for consecutive access.

1. Write Base Address Register **SMDIO_BADR**
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Read Target Data
   a) OPCODE[1:0] = 10_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Read Data from Target]

Multiple Read Access

Reading data from an internal register through indirect access can also access the same register multiple times or the consecutive register within a range. This can be used, for example, to read from a FIFO-style memory through a single register address or to poll a register for a certain value. The sequence is as follows:

1. Write Base Address Register **SMDIO_BADR**
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Read Target Data
   a) OPCODE[1:0] = 10_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Read Data from Target]
3. Repeat Step 2 if the target register address is within offset 0 to 30 from the target base address

Single Write Access

Writing data to an internal register through indirect access is performed in following steps:

1. Write Base Address Register **SMDIO_BADR**
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Write Target Data
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Write data To Target]

Multiple Write Access

Writing data to an internal register through indirect access can also access the same register multiple times or the consecutive register within a range. This can be used, for example, to write a FIFO-style memory through a single register address or to write a register for a certain value. The sequence is as follows:

1. Write Base Address Register
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Write Target Data
   a) OPCODE[1:0] = 01_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Write Data to Target]
3. Repeat Step 2 if the target register address is within offset 0 to 30 from the target base address

3.2.4 SPI Master Module

It supports the following functions:

- Configuration download from an external serial EEPROM after hardware reset or global software reset is triggered.
- Configuration upload to an external serial EEPROM during run time after initialization is done

Operation

External or internal controller can control SPI master interface via SPI access registers. Operation relies on regular interrupt that is asserted at the boundary of 8-bit transactions. SPI interrupt indicates that data out buffer is ready to be written and data in carries the valid data and is ready for reading.

Operation Configuration:

- First Set **MSPI_CFG.MDSEL** to 1_B
- Wait until **MSPI_OP.MDSTA** = 1_B
- Do single or multiple manual access

Single Read Access Operation:

- Write address to **MSPI_DIN01**/**MSPI_DIN23**.
- Configure **MSPI_MANCTRL.SIZE** = number of bytes and **MSPI_MANCTRL.START** to 1_B
- Wait for SPI interrupt **MSPI_ISR.DONE** = 1_B
- Write 1_B to **MSPI_ISR.DONE** to clear interrupt
- Read **MSPI_DOUT01**/**MSPI_DOUT23**/**MSPI_DOUT45**/**MSPI_DOUT67**

Single Write Access Operation:

- Configure **MSPI_DIN01**/**MSPI_DIN23**/**MSPI_DIN45**/**MSPI_DIN67**.
- Configure **MSPI_MANCTRL.SIZE** = number of bytes and **MSPI_MANCTRL.START** to 1_B
- Wait for SPI interrupt **MSPI_ISR.DONE** = 1_B
- Write 1_B to **MSPI_ISR.DONE** to clear interrupt

3.2.5 SPI Slave Access

Intel® Ethernet Switch can work as SPI slave. An external controller can manage Ethernet Switch via SPI slave interface.

SPI Slave module is a master of internal bus. Read and write requests of SPI are translated to read and write requests to internal bus.

SPI Slave follows the 16-bit/24-bit serial EEPROM like protocols (for WRITE/READ respectively) as shown in timing diagrams **Figure 10**:

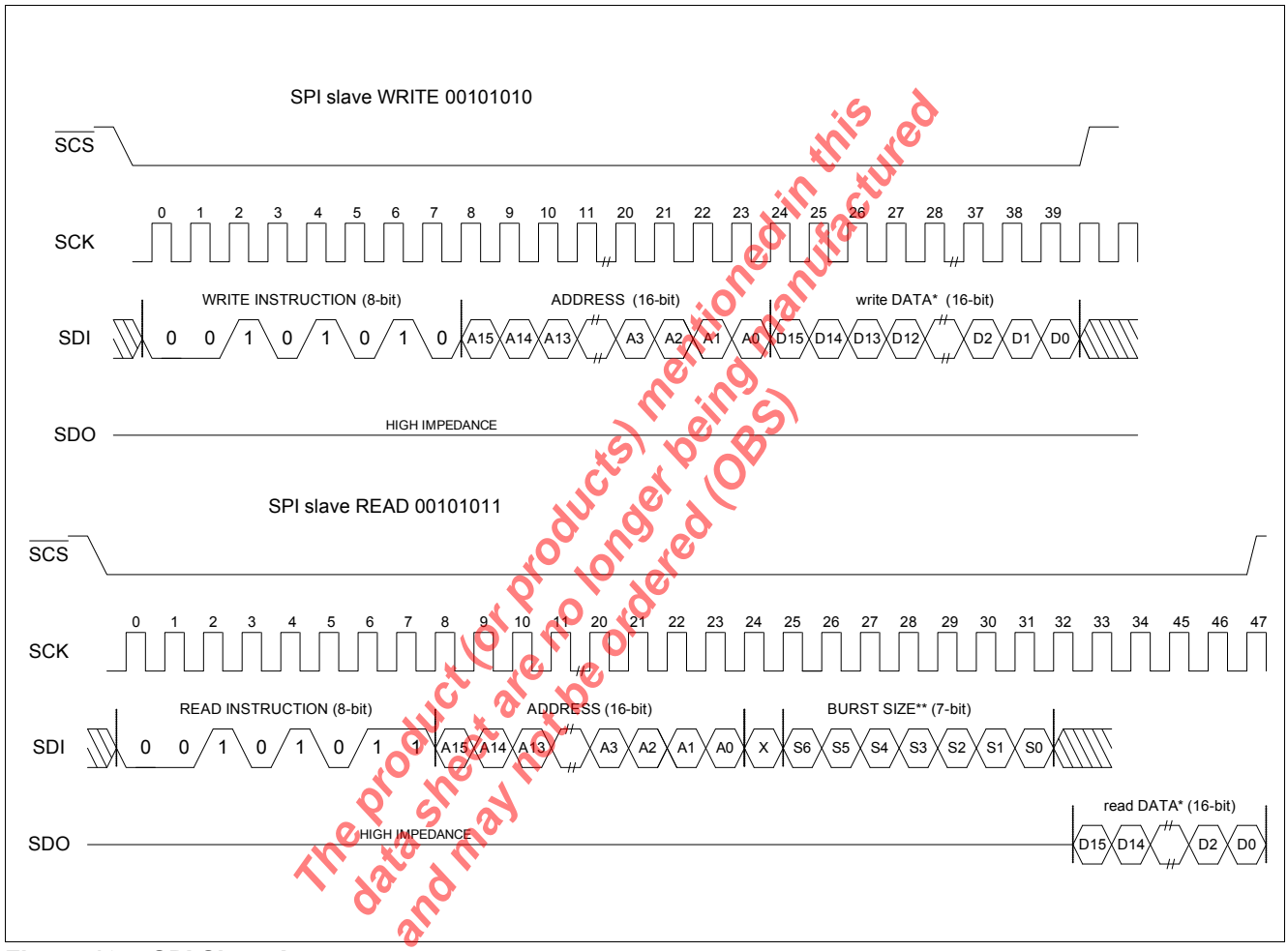


Figure 10 SPI Slave Access

The maximal SCK frequency of 50 MHz and the minimum SCK frequency of 2.5 MHz is supported.

Two major synchronization techniques are used:

- In SDI direction, special preamble like "001010" is used to adjust sampling edge to middle of the stable region. Preamble is part of READ or WRITE command.
- In SDO direction, delay is adjustable in steps of 4ns from rising or falling edge of SCK.
  - delay is (3+ **SSPI_CFG.DRVDLY**)*4ns if **SSPI_CFG.DRVDLY** /= 0
  - delay is 4*4ns if **SSPI_CFG.DRVDLY** = 0
- SDO can also be driven up to 2 SCK cycles earlier than the sequence defined in **Figure 10**.
  - if **SSPI_CFG.REFCYC** = 0, SDO is driven 2 SCK cycles earlier than the sequence defined in **Figure 10**.
  - if **SSPI_CFG.REFCYC** = 1, SDO is driven 1 SCK cycles earlier than the sequence defined in **Figure 10**.
  - if **SSPI_CFG.REFCYC** = 2, SDO is driven as the sequence defined in **Figure 10**.
  - if **SSPI_CFG.REFCYC** = 3, SDO is driven 1 SCK cycles after than the sequence defined in **Figure 10**

- when **SSPI_CFG.SDIEGSEL** is set to 0, SDI is latched with the rising edge of SCK (for example in case when the master is driving SDI with the falling edge of SCK)
- when **SSPI_CFG.SDIEGSEL** is set to 1, SDI is latched with the falling edge of SCK (for example in case when the master is driving SDI with the rising edge of SCK)

3.2.6 UART Access

UART supports connection to internal bus of chip via a standard com terminal emulator running on UNIX or Windows. UART module is a master of internal bus. Read and write requests of UART are translated to read and write requests to internal bus. Three commands supported are:

```
> r address16
> w address16 write_data16
> m address16 write_data16 enable_data16
```

The UART module echoes the commands as is, ignoring any character that does not match the command format. The return value of r address16 command includes read_data16 on a new line.

The format of address16, write_data16 and enable_data16 are four consecutive hexadecimal digits between 0000_H and $FFFF_H$ or $FFFF_H$. The returned read_data16 is same format in lower case.

After chip reset, UART is in line monitoring state, searching line for valid byte. This must be preceded by at least 12 consecutive ones, (IDLE). When first error-free byte is detected, UART module responds by sending a system message:

System ready! Use:r/w <addr> <data>

followed by prompt sequence:

'\r\n' and '>'

where the '\r' ASCII(13) can be disabled by setting **UART_CFG.CRDIS**=1 and the '\n' ASCII(10) can be disabled by setting **UART_CFG.LFDIS**=1 in order to adjust new line sequence to different platforms (UNIX, MAC, Windows)

The default prompt character '>' can be changed by **UART_PROMPT.Promt0** and **UART_PROMPT.Promt1**. Up to two prompt characters are supported. Setting the character to zero disables this character.

In addition to 3 commands, the character '#' can be used as a first character of the line and the rest of the line will be ignored. The character '#' and following characters are not echoed. In line comment, following the valid command, will be ignored as invalid character sequence and no other special handling is required.

When using UART from terminal, the basic editing facilities are provided using '\b' 'backspace' character, ASCII(8). 'b' will erase a single character on the current line that is echoed. Ignored characters cannot be erased. Multiple 'b' characters can erase the line up to the prompt. Prompt will not be erased.

Any command can be aborted by DEL ASCII(127) or ESC(27) characters. The indication of abort of a command is done by '$' character. Abort of empty line is not indicated by '$' character.

The following baudrates are supported: 4800, 9600, 19200, 38400, 57600, 115200 (default), 230400, 460800, 921600. The baudrate is programmed via **UART_BD** and **UART_FDIV**. **UART_BD** is the whole part of divider and **UART_FDIV** is the fractional part of the divider.

Only 8-bit data format is supported. Parity can be enabled or disabled (default) via **UART_CFG.PAREN**. Even parity is supported. In receive direction any number of stop bits is supported. In transmit direction, the number of stop bits is configured via **UART_CFG.STOP**.

3.2.7 Boot Loader Description

The device supports the following boot modes:

- Wait for external master (via SPI Slave, MDIO slave or UART)'s configuration and trigger
- Self-start mode (External EEPROM not attached)
- SPI master EEPROM mode (External EEPROM attached)

The boot mode is determined by pin strapping (please refer to **Pin Strapping**).

Wait For External Master Procedure (PS_NOWAIT = 0_B)

If pin strapping indicates that boot mode is "wait for external master", boot loader only configures slave interface according to pin strapping. External master shall configure and enable Gigabit Ethernet Switch core operation.

Self-start Mode Procedure (PS_NOWAIT = 1_B)

If pin strapping indicates that boot mode is not "wait for external master" and no EEPROM is attached, boot loader configures the registers according to pin strapping values as shown in **Table 10** and **Table 11**.

Table 10 shows Registers Configuration for "Self-start" Mode: "Standalone Unmanaged Switch" Sub-Mode (PS_OP_MD = 01_B).

Table 10 Registers Configuration for "Self-start" Mode: "Standalone Unmanaged Switch" Sub-Mode

Register	Field	Description	Note
GPHY0_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY1_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY2_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY3_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY4_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPIO_ALTSEL0	Bit 5 to 4	$=11_B$	Enable "PWLED" Alternate Function on GPIO7 Enable "Light" Alternate Function on GPIO6
GPIO_ALTSEL1	Bit 5 to 4	$=11_B$	Enable "PWLED" Alternate Function on GPIO7 Enable "Light" Alternate Function on GPIO6
GPIO_PUDEN	Bit 5 to 4	$=00_B$	Disable "PWLED" and "LIGHT" Pin Pull up and pull down
GPIO_OUT	Bit 5	$= 1_B$	Turn on Power LED
GPIO_DRIVE0_CFG	Bit 5	$= 1_B$	Change "PWLED" drive strength to 12 mA
GPIO2_ALTSEL0	All field	Depends on LED Mode of Pin strapping	Configured according to **Table 12**
GPIO2_PUDEN	All field	Depends in LED Mode of Pin strapping	Configured according to **Table 12**
GPIO2_DRIVE0_CFG	All field	Depends in LED Mode of Pin strapping	Configured according to **Table 12**
MII_CFG_5	Bit 14:13	If PS_SUBTYPE_MD[0] is 1_B: $=10_B$	Enable RGMII5 interface according to pin strap

Table 10 Registers Configuration for "Self-start" Mode: "Standalone Unmanaged Switch" (cont'd)**Sub-**

Register	Field	Description	Note
MII_CFG_6	Bit 14:13	If PS_SUBTYPE_MD[0] is 1_B: $=10_B$	Enable RGMII6 interface according to pin strap
PHY_ADDR_5	All fields	If PS_SUBTYPE_MD[2] is 1_B and PS_SUBTYPE_MD[0] is 1_B: $= 32A5_H$	For RGMII5 interface, force link on, speed is 1Gbps, full duplex, pause enable according to pin strap.
PHY_ADDR_6	All fields	If PS_SUBTYPE_MD[1] is 1_B and PS_SUBTYPE_MD[0] is 1_B: $= 32A6_H$	For RGMII6 interface, force link on, speed is 1Gbps, full duplex, pause enable according to pin strap.
GSWIP PCE_PCTRL_2 for Port 3	All Field	$=0001_H$	Enable higher priority for port 3
GSWIP PCE_PCTRL_2 for Port 4	All Field	$=0001_H$	Enable higher priority for port 4
BM_WRED_GTH_0	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
BM_WRED_GTH_1	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
MAC_CTRL_4 (for each port)	All Fields	$=1494_H$	Enable EEE LPI Mode for each port
SDMA_PFCTHR8 (for each port)	All Fields	$=0018_H$	Configure backpressure watermark for each port
SDMA_PFCTHR9 (for each port)	All Fields	$=001E_H$	Configure backpressure watermark for each port
SDMA_FCTHR1	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR2	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR3	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR4	All Fields	$=03FF_H$	Configure tail drop watermark
Buffer Reservation for each queue	All Fields	$=001E_H$	Buffer Reservation for each queue is 30 segments
WRED green min/max for each queue	All Fields	$=03FF_H$	Configure WRED green min/max for each queue
Queue weight for each queue	All Fields	$=FFFF_H$	Enable strict priority
GSWIP MAC_CTRL_2	Bit 15 to 0	$= 000D_H$	Enable GSWIP Jumbo Support up to 9.6K
GSWIP_CFG	All Fields	$=8000_H$	Enable GSWIP and all ports

Table 11 shows Registers Configuration for "Self-start" Mode: "Managed Switch" Sub-Mode when PS_OP_MD = $1x_B$.

Table 11 Registers Configuration for "Self-start" Mode: "Managed Switch" Sub-Mode

Register	Field	Description	Note
Following Configurations If PS_OP_MD is "11"			
SMDIO_CFG	Bit 8 to 4	if PS_SUBTYPE_MD[1:0] is 0: = 0_H if PS_SUBTYPE_MD[1:0] is 1: = 4_H if PS_SUBTYPE_MD[1:0] is 2: = 10_H if PS_SUBTYPE_MD[1:0] is 3: = $1F_H$	Configure SMDIO Address
Following Configurations if PS_OP_MD is "10"			
SSPI_CFG	Bit 15	=~PS_SUB_MD[0]	SDO Driving Edge Selection
SSPI_CFG	Bit 14	=~PS_SUB_MD[1]	SDI Sampling Edge Selection
SSPI_CFG	Bit 0	$=1_B$	Enable SSPI
GPIO_ALTSEL0	Bit 5 to 2	$=1111_B$	Change GPIO to alternate function SSPI
GPIO_ALTSEL1	Bit 5 to 2	$=0000_B$	Change GPIO to alternate function SSPI
Configurations if PS_OP_MD is "1X"			
MII_CFG_5	Bit 14:13	$=10_B$	Enable RGMII5 interface
MII_CFG_6	Bit 14:13	$=10_B$	Enable RGMII6 interface
PHY_ADDR_5	All fields	$= 32A5_H$	For RGMII5 interface, force link on, speed is 1 Gbps, full duplex, pause enable
PHY_ADDR_6	All fields	$= 32A6_H$	For RGMII6 interface, force link on, speed is 1 Gbps, full duplex, pause enable
PCDU_5	Bit 9:7	if PS_SUBTYPE_MD[4] is 1_B: = 4	Setting RGMII RX delay to 2ns
PCDU_5	Bit 2:0	if PS_SUBTYPE_MD[3] is 1_B: = 4	Setting RGMII TX delay to 2ns
PCDU_6	Bit 9:7	if PS_SUBTYPE_MD[4] is 1_B: = 4	Setting RGMII RX delay to 2ns
PCDU_6	Bit 2:0	if PS_SUBTYPE_MD[3] is 1_B: = 4	Setting RGMII TX delay to 2ns
BM_WRED_GTH_0	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
BM_WRED_GTH_1	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation

Table 11 Registers Configuration for "Self-start" Mode: "Managed Switch" (cont'd)**Sub-Mode**

Register	Field	Description	Note
MAC_CTRL_4 (for each port)	All Fields	$=1494_H$	Enable EEE LPI Mode for each port
SDMA_PFCTHR8 (for each port)	All Fields	$=0018_H$	Configure backpressure watermark for each port
SDMA_PFCTHR9 (for each port)	All Fields	$=001E_H$	Configure backpressure watermark for each port
SDMA_FCTHR1	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR2	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR3	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR4	All Fields	$=03FF_H$	Configure tail drop watermark
Buffer Reservation for each queue	All Fields	$=001E_H$	Buffer Reservation for each queue is 30 segments
WRED green min/max for each queue	All Fields	$=03FF_H$	Configure WRED green min/max for each queue
Queue weight for each queue	All Fields	$=FFFF_H$	Enable strict priority
GSWIP MAC_CTRL_2	Bit 15 to 0	$= 000D_H$	Enable GSWIP Jumbo Support up to 9.6K
GSWIP_CFG	All Fields	$=8000_H$	Enable GSWIP and all ports

Table 12 LED Status VS LED Mode

LED Mode	LEDx0	LEDx1	LEDx2	Configuration
0	10 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	100 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	1000 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	**GPIO2_ALTSEL0**=$7FFF_H$ **GPIO2_PUDEN** = 4000_H **GPIO2_DRIVE1_CFG** = $7FFF_H$
1	Link Single color or dual color	Activity Blinking depends on Packet Rate Single color or dual color	GPIO (Except LED42 still used for LED)	**GPIO2_ALTSEL0**=$43FF_H$ **GPIO2_PUDEN** = $7C00_H$ **GPIO2_DRIVE1_CFG** = $03FF_H$

Table 12 LED Status VS LED Mode (cont'd)

LED Mode	LEDx0	LEDx1	LEDx2	Configuration
2	Link Activity Blinking frequency: 4 Hz Single color or dual color	100 Mbps Single Color or Dual color	1000 Mbps Single color or dual color	**GPIO2_ALTSEL0**=$7FFF_H$ **GPIO2_PUDEN** = 4000_H **GPIO2_DRIVE1_CFG** = $7FFF_H$
3	10 Mbps or 100 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	1000 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	GPIO (Except LED42 still used for LED)	**GPIO2_ALTSEL0**=$43FF_H$ **GPIO2_PUDEN** = $7C00_H$ **GPIO2_DRIVE1_CFG** = $03FF_H$

EEPROM Detection Procedure (PS_NOWAIT = 1_B)

Boot loader configures the registers in the same way as Self-start mode procedure first (as shown in **Self-start Mode Procedure (PS_NOWAIT = 1_B)**. After that, SPI master uses default low speed clock and 24-bit address mode to start. It uses SPI master manual mode and start to read the first six addresses of EEPROM. If the value in **MSPI_DIN23** = $010101XX010101XX_B$, then most likely valid flash is attached. The address mode (**ADDRMD** in MSPI_CFG) is set to the lower 2 bits of **MSPI_DIN23**. After that, with the new addressing mode, read address 6 and 7 of the EEPROM. If the value of the address 6 is 10101010_B, then it is confirmed that the flash is detected. Configure SPI master clock frequency (**CLKDIV** in **MSPI_CFG**) to the value in the address 7 of the EEPROM. Finally the configuration in EEPROM is executed by boot loader.

EEPROM Applications

Connecting an external EEPROM is intentionally used to enable customers implementing systems without any management entity or STA. In such a system there is no STA driving the management interface and thus neither control nor configuration information is transferred as such. Also it is not possible to configure all functionality of the Ethernet Switch solely using the pin-strapping interface. In such applications the external EEPROM provides a low cost and efficient solution to store the whole configuration information that needs to be loaded by the Intel® Ethernet Switch during startup.

The Intel® Ethernet Switch supports EEPROM devices by means of SPI master interface.

In the simplest application the EEPROM is only used to store the configuration information of the Intel® Ethernet Switch. This configuration is loaded by the Ethernet Switch directly after reset or power-up if an EEPROM has been detected.

EEPROM Content

EEPROM contents include EEPROM type record and configuration content records shown in **Table 20**.

The start address for EEPROM type record is 0. There are 8 bytes in EEPROM type record. The format of EEPROM type record is shown in **Table 13**.

The start address for EEPROM configuration content record is 8.

The overall EEPROM content format is show in **Table 20**.

Table 14 to **Table 19** defines configuration content record. It consists of multiple access blocks. For each access block, there are the following elements:

- Number of Configuration Entries. If it is 0, then this is the last access block and no valid configuration for the last access block. If it is non-0, it represents the number of configuration entries in the current access block.
- Access Type
  - If it is 0000_H, then the current access type is incremental access type. Only the address for the first access entry is stored in the EEPROM. Please refer to **Table 14**.
  - If it is $FFFF_H$, then the current access type is single access without write enable type. The address for each access entry is stored in the EEPROM. Please refer to **Table 15**.
  - If it is 6666_H, then the current access type is single access with write enable type. The address and the write enable for each access entry is stored in the EEPROM. This requires read-modify-write operation for each access entry. Please refer to **Table 16**.
  - If it is 9999_H, then the current access type is “run self-start mode configuration”. The configuration is listed in **Self-start Mode Procedure (PS_NOWAIT = 1_B)**. Please refer to **Table 17**.
  - If it is 5555_H, then the current access type is wait until true access. Boot loader polls a 16-bit register until its value after mask matches with the expected data. Please refer to **Table 18**.
  - If it is $AAAA_H$, then the current access type is conditional jump access. Boot load reads a 16-bit register, if its value after mask matches with the expected data, boot loader jumps to a new location. The new location’s relative offset to the current address is programmable in the block. Please refer to **Table 19**,
- Optional: 16-bit Bus Address
- Single or Multiple 16-bit Data to be written or read
- Optional: 16-bit mask for read or enable for write
- Optional: The offset of the next address from the current address

Table 13 EEPROM Type Record

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	1	EEPROM Address Mode		Identify EEPROM and EEPROM Address Mode EEPROM Address Mode: **Constants** 00_B **9-bit** SPI master interface is in 9-bit address mode. 01_B **16-bit** SPI master interface is in 16/17-bit address mode. 10_B **24-bit** SPI master interface is in 24-bit address mode. 11_B **24H-bit** SPI master interface is in 24-bit high speed address mode.
1	0	1	0	1	0	1	EEPROM Address Mode		
2	0	1	0	1	0	1	EEPROM Address Mode		
3	0	1	0	1	0	1	EEPROM Address Mode		
4	0	1	0	1	0	1	EEPROM Address Mode		
5	0	1	0	1	0	1	EEPROM Address Mode		
6	1	0	1	0	1	0	1	0	Check Value
7	CLKDIV								Master SPI Clock is 62.5 MHz/(CLKDIV+1)

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode

Table 14 Configuration Content Record: Incremental Access Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Incremental Access Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	0	0	0	0	0	0	0	0	0000_H = Incremental Access Type
3	0	0	0	0	0	0	0	0	
4	ADDR(0)[15:8]								PDI Bus Address and Configuration-Data for Entry 0
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	DATA(1)[15:8]								PDI Bus Configuration-Data Word for Entry 1
9	DATA(1)[7:0]								
...	...								...

Table 14 Configuration Content Record: Incremental Access Format (cont'd)

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
6+2*(NOCE-1)	DATA(NOCE-1)[15:8].								PDI Bus Configuration-Data Word for Entry #NOCE -1
7+2*(NOCE-1)	DATA(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 15 Configuration Content Record: Single Access without Write Enable Format

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
Single Access Without Write Enable Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	1	1	1	1	1	1	1	1	$FFFF_H$ = Single Access Without Write Enable Type
3	1	1	1	1	1	1	1	1	
4	ADDR(0)[15:8]								PDI Bus Address and Configuration-Data for Entry 0
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	ADDR(1)[15:8]								PDI Bus Address and Configuration-Data for Entry 1
9	ADDR(1)[7:0]								
10	DATA(1)[15:8]								
11	DATA(1)[7:0]								
...	...								...
4 + 4*(NOCE-1)	ADDR(NOCE-1)[15:8]								PDI Bus Address and Configuration-Data for Entry #NOCE-1
5 + 4*(NOCE-1)	ADDR(NOCE-1)[7:0]								
6 + 4*(NOCE-1)	DATA(NOCE-1)[15:8]								
7 + 4*(NOCE-1)	DATA(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 16 Configuration Content Record: Single Write Access with Write Enable Format

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
Single Access With Write Enable Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	0	1	1	0	0	1	1	0	6666_H = Single Access With Write Enable Type
3	0	1	1	0	0	1	1	0	

Table 16 Configuration Content Record: Single Write Access with Write Enable Format (cont'd)

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
4	ADDR(0)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry 0 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	WE(0)[15:8]								
9	WE(0)[7:0]								
10	ADDR(1)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry 1 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
11	ADDR(1)[7:0]								
12	DATA(1)[15:8]								
13	DATA(1)[7:0]								
14	WE(1)[15:8]								
15	WE(1)[7:0]								
...	...								...
4 + 6*(NOCE-1)	ADDR(NOCE-1)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry #NOCE-1 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
5 + 6*(NOCE-1)	ADDR(NOCE-1)[7:0]								
6 + 6*(NOCE-1)	DATA(NOCE-1)[15:8]								
7 + 6*(NOCE-1)	DATA(NOCE-1)[7:0]								
8 + 6*(NOCE-1)	WE(NOCE-1)[15:8]								
9 + 6*(NOCE-1)	WE(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 17 Configuration Content Record: Run Self-start Mode Configuration Format

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
Run Self Start Mode Configuration Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								
2	1	0	0	1	1	0	0	1	9999_H = Run Self Start Mode Configuration
3	1	0	0	1	1	0	0	1	

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 18 Configuration Content Record: Wait Until True Format

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
Wait Until True Access Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								

Table 18 Configuration Content Record: Wait Until True Format (cont'd)

Address[1]	Content								Comment
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
2	0	1	0	1	0	1	0	1	5555_H = Wait Until True Access
3	0	1	0	1	0	1	0	1	
4	ADDR[15:8]								Register Address
5	ADDR[7:0]								
6	DATA[15:8]								Expected Data
7	DATA[7:0]								
8	MASK[15:8]								Comparison Mask **Constants** 0_B **DIS** Don't Compare. 1_B **EN** Compare.
9	MASK[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 19 Configuration Content Record: Conditional Jump Access Format

Address[1]	Content								Comment
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
Conditional Jump Access Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								
2	1	0	1	0	1	0	1	0	$AAAA_H$ = Conditional Jump Access
3	1	0	1	0	1	0	1	0	
4	ADDR[15:8]								Register Address
5	ADDR[7:0]								
6	DATA[15:8]								Expected Data
7	DATA[7:0]								
8	MASK[15:8]								Comparison Mask **Constants** 0_B **DIS** Don't Compare. 1_B **EN** Compare.
9	MASK[7:0]								
A	OFFSET[15:8]								Next Address = Next EEPROM Address of OFFSET[7:0] + OFFSET[15:0]*2 OFFSET is a signed integer.
B	OFFSET[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 20 EEPROM Content Format

Address Range	Content	Comment
0 to 7	EEPROM Type Record	Identify EEPROM Address Mode and Speed
8 to ...	Configuration Content Record	Boot loader

Pin Strapping

This section describes the configuration of the device by means of pin strapping. As can be seen the pin-strapping functionality shares the LED pins, SPI and TDO signals.

Internal pull up for the pin strapping shall be disabled after reset.

The pin strapping mapping are described below.

All GPIO pins are sampled at the rising edge of HRSTN and stored in registers PS0 and PS1. These two registers can only be reset by hardware reset.

PLL shall be released from reset state some cycles after the rising edge of HRSTN (so that pin strapping occurs and be stable before PLL is released).

Table 21 Functional Mode Pin Strapping

Pin Strap	Description
PS0(3): UTXD	PS_XTAL
PS0(7): MSDO	PS_OP_MD1
PS0(8): MSCK	PS_SUBTYPE_MD3
PS0(9): MSCS	PS_SUBTYPE_MD4
PS1(10): LED02	PS_NOWAIT
PS1(11): LED12	PS_OP_MD0
PS1(12): LED22	PS_SUBTYPE_MD0
PS1(13): LED32	PS_SUBTYPE_MD1
PS1(14): LED42	PS_SUBTYPE_MD2

Table 22 Pin Strapping Description

Pin Strapping Signals	Description
PS_XTAL	**XTAL Frequency** This is to specify the frequency of XTAL. 0_B **40 MHz** 40 MHz 1_B **25 MHz** 25 MHz
PS_NOWAIT	**No Wait for External Master Trigger** This is to specify if boot loader wait for external master to trigger the start. 0_B **WAIT** Boot loader wait for external master to trigger the start of GPHY and GSWIP 1_B **NOWAIT** Boot loader starts GPHY and GSWIP after the initialization is done
PS_OP_MD	**Operation Mode** This is to specify the chip operation mode. 00_B **OPMD0** Reserved. 01_B **OPMD1** Standalone Unmanaged Switch. 10_B **OPMD2** Managed Switch with SPI Slave Interface. 11_B **OPMD3** Managed Switch with MDIO Slave Interface.
PS_SUBTYPE_MD	**SUB Type Mode** Please refer to Table 23.

Table 23 SUBTYPE Mode Configuration

Operation Mode	SUBTYPE Mode
OPMD1: Standalone Unmanaged Switch	PS_SUBTYPE_MD[4:3]: 00_B **MD0** LED Display Mode 0 01_B **MD1** LED Display Mode 1 10_B **MD2** LED Display Mode 2 11_B **MD3** LED Display Mode 3
	PS_SUBTYPE_MD[2]: 0_B **AUTO** Auto-polling to determine RGMII5 link status 1_B **FORCE** Force RGMII5 link speed to 1G, full duplex and on.
	PS_SUBTYPE_MD[1]: 0_B **AUTO** Auto-polling to determine RGMII6 link status 1_B **FORCE** Force RGMII6 link speed to 1G, full duplex and on.
	PS_SUBTYPE_MD[0]: 0_B **DIS** Disable RGMII5 and RGMII6 interface 1_B **EN** Enable RGMII5 and RGMII6 interface
OPMD2: Managed Switch with SPI Slave Interface	PS_SUBTYPE_MD[4]: 0_B **RXDLY0** RGMII Path RX Delay is 0 ns. 1_B **RXDLY2** RGMII Path RX Delay is 2 ns.
	PS_SUBTYPE_MD[3]: 0_B **TXDLY0** RGMII Path TX Delay is 0 ns. 1_B **TXDLY2** RGMII Path TX Delay is 2 ns.
	PS_SUBTYPE_MD[2]: Reserved
	PS_SUBTYPE_MD[1]: SSPI SDI Edge Select 0_B **RISE** Sample at rising edge 1_B **FALL** Sample at falling edge
	PS_SUBTYPE_MD[0] SSPI SDO Edge Select 0_B **RISE** Drive at rising edge 1_B **FALL** Drive at falling edge
OPMD3: Managed Switch with MDIO Slave Interface	PS_SUBTYPE_MD[4]: 0_B **RXDLY0** RGMII Path RX Delay is 0 ns. 1_B **RXDLY2** RGMII Path RX Delay is 2 ns.
	PS_SUBTYPE_MD[3]: 0_B **TXDLY0** RGMII Path TX Delay is 0 ns. 1_B **TXDLY2** RGMII Path TX Delay is 2 ns.
	PS_SUBTYPE_MD[2]: Reserved
	PS_SUBTYPE_MD[1:0]: 00_B **0** SMDIO Address is 0. 01_B **4** SMDIO Address is 4. 10_B **16** SMDIO Address is 16. 11_B **31** SMDIO Address is 31.

3.2.8 Packet Insertion and Extraction

An external controller can insert and extract the packets to/from the switch via port 6 of Ethernet switch. When packet insertion/extraction mode is enabled (**PIE** = 1_B), switch port 6 is connected to packet insertion/extraction module. This mode allows external CPU to insert/extract management/control packets without using RGMII interface.

In packet insertion/extraction mode, port 6 must be configured to 1000 Mbps, full duplex and pause disable mode. The link ok must be forced on.

For TX direction (packet extraction), when there is a new packet available, an interrupt is asserted. Interrupt status is cleared automatically when an external controller read **PKT_EXT_READ** register. When the AVAIL value is '1', then the data byte in the current read is the first byte of the packet and the data byte in the previous read is the last byte of the previous packet. When TXEN value of the read access is 0_B, then the data byte in the previous read is the last byte of the packet.

An external controller can flush the rest of the packet after reading the packet header in packet extraction direction.

Packet Insertion Programming Sequence

- Write **PKT_INS**:
  - **INSCMD** = 1_B
  - **RXVD** = 0_B or 1_B depending if injecting interframe gap (**RXVD**=0_B) or other types of data (including preamble, SFD and packet data, **RXVD**=1_B).
  - **RXD** = the byte to be written.
- Repeat the above step for all the bytes in a packet (including IPG, Preamble, SFD). At lease one interframe gap shall be inserted so that the MAC can identify the end of packet and the start of the packet. At least one cycle between the two writes to **PKT_INS** shall be met.

Packet Extraction Read Programming Sequence

- Wait for interrupt.
- Read **PKT_EXT_READ** register.
- If **TXEN** is 1_B, then the data byte is valid. If **TXEN** is 0_B, then the data byte is not valid.
- If the previous read **TXEN** = 0_B, the current read **TXEN** = 1_B and the current read **AVAIL** = 1_B, then current read data byte is the first byte of the packet (including preamble and SFD).
- If the previous read **TXEN** = 1_B and the current read **TXEN** = 0_B or current read **AVAIL** = 1_B, then the previous read data byte is the last byte of the packet.
- Repeat reading until **TXEN** = 0_B or current read **AVAIL** = 1_B (EOP or SOP is detected). At lease one cycle between the read reads to **PKT_EXT_READ** shall be met.

Packet Extraction Flush Programming Sequence

- Write **PKT_EXT_CMD** to issue flush command (**FLUSH** = 1_B).
- Wait for interrupt and check if **AVAIL** in **PKT_EXT_CMD** is set for the next new packet.

3.3 LED Controller Function Description

3.3.1 LED

LED pin 10, 20, 30 and 40 are multiplexed with JTAG interface. When TRSTN = ‘0’, these 4 pins are used for GPIO/LED pins. When TRSTN = ‘1’, these 4 pins are used for JTAG interface.

3.3.2 LED Display

Each GPHY has 3 LEDs. The 3rd LED are used for pin strapping in the boot loader. All of them can be used as single color LED or dual color LED. If dual color LED is required in system, it is recommended to use the 3rd LED as one of the dual color LED to ease the pin strapping circuit. The 3rd LED are used for pin strapping in the Boot ROM code.

Power LED is always in single color mode and multiplexed with GPIO pin. The value of power LED is directly configurable via GPIO output register.

For each LED in single color mode, it can choose to either connecting external LED to ground or connecting external LED to power as showing **Figure 11**. It is configurable per LED to one of the mode via **LED_MD_CFG**. For dual color LED, the corresponding field must be set to 0_B. If LED is configured to “power” mode, then internal LED signal is inverted before feeding to the LED PAD. If LED is configured to “power” mode, both push-pull and open drain mode are supported via GPIO programming registers.

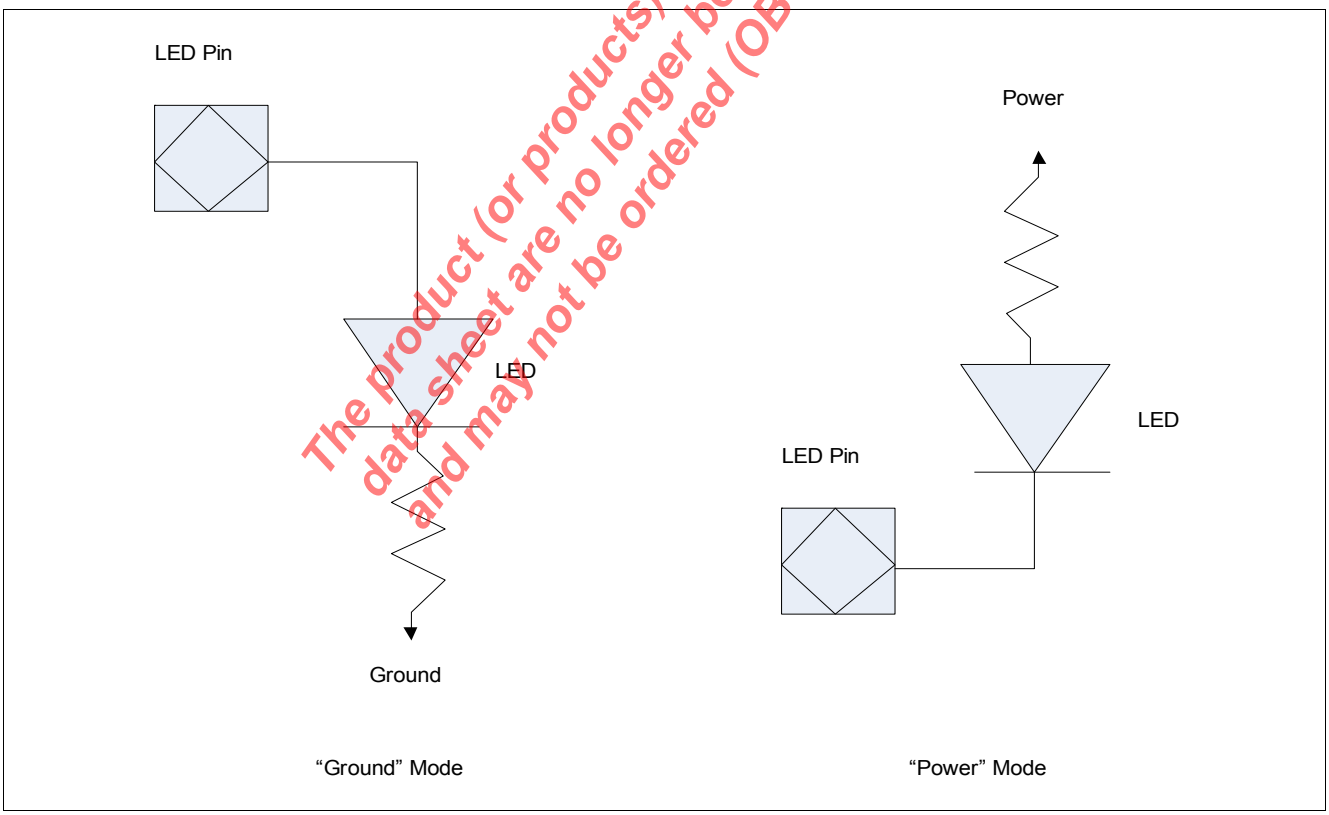


Figure 11 LED Display Mode

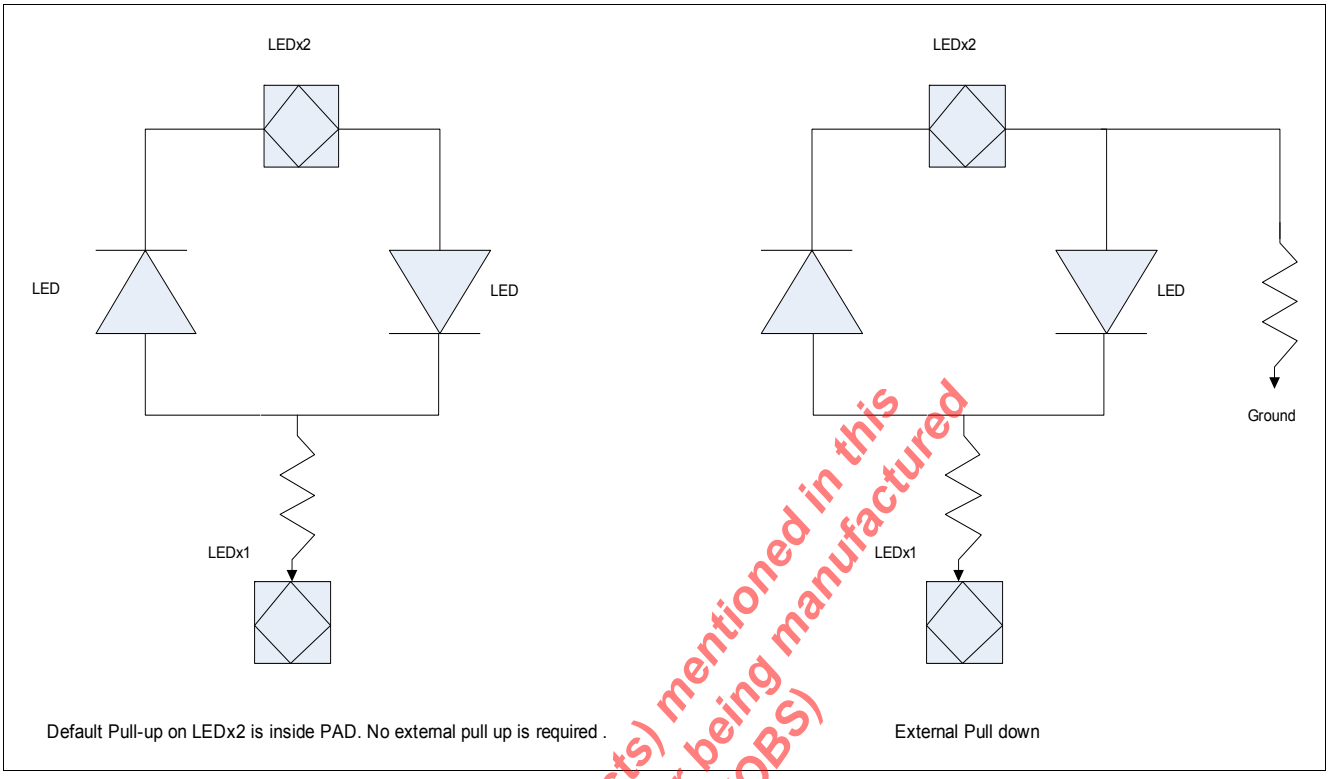


Figure 12 Pin Strapping on Dual Color LED

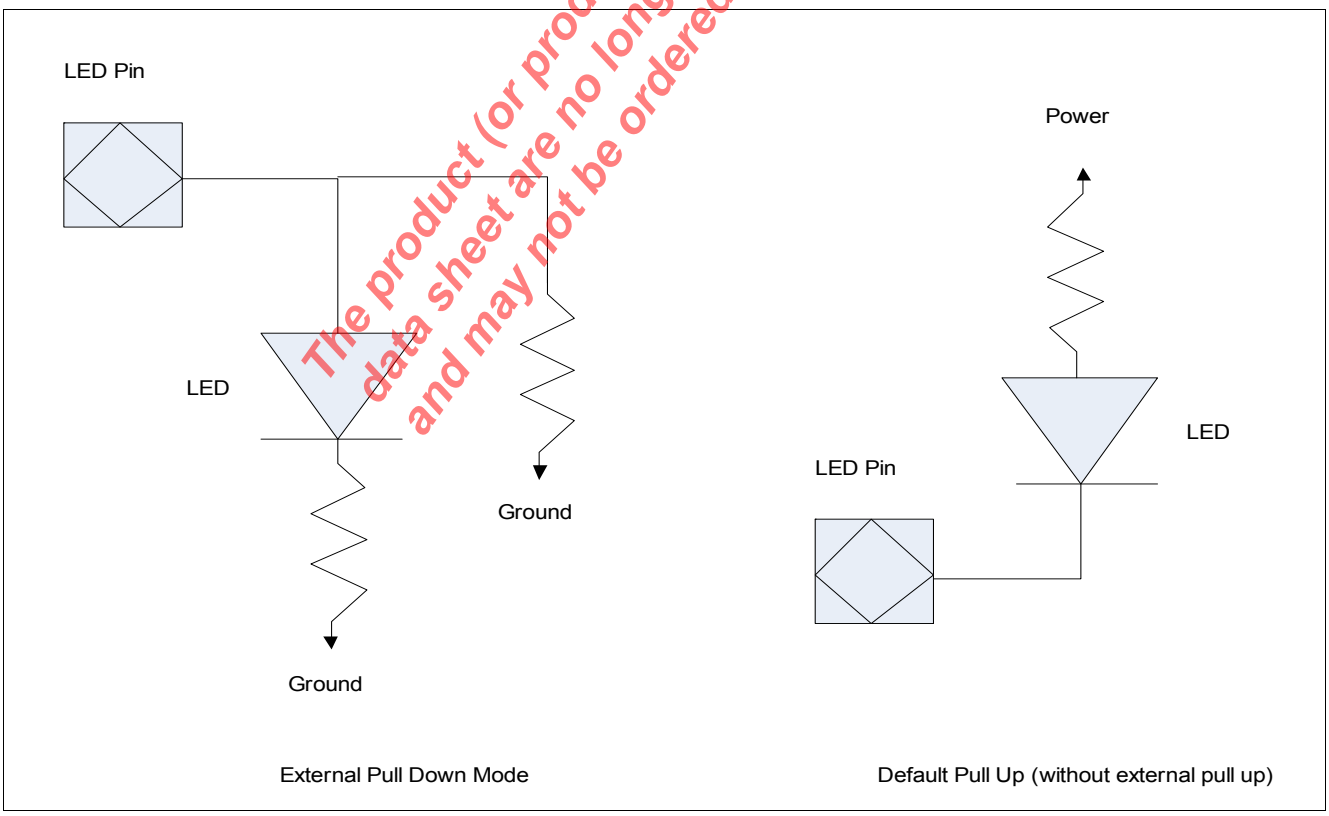


Figure 13 Pin Strapping on Single Color LED

3.3.3 LED Brightness Control

There are two brightness control mode. Either one of them can be used. The selection is determined by board design. They shall not be used simultaneously.

- 2 Level Brightness Switch Mode
- 16 Level Light Sensor Control Mode

Brightness Control

This block controls the brightness of the LED by way of controlling the time duration the LED is ON/OFF, and due to persistence of the eye, LED brightness will be perceived. When LED is off, the output is disabled. When LED is on, the output is enabled. Brightness control controls the LED output enable directly.

As show in **Figure 14**, brightness control frequency is 100 Hz. Each period is divided into 64 slots. LED brightness control is enabled/disabled via **LED_BRT_CTRL.EN**.

When LED brightness control is disabled, LED is enabled in all 64 slots.

When LED brightness control is enabled, LED is enabled for consecutive n slots. n is determined by brightness level configured. LED output is disabled in the 64th slot. LED42 pin is in input mode during 64th slot and used to detect the rising/falling edge of external brightness switch input.

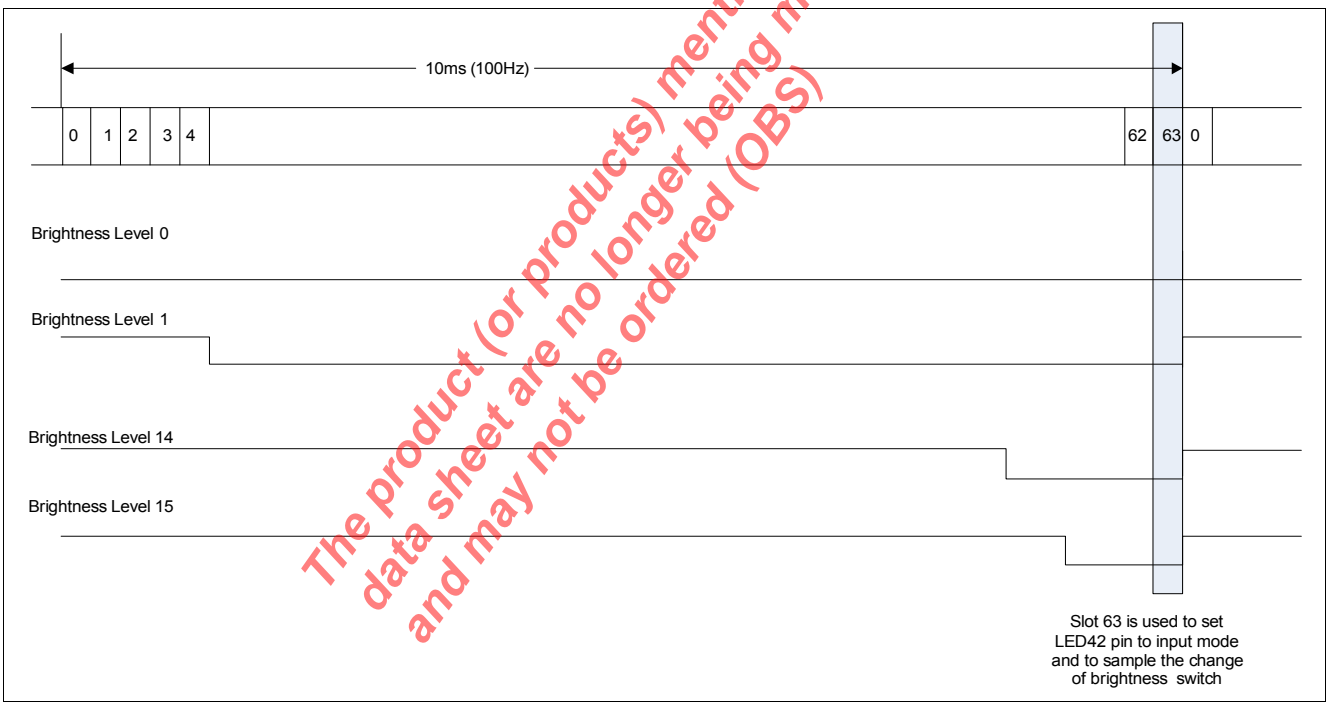


Figure 14 LED Brightness Control By Controlling LED Output Enable/Disable

2 Level Brightness Switch Mode

LED42 pin is sampled at slot 63 to detect the toggling. The LED brightness is switched between two configurable brightness level (**LED_BRT_CTRL.MAXLEVEL**, **LED_BRT_CTRL.MINLEVEL**)

This can be enabled/disabled via **LED_BRT_CTRL.2SEWN**. When 2 level brightness switch mode is disabled, the brightness level is configured via **LED_BRT_CTRL.MAXLEVEL**.

The spike on LED42 pin is filtered. Only when the value are stable for two consecutive sample after a change, the edge is considered as detected. The brightness shall start with **LED_BRT_CTRL.MAXLEVEL**. If LED42 pin is pulled up at pin strapping, then the falling edge of the sampling triggers the brightness toggle. If LED42 pin is pulled down, then the rising edge of the sampling triggers the brightness level toggle. The falling edge or rising edge trigger is selected via **LED_BRT_CTRL.EDGE**.

If 2 level brightness switch control is disabled on system board, LED42 pin is either pull up or pull down externally (depending on pin strap option) to allow there is a constant, untoggled level on LED42 during the sample slot.

If 2 level LED brightness switch control is enabled on system board, then an external recess switch is required to connect to LED42 pin.

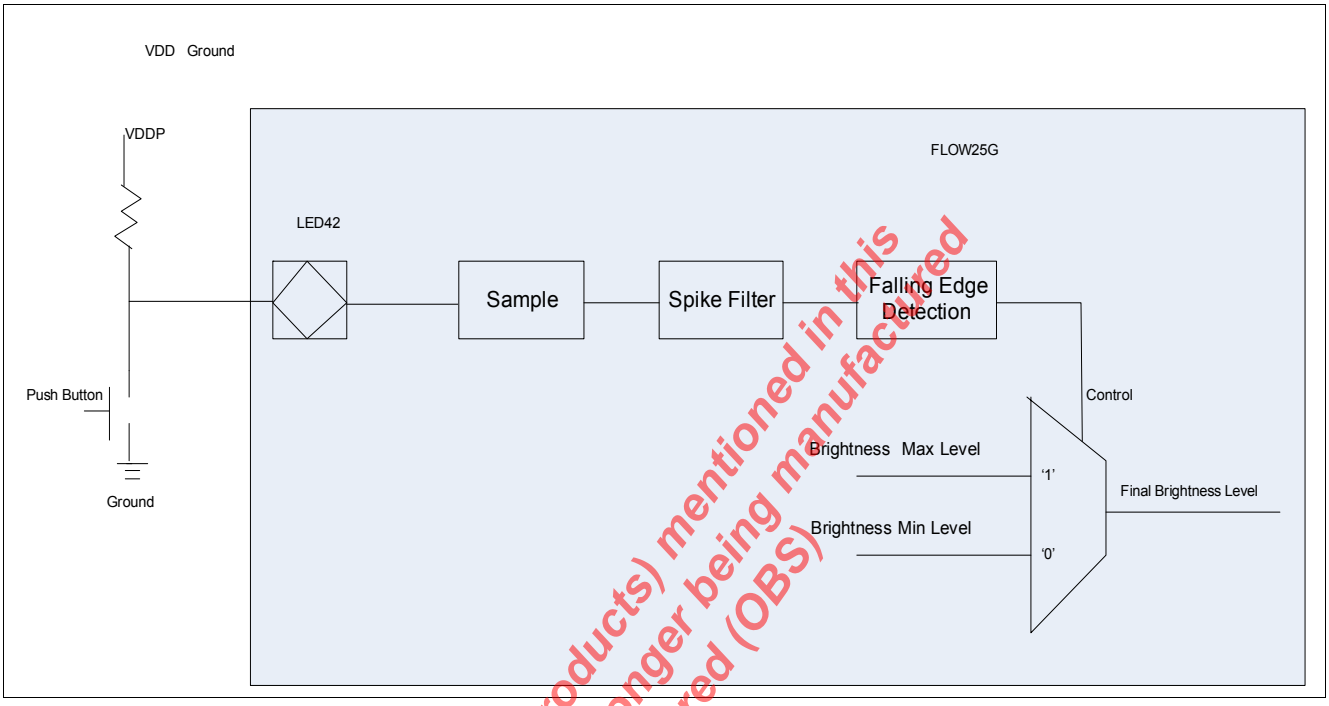


Figure 15 Direct 2 Level LED Control Enable on System Board (with Pull-Up)

16 Level Light Sensor Control Mode

In this mode the brightness of LED dynamically varies depending on the intensity of the light. The intensity of light is measured by light sensor. This approach would use a constant current source (Visible Light Detector) and capacitor. The time it takes for capacitor to charge to given threshold voltage would be linearly proportional to charging current. And current is proportional to LUX value. One of GPIO pin is used for this purpose.

The sensing is repeated periodically. The period of the sensoring is programmable via **LED_LSENS_CTRL.PERIOD**. For each period, there are 256 slots. The first few slots are for discharging circuit. The number of slots for discharging is configurable via **LED_LSENS_CTRL.TD**. After the discharging, the rising edge of the GPIO pin is detected. The number of slots from the end of discharging to the slot when the rising edge is detected (t - td) is used to determine the light condition. There are 16 level of light condition, this 16 level light condition is converted to a 16-bit brightness level. Only when the difference between the sensed brightness level and the current brightness level is more than 1 (exception is when sensed brightness level is 1 and 15), the brightness is adjusted. Only 1 brightness level (+/-) can be adjusted from the current value. The brightness level must be within the range configured within **LED_BRT_CTRL.MINLEVEL**, **LED_BRT_CTRL.MAXLEVEL**

When both **LED_BRT_CTRL.2SEWN** and **LED_LSENS_CTRL.SENS** are enabled, the final brightness level is the smaller value of the value determined by sensoring logic and by the 2 Level LED switch logic.

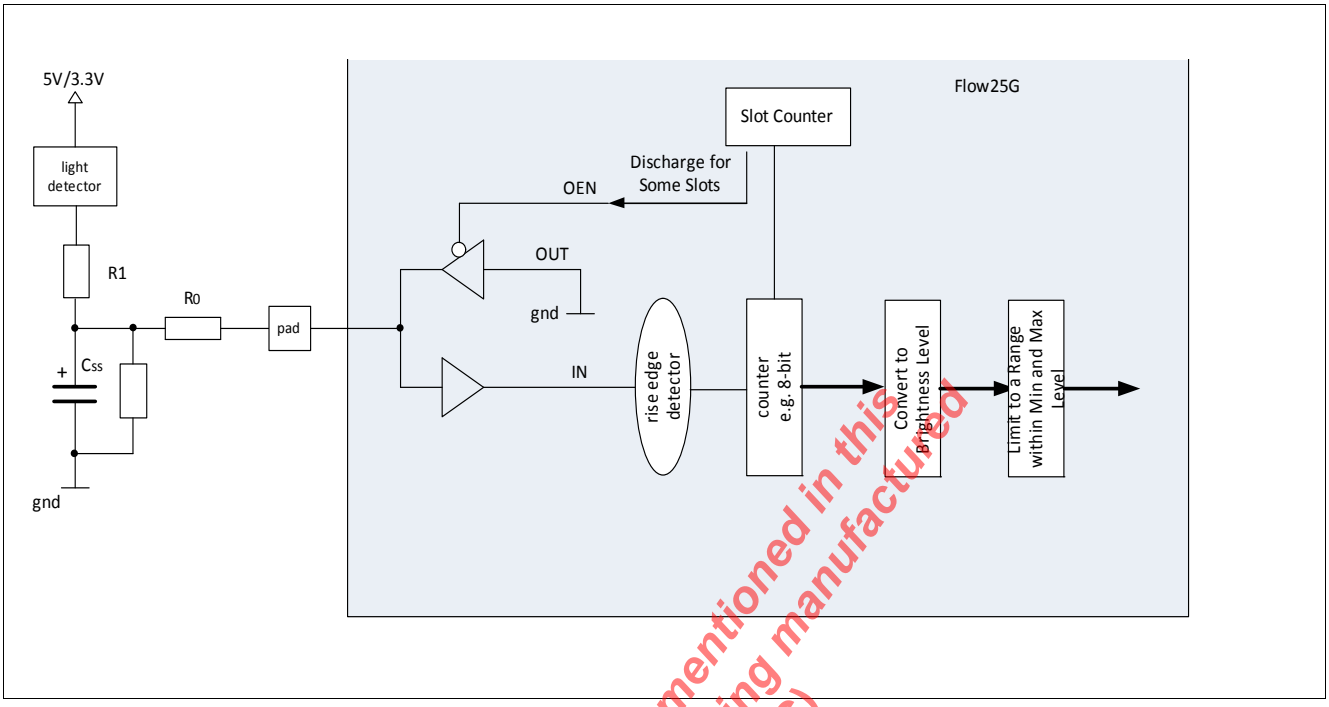


Figure 16 Light Sensing System

3.4 General Purpose Input Output Function Description

Figure 17 shows a general block diagram of a GPIO pin. Each GPIO pin is equipped with a number of control and data bits, enabling very flexible usage of the line.

Each GPIO pin can be configured for input or output operation. In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via the read only register GPIO_IN. In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. Switching between input and output mode is accomplished through the GPIO_DIR register, which enables or disables the output driver.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used as general purpose output, the multiplexer is switched by software to the Output Data Register GPIO_OUT. Software can set or clear the bit in GPIO_OUT, and therefore it can directly influence the state of the port pin. If the on-chip peripheral units use the pin for output signals, alternate output lines can be switched via the multiplexer to the output driver circuitry.

Latch GPIO_IN is provided for input functions of the on-chip peripheral units. Its input is connected to the output of the input Schmitt-Trigger. Further, an input signal can be connected directly to the various inputs of the peripheral units (AltDataIn). The function of the input line from the pin to the input latch GPIO_IN and to AltDataIn is independent of the port pin operates as input or output. This means that when the port is in output mode, the level of the pin can be read by software via latch GPIO_IN or a peripheral can use the pin level as an input. This offers additional advantages in an application.

- Each GPIO pin can also be programmed to activate an internal weak pull-up or pull-down device. Register GPIO_PUDSEL selects whether a pull-up or the pull-down device is activated while register GPIO_PUDEN enables or disables the pull devices.
- The data written to the output register GPIO_OUT by software can be used as input data to an on-chip peripheral. This enables, for example, peripheral tests via software without external circuitry. Examples for this can be the triggering of a timer count input, generating an external interrupt, or simulating the incoming serial data stream to a serial port receive input via software.

- When the pin is used as an output, the actual logic level at the pin can be examined through reading latch GPIO_IN and compared against the applied output level (either applied through software via the output register GPIO_OUT, or via an alternate output function of a peripheral). This can be used to detect some electrical failures at the pin caused through external circuitry. In addition, software supported arbitration schemes can be implemented in this way using the open-drain configuration and an external wired-And circuitry. Collisions on the external communication lines can be detected when a logic 1 is output, but a logic 0 is seen when reading the pin value via the input latch GPIO_IN.
- The output data from a peripheral applied to the pin via an alternate output function can be read through software or can be used by the same or another peripheral as input data. This enables testing of peripheral functions or provides additional connections between on-chip peripherals via the same pin without external wires.

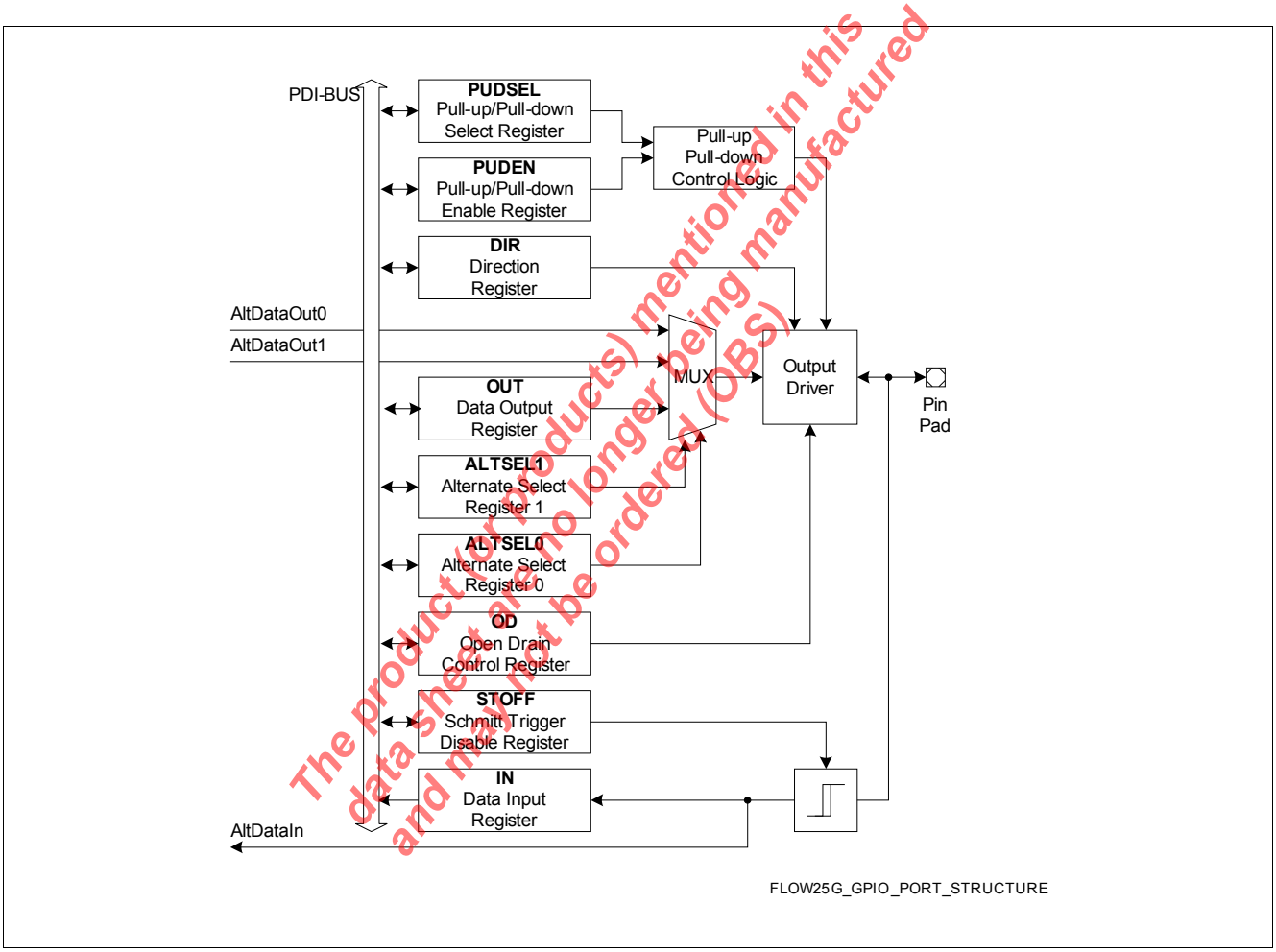


Figure 17 General Port Structure

GPIO pins share with other alternative functions as show in GPIO pins share with other alternative functions as show in **Table 5** and **Table 6**.

3.5 External Interrupt Description

3.5.1 Features

- 2 External Interrupt Pins
  - Share with GPIO functions
  - Programmable open drain or pull-pull mode
  - Programmable pull up or pull down
  - Programmable polarity mode (active low or active high)

3.5.2 Interrupt Controller Functionality

Figure 17 shows a general block interrupt controller diagram. An interrupt module (IM) provides connectivity for multiple interrupt request lines, condensed to two interrupt request lines to external pins.

Interrupt Request

Each interrupt module (IM) provides up to multiple interrupt request inputs, where the interrupt request lines IM_IRL from several peripheral Interrupt Nodes (IRN) are attached to. A high level on an interrupt request line IM_IRL causes the associated interrupt request flag IM_ISR.IRx to be set. Interrupt status register is readable. Writing ‘1’ to interrupt status registers clear the corresponding bit in IM_ISR.IRx.

Interrupt Request Enable Function

For each condensed interrupt request, there are separate request enable registers.

- IM_EINT0_IER register
- IM_EINT1_IER register

All outputs of the enabled interrupt status are logically or’ed and feed to the corresponding interrupt controller.

Interrupt Output Polarity

External Interrupt request outputs can be programmed to active high or active low.

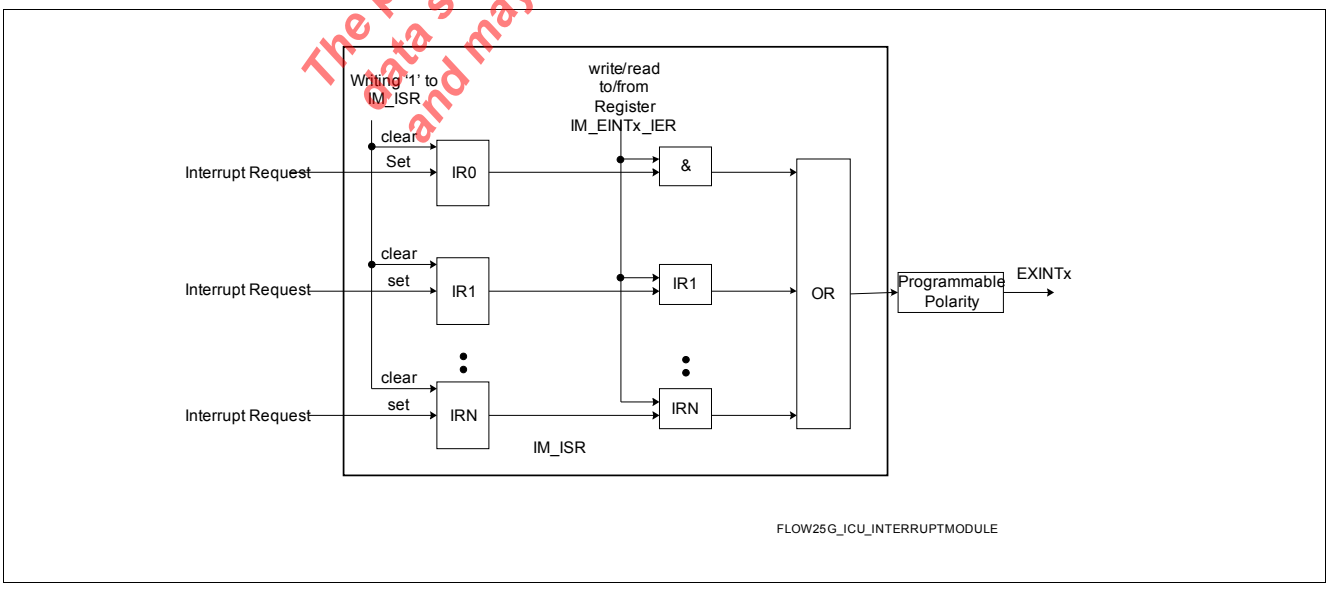


Figure 18 Interrupt Controller Block Diagram

3.6 Gigabit Ethernet PHY Functional Description

3.6.1 Features

- Supports Energy-Efficient Ethernet (EEE):
  - 10BASE-Te
  - 100BASE-TX
  - 1000BASE-T
  - Power Down modes
  - Wake-on-LAN support
  - Integrated termination resistors
  - Supports transformerless Ethernet (TLE) for backplane applications
  - Low-EMI voltage mode line-driver
- Auto-negotiation with next-page support
- Auto-downspeed
- Auto-MDI/MDIX and Polarity selection
- Test Loops
- Cable diagnostics:
  - Cable open/short detection
  - Cable length estimation

3.6.2 Functional Description

3.6.2.1 Twisted-Pair Interface

The Twisted-Pair Interface (TPI) of the GPHY IP is fully compliant with IEEE 802.3. To reduce PCB costs, the series resistors that are required to terminate the twisted-pair link to nominally 100 Ω are integrated into the device.

As a consequence, the TPI pins can be directly connected via the transformer to the RJ45 plug. Additional external circuitry is only required for proper common-mode termination and rejection. A high-level schematic of the TPI circuitry is shown in **Figure 19**, taking these components into account.

GPHY IP supports normal operation with transformers whose center-taps on the chip side are shorted and connected to capacitors.

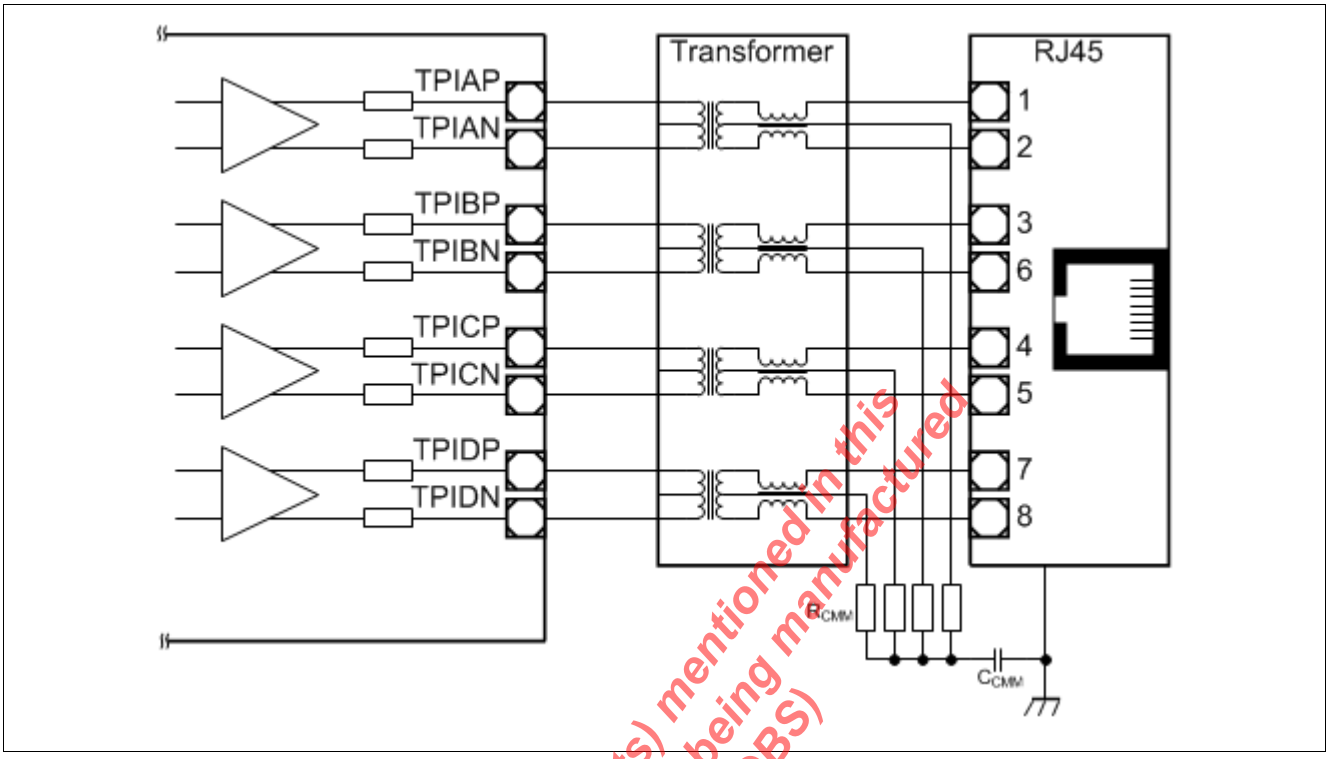


Figure 19 Twisted-Pair Interface of GPHY IP Including Transformer and RJ45 Plug

3.6.2.2 Auto-Negotiation (ANEG)

The GPHY IP supports Auto-Negotiation (ANEG) as a startup procedure to exchange capability information with the link partner.

Unless ANEG is manually disabled, the GPHY IP will initiate each link-up using an ANEG procedure according to IEEE 802.3-2008 Clause 28 and essentially required for the 1000BASE-T mode in IEEE 802.3-2008 Clause 40.

Unless otherwise configured, the GPHY IP carries out an auto-crossover detect/enable procedure prior to the start of the ANEG process. This ensures optimal interoperability even in inadequate cable infrastructure environments. However, if ANEG is disabled, the auto-crossover procedure is still done during link-up.

The implementation of the ANEG procedure is compliant with the standards given in IEEE 802.3-2008, clause 28. If the link partner does not support ANEG, the GPHY IP extracts the link-speed configuration using **parallel detection**.

The GPHY IP supports Next Page (NP) exchange, since this is mandatory for advertising 1000BASE-T capabilities. By default, NPs are exchanged autonomously and do not require interaction with any management device.

3.6.2.3 Auto-Downspeed

The Auto-Downspeed (ADS) feature ensures maximum interoperability even in harsh or inadequate cable infrastructure environments. In particular, ADS is applied during 1000BASE-T training. This is necessary because the information available about the cabling during ANEG is insufficient. It is possible to advertise 1000BASE-T during ANEG, even though it might happen that both link partners are connected via a CAT-3 cable, which does not support the 4-pair Gigabit Ethernet mode.

In order to avoid continuous link-up failures in such a situation, the GPHY IP operates a detection algorithm to identify this situation. As a consequence, Gigabit-capability indication is cleared from the ANEG registers. After the resulting link-down, the next ANEG process does not advertise 1000BASE-T anymore, such that even when

the link partner does not implement this kind of ADS algorithm, the next link-up will be done at the next advertised speed below 1000 Mbit/s.

It can also happen that the existing cable infrastructure is adequate, but that the integrity of received signals is not suitable for a 1000BASE-T link-up, for example due to increased alien noise, or over-length cables. If such a condition is detected, the GPHY IP also does an ADS procedure.

Finally, it can also happen that, even though the GPHY IP is able to link up properly, for example in slave mode, the link partner is not able to. In this situation, ADS criterion described previously does not become active, but the link also never comes up. In order to address this corner situation, the GPHY IP counts the number of attempts to link up to 1000BASE-T. If this number is greater than 3, the ADS procedure is carried out. This number is reset internally after each successful 1000BASE-T link-up.

In all flow and mode settings that support only speeds of 1000 Mbit/s, the ADS feature is automatically disabled.

The number of times GPHY IP decide to downspeed the link is counted and available as statistics via the MDIO.PHY.ERRCNT register.

3.6.2.4 Auto-Crossover and Polarity-Reversal Correction

In order to maximize interoperability even in inadequate wiring environments, the GPHY IP supports auto-crossover and polarity-reversal detection and correction. Both features are enabled by default.

Auto-crossover detection and correction operates at all supported twisted-pair speeds.

In 10BASE-T and 100BASE-TX, pairs C and D are not used. Consequently, mode 2 and 3 as well as 1 and 4 are identical.

In 1000BASE-T all modes are applicable.

The auto-crossover functionality is fully compliant with IEEE 802.3, clause 40.4.4, in 1000BASE-T mode. In the 10BASE-T and 100BASE-TX modes, this functionality depends on the detection of valid link pulses.

Polarity-reversal errors caused by improper wiring are automatically corrected by the GPHY IP. This correction is done on all pairs in the receive direction for all supported twisted-pair media modes. In 10BASE-T mode, the polarity correction is based on the detection of valid link pulses. In 100BASE-TX, the polarity of the receive signal is inherently corrected by the negation invariance of line code. In the 1000BASE-T mode, polarity detection is part of the training sequence. In all the modes, the detected polarity is frozen once the link has been established, and remains unchanged until the link is dropped.

3.6.2.5 Transformerless Ethernet (TLE)

Transformer-Less Ethernet (TLE) is required for back-plane or PICMG applications, where the use of a transformer (magnetics) is not necessarily required in order to fulfill the galvanic-decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of materials and the space requirements on the PCB.

As the GPHY IP incorporates a novel type of voltage-mode line-driver, the only stringent requirement is to use AC coupling. AC coupling can be achieved using simple SMD-type series capacitors, the value of which is selected such that the high-pass characteristics correspond to an equivalent transformer-based standard application (recommended $C_{coupling}$ = 100 nF). The external circuitry for TLE is shown in **Figure 20**. Note that the RJ45 connector is shown only for illustration purposes. Back-plane applications use different connectors.

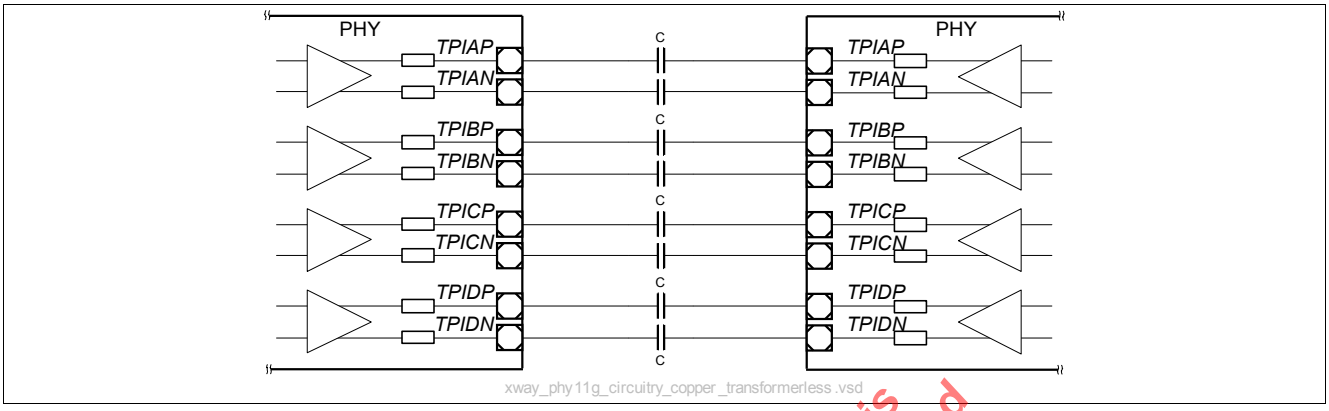


Figure 20 External Circuitry for the Transformerless Ethernet Application

3.6.2.6 Configuration and Control via MDIO

If a higher-level management entity exists in the system, this can configure and control the GPHY IP completely by means of the MDIO interface, according to IEEE 802.3-2008.

3.6.2.7 Power Management

This chapter introduces the power management functions of the GPHY IP.

3.6.2.7.1 Power Down Modes

This section introduces the power-down modes that are supported by the GPHY IP. These modes can be associated to states as depicted in Figure 21. The functionality of each mode and the state transitions are discussed in detail in the subsequent sections.

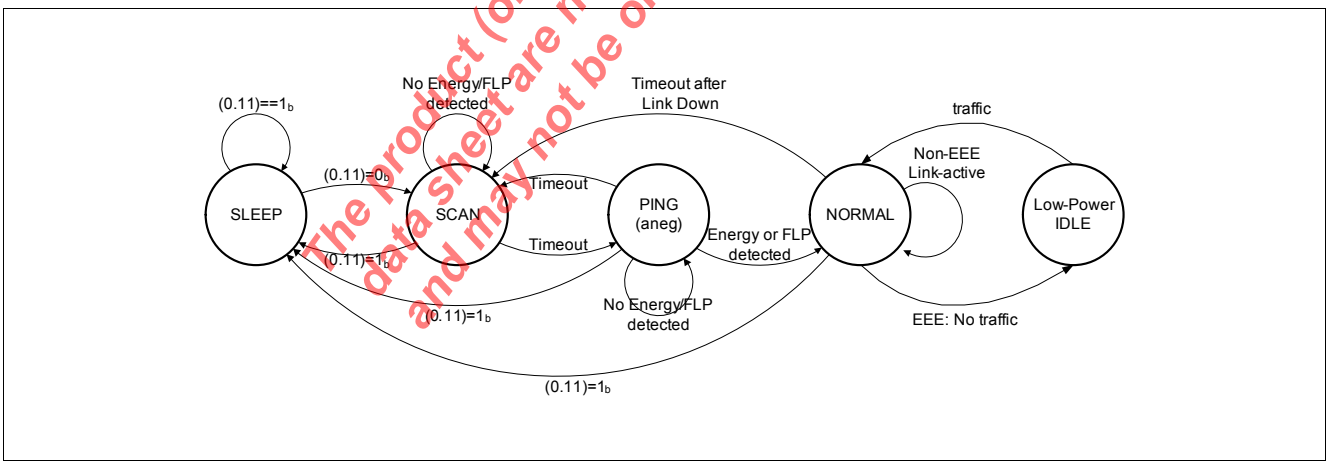


Figure 21 State Diagram for Power-Down Mode Management

3.6.2.7.2 Sleep Mode

The SLEEP mode is entered by setting register (0.11) to logic one, regardless of the current state of the device. Active links are dropped when the PHY is leaving the NORMAL mode. The sleep mode corresponds to power down as specified in IEEE802.3, clause 22.2.4.1.5. The device still reacts to MDIO management transactions. The interface clocks to the MAC are switched off. No signal is transmitted on the MDI.

Since this mode is entered manually, the device will neither wake itself nor any link partner. This functionality can be enabled by setting register (0.11) to logic zero and thus entering the SCAN mode.

3.6.2.7.3 Scan Mode

The SCAN mode differs from the SLEEP mode in that the receiver periodically scans for signal energy or FLP bursts on the media. In this mode, there is no transmission. This shall correspond to the state of “NO-LINK”.

After a certain time-out has expired, the PHY moves into the PING mode. The time-out is randomized between configurable limits to prevent deadlock conditions.

3.6.2.7.4 Ping Mode

The PING mode is similar to the SCAN mode except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the power-down state. This shall correspond to the state of “ANEG”.

After a certain time-out has expired, the PHY moves back into SCAN mode. The time-out is randomized between configurable limits to prevent deadlock conditions.

3.6.2.7.5 Normal Mode

The NORMAL mode is used to establish and maintain a link connection. Once this connection is dropped, the PHY moves back into SCAN mode after a configurable time-out has expired.

3.6.2.7.6 Low-Power Idle Mode: Energy-Efficient Ethernet

The IEEE 802.3az supports Energy-Efficient Ethernet (EEE) operation. The standard is also supported by the GPHY IP. Since the method used for saving energy depends on the PHY speed, this section is divided into 3 subsections corresponding to the various speeds of 10BASE-Te, 100BASE-TX and 1000BASE-T. Except for 10BASE-Te, the general idea of EEE is to save power during periods of low link utilization. Instead of sending an active idle, the transmitters are switched off for a short period of time (20 ms). The link is kept active by means of a frequent refresh cycle initiated by the PHY itself during low power mode. This sequence is repeated until a wake request is generated by one of the link-partners MACs. An EEE-compliant MAC must grant the PHY a time budget of wake time before the first packet is transmitted. The basic principle is shown in **Figure 22**.

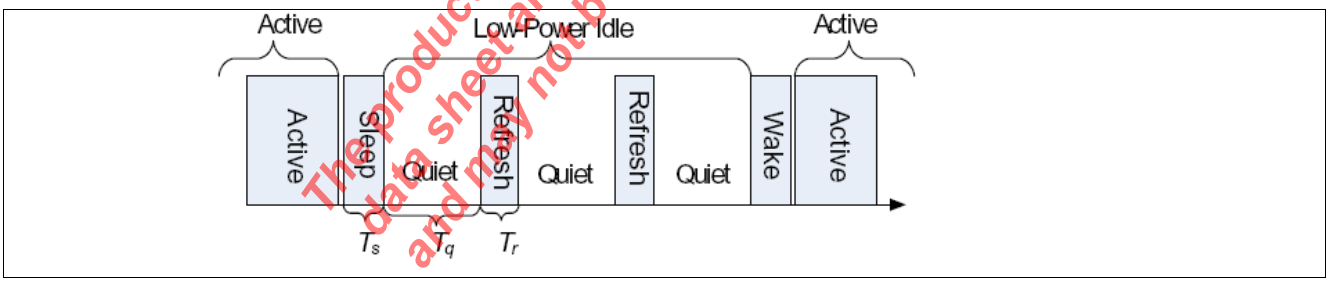


Figure 22 EEE Low-Power Idle Sequence

Auto-Negotiation for EEE Modes

It is imperative that EEE capability is advertised, since, except for 10BASE-Te, a compliant link partner is required. Similarly to 1000BASE-T auto-negotiation, the GPHY IP automatically advertises EEE capability if this is enabled using next pages. EEE capability is stored in the `MMD.ANEG.EEE_AN_ADV` registers. Setting this register to zero disables EEE. After a successful negotiation the link partners’ capabilities are stored in the `MMD.ANEG.EEE_AN_LPADV` register. After a successful auto-negotiation, the GPHY IP performs an auto-resolution on the exchanged capabilities. The result is combined with the speed resolution. Whether or not a link is able to operate EEE is reported in the `MDIO.PHY.MIISTAT.EEE` register.

3.7 Switch Fabric Functional Description

3.7.1 Overview

The Gigabit Ethernet Switch Macro is responsible for classifying, storing and forwarding multiple data flows. The macro consists of storage buffer, packet queuing and packet classification units. Ingress data can be received on one of the port interfaces, classified and placed in the appropriate QoS queue in the Shared Buffer. Ingress policing and access control rules are applied to the received traffic and packets not compliant to the rules are discarded. Prior to packet being fetched from the shared memory and transmitted on one of the egress ports, it is subject to egress scheduling and rate shaping.

Figure 23 describes a typical packet data flow through various stages of switch.

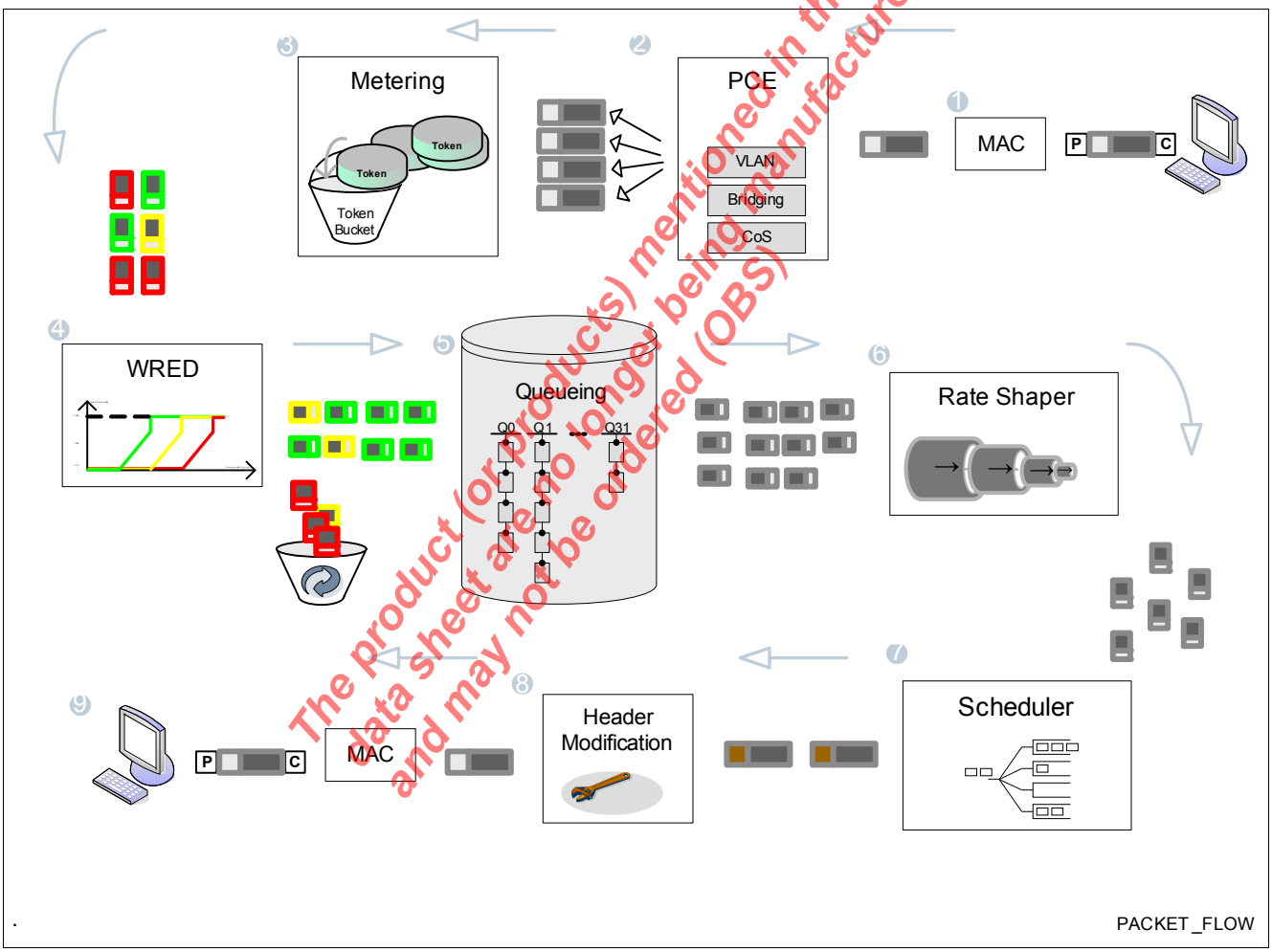


Figure 23 Packet Flow Diagram

Packet received on the ingress port is stripped from the Ethernet Preamble and checked for correct FCS. In case of any reception errors the packet might be discarded. Received packet is classified in the Packet Classification Engine and assigned to an appropriate QoS queue. Prior to accepting the packet to certain queue it is subject to metering and WRED functions. Packets marked as non-conforming by the Metering Engine might be discarded by the WRED algorithm based on the configurable drop precedence. Prior to transmission on the egress side, the packet is subject to Rate Shaping. If transmission of the packet is not delayed by the Rate Shaper it is subject to the Scheduling algorithm (WFQ or SP). Packets that are scheduled for transmission are subject to Header Modification, such as, VLAN Tag modification or DSCP remarking.

3.7.2 Ethernet Bridging

Ethernet bridging (or Switching) is the primary task of the Gigabit Ethernet Switch Macro. Frames which have been received on one of the ingress ports have to be forwarded to the appropriate destination port. The destination port is determined by a lookup in the MAC bridging table. The MAC bridging table can be populated by software (static entries) or entries can automatically be learned by the hardware learning function. Entries which have been learned by the hardware can age out after a configurable time and are deleted from the MAC bridging table.

3.7.2.1 Parsing

The Gigabit Ethernet Switch Macro features a Parser which is realized as a microcoded engine. This allows a flexible adaptation to any future protocol changes. The parser microcode evaluates the frame header and is capable of extracting all relevant information up to the layer 4 protocol from the frame. The microcode has to be loaded otherwise only the MAC destination and MAC source address is extracted from the frame. The parsed fields are:

- MAC source and destination address (also available without loading the parser microcode)
- Special tag
- Ethernet type field
- Service VLAN tag (VLAN ID, DEI/CFI and PCP)
- Customer VLAN Tag (VLAN ID, CFI and PCP)
- PPPoE Session ID (for PPPoE frames)
- DSCP/TOS/Traffic Class (for IPv4/IPv6 packets)
- IP Protocol/Next Header (for IPv4/IPv6 packets)
- IPv4/IPv6 source and destination address (for IPv4/IPv6 packets)
- Application, typically L4 source and destination port (for UDP and TCP)
- Flags (IP version, WOL Packet Flag, Parser Error Flag, Length Encapsulated Packet Flag, IP Short Option Flag, IP Long Option Flag)

A packet is also parsed if it was received encapsulated in a PPPoE frame. The parsing considers Zero or One Service tag, any number of Customer VLAN tags and any number of extension headers, the parsing continues as long as the parsing depth (256 bytes) is not exceeded. If Ethernet type field is not IPv4, IPv6 or PPPoE and IP protocol/next header is not UDP or TCP, the parsing is finished and the next four bytes are stored as application field. This allows to set up rules for unknown protocols.

Note:

1. *Outer customer VLAN tag is extracted by locking the register after the first customer VLAN tag was detected, following customer VLAN tags can not overwrite the value.*
2. *Parsing not continued for length encapsulated frames.*

3.7.2.2 MAC Bridging Table

The MAC bridging table is realized as a hash table with four collision buckets and holds the lookup key (MAC address, FID), control information (static indication, aging timer, “changed” indication) and the result (port or port map, MAC VLAN ID). A port map is a bitmap where each bit represents a single port. The port map allows to send the frame to multiple destination ports and is available for static entries only.

The Gigabit Ethernet Switch Macro supports shared and independent VLAN learning (SVL or IVL). This is achieved by mapping the default Customer VLAN ID or a Flow to a forwarding identifier (FID) which is used as part of the lookup key, together with the MAC address, for the MAC bridging table lookup. By default the FID is zero and all entries belong to shared VLAN learning. Please refer to **Shared/Independent VLAN Learning**for more details regarding VLAN learning modes.

The Gigabit Ethernet Switch Macro supports MAC based VLAN. The idea is to provide, for example, the possibility to extend the number of interfaces behind the same physical Ethernet port. MAC VLAN ID represents a single sub-

interface or a group of sub-interfaces behind a port. This is achieved by learning MAC VLAN ID (shortened as “MVID” in this document) together with port ID. MAC VLAN ID is carried via Service VLAN Tag.

Entries can be entered automatically by hardware (dynamic MAC address learning, described in **Chapter 3.7.2.4**) and can also be entered by software via “manual learning”. Typically the software writes static entries into the MAC bridge table but it is also possible to write dynamic entries which are subject to aging.

The MAC bridge table can hold unicast, multicast or broadcast addresses. Table entries containing multiple egress ports as a destination, can be entered only as static entries, by appropriate management action.

The MAC table can be accessed by software to read out static or dynamically learned entries and optionally modify them. Following MAC table access modes are supported. For each access, a 12-bit MAC table pointer is returned.

- By KEY: MAC address and FID.
- By a 12-bit MAC table pointer
- By reading next valid entry
- By reading next “changed” entry. The “changed” entry is the entry which is added, updated or removed (invalidated) after the last read.

Note: Due to the 4-bucket hash architecture of the table, certain MAC addresses might be rejected while others can still be added.

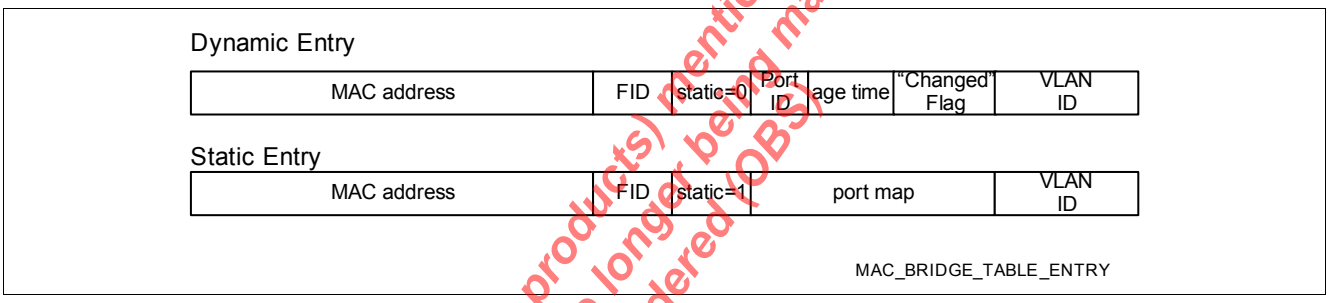


Figure 24 MAC Bridge Table Entry Formats

Bridging Table Flushing

If all learned entries shall be removed, the complete MAC bridging table can be cleared by hardware automatically, with the help of an automated “flushing” function. This function removes all entries, static as well as dynamic ones. Flush function can be triggered by writing 1_B to MTFL bit in PCE_PCTRL_0.

3.7.2.3 MAC Based Forwarding

For each frame the MAC destination address and the FID form a lookup key which is used to determine the destination port (or port map) and MAC VLAN ID. The lookup key is hashed and the hash index is used to address the MAC bridging table and read out the contents of the four buckets. The result of the lookup is an egress port (or multiple ports in case of a multicast entry) and MAC VLAN ID. In case the egress port or port map is programmed to all-zero, the frame is discarded.

Default Forwarding

If no match for the destination MAC address + FID pair was found in the Bridging table, the default port map is used. A default port map can be configured for L2 unicast (via PCE_PMAP_3) and L2 multicast/broadcast (via PCE_PMAP_2) addresses separately. After reset unknown destinations are flooded to all egress ports. MAC VLAN ID is “NULL” (all 0) for unknown unicast, unknown multicast and broadcast.

3.7.2.4 Dynamic Source MAC Address Learning and Aging

The MAC bridging table can be populated automatically if learning is enabled on the ingress port. The lookup key (concatenation of the source MAC address and the FID) is hashed and the index is used to address the MAC bridging table.

Dynamic learning operates in the following way:

- **Match Found:** If the entry was found and if the PortID+MVID association with SA+FID is unchanged, the aging timer of the entry is refreshed. If the entry contains a different port number or different MVID, old PortID + MVID in the entry is replaced by the new PortID+MVID. Note: Static entries will not be modified by dynamic learning function. If the matched entry is static, the association is not changed.
- **No Match - Table not full:** If SA+FID pair could not be found in any of the collision buckets and there is an empty bucket for this hash index, the lookup key together with PortID+MVID pair are stored and the aging timer is refreshed.
- **No Match - Table full:** If SA+FID pair could not be found and there are no available entries (i.e. all collision buckets are full) and LRU mode (Least Recently Used) of the switch is enabled, the oldest entry (lowest age time) will be replaced by the new lookup key and new PortID+MVID pair. If LRU mode is disabled, no entry will be overwritten and the source MAC address will not be learned.
- **No Match - All static:** If SA+FID pair could not be found and all the collision buckets for this hash index are occupied by static entries, no entry will be overwritten and the source MAC address will not be learned.

Dynamic learning of SA+FID pair can be performed only if all of the following conditions are fulfilled.

- Source MAC address is a Unicast address.
- Learning is enabled on the ingress port.
- The frame discarded by the filtering function is not due to ingress reasons (e.g., VLAN filtering, Flow Classification filtering).
  - See Flow Classification chapter for details.
- Bridging table is not full or table is full but overwriting existing entry is allowed.
- Number of entries for the port does not exceed the learning limit if MAC learning limitation is enabled (see **MAC Learning Limitation**)
- Ingress PortID+MVID is identical to the stored PortID+MVID pair in the MAC bridge table if stored port MAC port locking is not enabled and the receiving port MAC spoofing is not disabled (see **MAC Port Locking and MAC Port Spoofing Detection**)

If a packet's SA+FID pair is new or its association with PortID+MVID pair is changed, the packet can be mirrored to the monitoring port. This feature can be switched on or off (default) via configuration (VIO_9 bit in PCE_PCTRL_3) per ingress port.

MAC Address Aging

To avoid table overflow over time, the entries that have been learned need to be removed once they have not been used for a certain amount of time. This functionality is covered by the aging process, which removes bridging table entries after a configurable time of inactivity (age time). The range of the age time reaches from 1 s up to more than 24 hours. A typical value of 300 s is used as a default. Static entries do not age out, they have to be deleted by software. The aging can be enabled or disabled per ingress port. When disabled, addresses learned from this port will not be aged out.

Shared/Independent VLAN Learning

When VLAN function is used, each VLAN group is mapped to the Filtering Identifier (FID). Single or multiple VLAN groups can be assigned to the same or to different FIDs. VLANs assigned to the same FID perform Shared VLAN Learning (SVL). VLANs assigned to different FIDs perform Independent VLAN Learning (IVL). The source MAC address of the received frame can be learned using either IVL or SVL method. Shared and Independent VLAN Learning is defined as follows:

- **Independent VLAN Learning:**
  Each VLAN uses its own filtering database. The source MAC address learning is performed as a result of incoming VLAN traffic and is not made available to any other VLAN for forwarding purposes. One FID is assigned per VLAN group.
- **Shared VLAN Learning:**
  Two or more VLANs are grouped to share common source MAC address information. This setting is useful for configuring complex VLAN traffic patterns without forcing the switch to flood the unicast traffic in each direction. Addressing information is shared among VLANs. One FID is used by two or more VLAN groups.

By default, all VLAN groups are assigned to the same FID (FID=0) and Shared VLAN Learning is performed for the source MAC addresses.

3.7.2.5 Layer 2 Security

This chapter summarizes the L2 security features of the GSWIP. The L2 security features comprise:

- IEEE 802.1X
- MAC Learning Limitation, allows only a limited number of MAC addresses to be learned on a port.
- MAC Port Locking and MAC Spoofing Detection, allows only frames with a previously learned MAC and PortID association.
- MAC Table Freeze, allows only frames with previously learned MAC addresses.
- Source MAC Address Filtering and Destination MAC Address Filtering, filters user defined MAC addresses.

IEEE 802.1X (Port-based Authorization) Support

Gigabit Ethernet Switch Macro supports the port states required for the 802.1X - Port Based Authorization and Network Access Control Protocol functionality. The following states are supported per port:

- Not Authorized. In this state, all frames received on the port will be dropped, the source MAC address will not be learned. Not authorized port will not be taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized for Ingress Traffic only. In this state, all regular traffic received on the port is accepted. However, the port is not allowed to transmit any traffic. This port will not be taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized for Egress Traffic only. In this state, all regular traffic received on the port is discarded. The port is allowed only to transmit traffic. This port can be taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized. Normal operation, ingress and egress traffic on this port is enabled for all frames.

When both protocols, STP and IEEE 802.1X, are enabled - port states for the 802.1X are effective only when STP port state is set to “Forwarding”.

EAPOL frames forwarding

Gigabit Ethernet Switch Macro supports special forwarding rules for the Extensible Authentication Protocol over LAN (EAPOL) frames that are used by the 802.1X protocol to exchange authentication information. EAPOL frames are identified by the unique group destination MAC address $01:80:C2:00:00:03_H$, and the Ethernet Type $88\ 8E_H$.

When 802.1X functionality is enabled, EAPOL frame forwarding is added as a dedicated rule to the Traffic Flow Table with a special action to ignore (cross) any states configured for the ingress or egress ports. EAPOL frames must be forwarded to the defined CPU port or any other port where managing entity is connected for further 802.1X processing.

MAC Learning Disable

The MAC learning can be disabled (via LNDIS bit in PCE_PCTRL_3) per ingress port. If MAC learning is disabled, the source MAC address is not learned and MAC learning limitation is not checked.

MAC Learning Limitation

The number of MAC addresses that are allowed to be learned can be limited per port. This feature provides protection from DoS attacks and avoids bridging table overflow by single ports that are sending too many frames with different source MAC addresses.

By default, the number of MAC addresses that can be learned by the switch is only limited by the size of the internal MAC bridging table. If MAC learning limitation is enabled on the ingress port and the programmed limit is reached, no more addresses are learned for this specific port. Dynamic learning is still enabled on other ports. Learning limitation violation can be indicated to the software and the violating frame can be configured to be discarded or forwarded as a normal frame. Regardless of the forwarding action, the source MAC address of the violating frame will not be learned. Refreshing of already stored addresses is allowed and not considered a violation.

The learning limitation configuration can be changed (increased or decreased) during run-time. If number of addresses that can be learned on the port increased from previous limit, more addresses from that port can now be added to the table. If number of addresses that can be learned on the port decreased, no new addresses are learned and no active flushing is performed to reach the learning limitation. Addresses are expected to be aged out. Note: setting learning limitation to zero disables the dynamic learning on that port, the source MAC address is looked up and violating frame can be configured to be discarded or forwarded.

MAC learning disable, MAC learning limitation and corresponding behavior are described in **Table 24**.

Table 24 MAC Learning disable and MAC Learning Limitation Description

LNDIS in PCE_PCTRL_3 (per ingress port)	LRNLIM in PCE_PCTRL_1 (per ingress port)	PLIMMOD in PCE_GCTRL_0 (global)	Description
1_B	Don't care	Don't care	Source MAC address is not learned, the packets are not dropped
0_B	!= 255	0_B	Source MAC address is not learned and packets are dropped if learning limitation is exceeded. Source MAC address is learned and packets are not dropped if learning limitation is not exceeded.
0_B	!= 255	1_B	Source MAC address is not learned and packets are not dropped if learning limitation is exceeded. Source MAC address is learned and packets are not dropped if learning limitation is not exceeded.
0_B	255	Don't care	Source MAC address is learned and packets are not dropped.

MAC Port Locking and MAC Port Spoofing Detection

The port locking and spoofing detection function are intended to prohibit MAC spoofing attacks.

Ingress traffic from a port carrying a source MAC address that has previously been learned on a different port (port locking enabled on the stored port) is considered a violation. If a port locking violation is detected, this can be indicated to the software and the violating frame can be configured to be discarded. Regardless of the forwarding action, source MAC address of the violating frame will not be learned.

Ingress traffic from the port on which port spoofing detection is enabled (via SPFDIS bit in PCE_PCTRL_0) carrying a source MAC address that has previously been learned on a different port (regardless of its port locking setting) is considered a violation. If port spoofing is detected, this can be indicated to the software and the violating frame can be configured to be discarded (via SPFMOD bit in PCE_GCTRL_1). Regardless of the forwarding

action, source MAC address of the violating frame will not be learned. MAC Port Spoofing detection function allows moving a MAC addresses to the port on which spoofing detection is disabled.

This feature ensures that a malicious user can not spoof another user's MAC address and gain illegitimate access to data traffic that he does not own.

If a user needs to change from one port to another, a wait time up to the configured aging time is required to be able to re-connect. If the locked MAC address is a static entry or if the aging time is too long, moving users between ports on which spoofing detection are enabled or port locking are enabled needs management interaction.

MAC Table Freeze

MAC Table Freeze can be enabled globally to freeze the MAC address table. If enabled no new entries can be entered into the MAC address table even if learning is enabled on the port. Refreshing of existing entries is performed, also if learning is disabled (by setting learning limitation to zero). This features allows to learn the MAC addresses from the connected stations for a given time and then freeze the MAC address table. Afterwards no new MAC addresses are learned. If learning is enabled and port locking is disabled, known stations are allowed to move. If port locking is enabled or learning is disabled, station moves are not allowed.

If a freeze violation is detected it can be configured to either discard the frame or to forward the frame. If the frame is to be discarded it can be configured to send it to the monitoring port. The freeze violation can be indicated to the software via a maskable interrupt.

Source MAC Address Filtering

A static MAC Table entry for specific source MAC address + FID pair can be programmed with a NULL (all-zero) value for the associated port map. If the source MAC address + FID pair of the received frame matches the configured entry, the frame is discarded. This function can be enabled or disabled per port.

Dedicated violation indication is asserted for any frame that has been discarded.

3.7.2.6 Spanning Tree Protocol Support

Gigabit Ethernet Switch Macro supports the port states required for the Spanning Tree Protocol (STP) functionality. 16 spanning tree instances per port are supported. Each Spanning Tree instance is associated with least significant 4 bits of the Filtering Identifier (FID) and a port. The port state programmed for one FID does not have effect on the behavior of another FID of the same port.The following states are supported per STP instance:

- **Disabled:** When disabled, all ingress frames will be dropped, the source MAC address will not be learned. All egress frames will be discarded.
- **Blocking/Listening:** In this state, all ingress and egress regular traffic is discarded. BPDU frames can ignore the port state and be forwarded to the STP managing entity. Source MAC address is not learned in this state.
  - Note: To be recognized by the switch, BPDU frames must be defined in the appropriate rule in Traffic Flow table.
- **Learning:** In this state, all ingress and egress regular traffic is discarded. Source MAC address is learned in this state. BPDU frames can ignore the port state and be forwarded to the STP managing entity.
  - Note: To be recognized by the switch, BPDU frames must be defined in the appropriate rule in Traffic Flow table.
- **Forwarding:** Normal operation, ingress and egress traffic is enabled for all frames.

BPDU frames forwarding

Gigabit Ethernet Switch Macro supports special forwarding rules for the Bridge Protocol Data Unit (BPDU) frames that are used by the STP protocol to exchange information about bridge IDs and root path costs. BPDU frames identified by the unique group destination MAC address $01:80:C2:00:00:00_H$.

When STP functionality is enabled, BPDU frame forwarding is added as a dedicated rule to the Traffic Flow Table with a special action to ignore (cross) any states configured for the ingress or egress ports. BPDU frames must be

forwarded to the defined CPU port or any other port where managing entity is connected for further STP processing.

3.7.2.7 Reserved MAC Addresses

The IEEE standard defines group destination MAC addresses in the range from $01:80:C2:00:00:00_H$ to $01:80:C2:00:00:FF_H$ as reserved. The Gigabit Ethernet Switch Macro can be configured to disable the forwarding of the frames containing reserved addresses. In this case a dedicated rule is added to the Traffic Flow Table with an action to discard any frame within the reserved address range.

3.7.2.8 Flow Control Function

In order to prevent buffer congestion and packet drop the Gigabit Ethernet Switch Macro supports a flow control mechanism. In full duplex operation the sender is notified to start or stop the transmission via a PAUSE frame based on the IEEE 802.3x standard. The Gigabit Ethernet Switch Macro is able to transmit/receive and react accordingly to 802.3x flow control frames. In half duplex operation, the Gigabit Ethernet Switch Macro supports a back pressure mechanism, specifically, a jam pattern will be transmitted on the port forcing a collision. Flow control can be enabled or disabled per port. When enabled, it depends on the auto negotiation result of the attached PHY.

Flow control can be applied in the following ways. When flow control on a port is activated by any one of the below triggerings, flow control is activated on that port. When flow control on a port is deactivated by all the below triggerings, flow control is deactivated on that port.

- **Global flow control:** Flow control is activated when the global buffer congestion level exceeds a programmable global threshold and is deactivated when the global buffer congestion level is below a programmable global threshold. The flow control applies to all enabled ports.
- **Ingress port congestion based flow control:** Flow control is activated when the ingress port local buffer congestion level exceeds a programmable local threshold (via SDMA_PFCTHR9) and deactivated when the local buffer congestion level drops below a programmable local threshold (via SDMA_PFCTHR8). The flow control applies to each port individually.
- **Ingress port metering based flow control:** When the global buffer filling level exceeds a programmable global threshold (via SDMA_FCTHR2), flow control is activated on the port that exceed the configured ingress rate. When the global buffer filling level drops blow a programmable threshold (via SDMA_FCTHR1) or the traffic rate is reduced below the configured rate, flow control is deactivated on the port. See also **Chapter 3.7.5.4** for more details regarding the metering based flow control and metering assignment.

3.7.2.9 Port Trunking Functions

Switch supports link aggregation according to IEEE 802.3ad. Link aggregation, which is also called port trunking, allows to combine multiple ports to a trunk for high bandwidth inter-switch links. Maximum two ports can form a trunk, there is no restriction on the port sequence which are used for the trunk (port 0 and port 1 can form a trunk but also port 0 and port 5 can form a trunk). The ports must have the same speed and have to work in full duplex mode only, otherwise a proper trunking functionality can not be achieved. Fault tolerance is not supported. If one link is broken or disabled for any reason (link on/off), packets are lost.

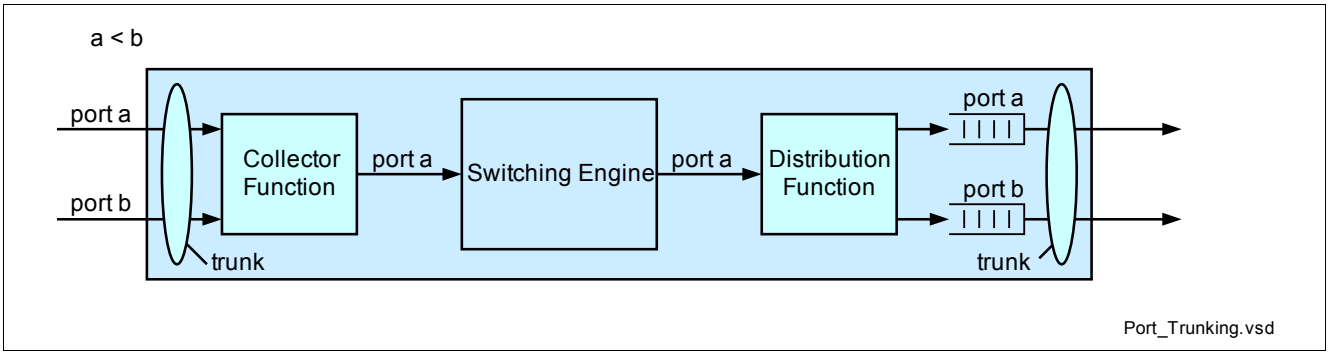


Figure 25 Port Trunking Function

If a frame was received on a trunk, the lowest port number of the trunk is used as ingress port by the collector function. This ingress port alone is used for the further processing, including learning and port security. The other port number (=higher port number of the trunk) is not used, all port parameters are taken from the lowest port number.

If a frame is to be transmitted on a trunk, the lowest port number of the trunk is the default port. Since the trunk consists of two ports it has to be determined which of the ports is used for the transmission. This is done by a distribution function which evenly distributes the frames on the two ports of the trunk.

The distribution is according to either a hash function of 32-bit key (XOR of all bits) or a Flow classification action.

The hash key consists of the following fields.

- MAC Destination Address (MAC_DA): 8 bit only (MAC_DA[7:0]), can be masked via DA bit in PCE_TRUNK_CONF
- MAC Source Address (MAC_SA): 8 bit only (MAC_SA[7:0]), can be masked via SA bit in PCE_TRUNK_CONF
- IP Destination Address (IP_DA): 8 bit only, (IP_DA[7:0]), can be masked via DIP bit in PCE_TRUNK_CONF
- IP Source Address (IP_DA): 8 bit only, (IP_SA[7:0]), can be masked via SIP bit in PCE_TRUNK_CONF

If a field is masked, all zero value is assumed for that field for hash calculation. If a packet is not an IP packet, all zero value is assumed for IP address.

The higher port number of a trunk shall not be configured as destination port or in a destination port map.

RMON counters shall be triggered for each ingress and egress port separately.

Flow control is also separately triggered for each ingress port. Each egress port can be shaped individually. The combined rate shaping of the trunk is also supported.

3.7.2.10 Gigabit Media Access Control (GMAC) Functions

GMAC modules are part of the Gigabit Ethernet Switch Macro and provide the following functions:

- Duplex Modes
  - Each MAC module interface can work in full- or half-duplex mode at any of the provided speeds. The duplex mode can be configured via auto negotiation (autopolling) or forced by register settings
- Preamble Generation
  - For each Ethernet frame, the MAC generates a preamble and at the Start of Frame Delimiter (SFD). During the generation of preamble and SFD the pending data will be delayed. In receive direction, the preamble and SFD are removed
- FCS Generation and Checking
  - The Frame Checksum (FCS) is a 32-bit CRC checksum that covers the destination address, source address, type field, and the payload data. The FCS of each frame is checked in receive direction and is regenerated in transmit direction. The generation of the FCS for an outgoing frame and the check of the FCS for an incoming frame can be disabled per port.
- Full Duplex Flow Control

  - In case the pause frame based flow control is enabled, the MAC generates a pause frame if a congestion situation is signaled. If this situation occurs while the MAC sends a normal frame, the MAC finishes the current transmission and then sends a pause packet. If the congestion situation ends, the MAC finishes the pending transmission and then sends a pause termination packet. The source address of the pause frames is configurable per switch port. A pause frame is identified by a type/length field of 88 08_H. The following two bytes provide the opcode field. For pause operation the opcode is 0001_H. The next two bytes specify the pause length. The pause length is always set to the maximum value of $FFFF_H$, which instructs the link partner to seize transmission for 65535_D slot times. To terminate the pause state, a pause frame with a pause time of 0000_H is sent, allowing the link partner to resume data transmission. Each time the pause state exceeds the length of $65535_D/4 = 16384_D$ slot times, another pause frame is sent automatically to maintain the pause state.
  - Destination MAC address of the pause frame is 01 80 C2 00 00 01_H.
  - The default source MAC address of the pause frame is AC 9A 96 00 00 00_H. This can be changed by configuration.
- Half Duplex Flow Control
  - The flow control in half-duplex mode uses the back-pressure collision mechanism in order to take control over the media. If a congestion situation is signaled, the received frame will be collided and MAC will try to occupy the line with a egress frame transmission or a special back pressure pattern (in case no data pending for this port). If the congestion situation ends, the MAC resumes normal operation.
- Frame Padding
  - The minimum frame size of an untagged Ethernet frame is 64 byte. The MAC fills all Ethernet egress frames with padding bytes until the minimum frame size requirement is fulfilled. The minimum size is 68 byte for tagged frames (containing a single VLAN tag) and 72 byte for stacked frames (containing two VLAN tags). Frame padding can optionally be disabled for untagged, single or stacked frames separately.
- Jumbo Frame Support
  - The maximum frame size is configurable to support jumbo frames of 9K bytes and below.
- Energy Efficient Ethernet Functions
  - For power saving purposes, the Low Power Idle (LPI) mode is supported as defined by IEEE 802.3az.
  - Recording of accumulated LPI state time period is supported. A 32-bit counter (accessible via MAC_LPITMER0 and MAC_LPITMER1) which counts the period during which the LPI idle state is maintained per port. The unit of the counter is 1 us. It is configurable to count one of the LPI state: RX LPI idle state, TX LPI idle state or both TX and RX in idle state.
- IFG Handling
  - The interframe gap (IFG) can be configured in receive and transmit direction. This allows the acceptance of frames with a short IFG of min. 8-bit times. It is possible to transmit frames with an IFG of 8 to 120 bit times. Typically the IFG is 96 bit times.
- The MAC performs several checks on the received frame and signals the following errors. Typically frames with a receive error are discarded but it is also possible to monitor such frames or even ignore the error and process the frame like an error free frame.
  - PHY Error (rx_error)
  - Alignment Error (align_err)
  - Length Error (len_error)
  - Oversized Frame (len_toolong_error)
  - Undersized Frame (len_tooshort_error)
  - FCS Error (crc_error)
  - Pause Frame (pause_frame)

3.7.3 VLAN Functions

This chapter describes VLAN Bridging functionality.

A VLAN is a *Virtual Local Area Network*, a grouping of network devices that is logically segmented by functions or applications without regard to the physical location of the devices. Ports in a VLAN share broadcast traffic and belong to the same broadcast domain. Any traffic in one VLAN is by definition not transmitted outside that VLAN. However, there are exceptions to this general rule which can be configured to cover certain system requirements.

The following chapters provide more details regarding the VLAN functionality.

3.7.3.1 VLAN Association

The VLAN classification function associates each packet received on the ingress side with a specific VLAN group. VLAN association can be performed in one of two ways:

- **Implicit VLAN Association**
  The VLAN group is based on packet attributes. If the association is based on the ingress port it is called *port-based VLAN*. If the association is based on the MAC address, it is called *MAC-based VLAN*. If the association is based on selected packet header fields (such as Ethernet Type, IP Protocol, IP Address Subnet, MAC Address, etc.) it is called *protocol-based VLAN*.
- **Explicit VLAN Association**
  The VLAN group information is carried in a VLAN tag in the Ethernet header of the received packet. This association is called *tag-based VLAN*.

3.7.3.2 VLAN QinQ

IEEE 802.1QinQ is an Ethernet networking standard formally known as IEEE 802.1ad and is an amendment to IEEE standard IEEE 802.1Q-1998. It is for Ethernet frame formats. The technique is also known as provider bridging, Stacked VLANs or simply QinQ or Q-in-Q. The idea is to provide, for example, the possibility for customers to run their own VLANs inside service provider's provided VLAN. This way the service provider can just configure one VLAN for the customer and customer can then treat that VLAN as if it was a trunk.

The original 802.1Q specification allows a single VLAN header to be inserted into an Ethernet frame. QinQ allows multiple VLAN headers to be inserted into a single frame.

In this context, a QinQ frame is a frame that has two VLAN 802.1Q headers (double-tagged). A tag stack creates a mechanism for Internet Service Providers to encapsulate customer tagged 802.1Q traffic with service provider tag, the final frame being a QinQ frame.

A STAG (Service VLAN Tag) frame is identified by assignable Protocol Type value (typically $88A8_H$, but programmable) and followed by two bytes of TCI field. TCI field consists of 3-bit Priority Code Point (PCP) field, 1-bit Drop Eligible Indicator (DEI) and 12-bit VLAN Identifier field (VID).

A CTAG (Customer VLAN Tag) frame is identified by an Protocol Type value (typically 8100_H, but programmable) and followed by two bytes of TCI field. TCI field consists of 3-bit Priority Code Point (PCP) field, 1-bit Canonical Format Indicator (CFI) and 12-bit VLAN Identifier field (VID).

3.7.3.3 Supported Frame Format

STAG can be configured to be enabled or disabled per port via STEN bit in PCE_PCTRL_2.

If STAG is enabled on a port, the supported frame formats are shown in **Figure 26**. If STAG is not enabled on a port, the supported frame formats are shown in **Figure 27**.

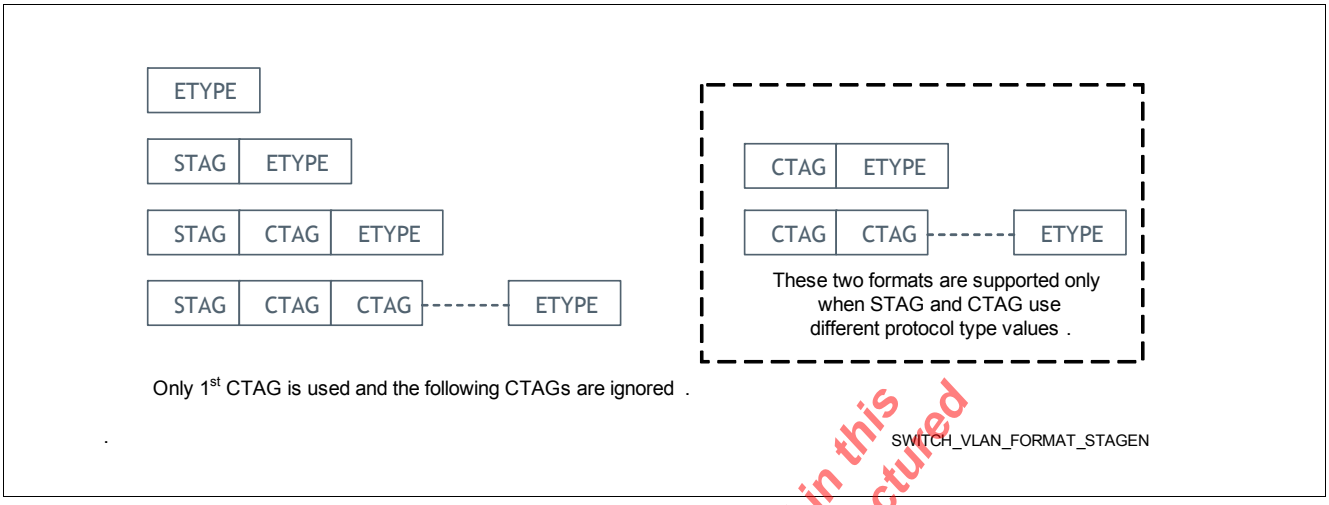


Figure 26 Supported Frame Formats when STAG is Enabled

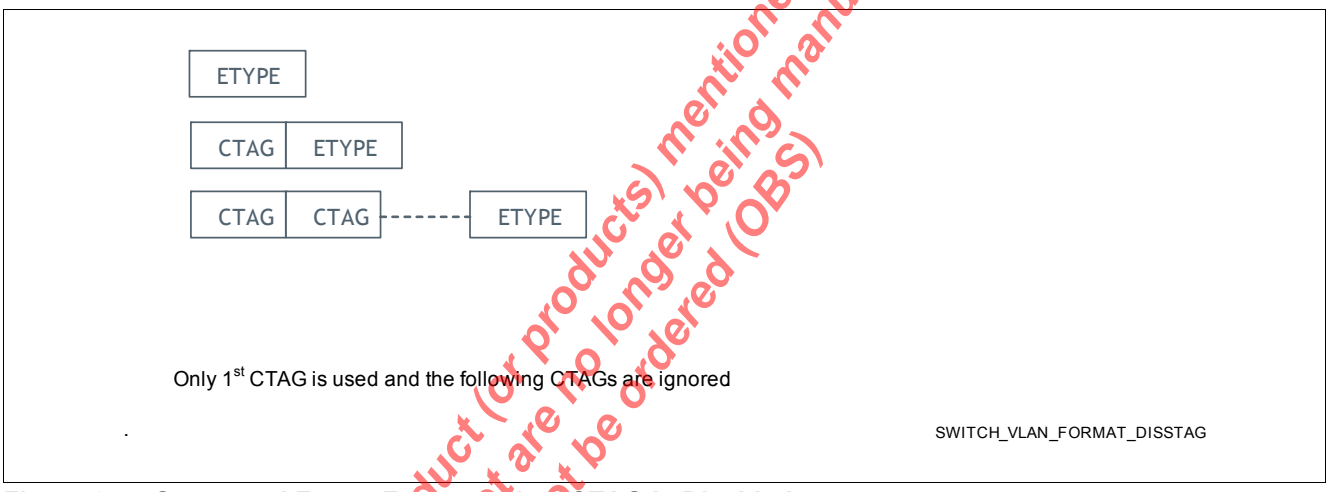


Figure 27 Supported Frame Formats when STAG is Disabled

3.7.3.4 Double VLAN Tag Function

Double tag VLAN function is supported. Double VLAN mode is enabled via setting VLANMD bit in PCE_GCTRL_1 to 1_B.

For every packet, there are two VLAN groups: STAG VLAN group and CTAG VLAN group.

STAG VLAN group can determine if CTAG VLAN group is ignored or not.

- If CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG filtering, CTAG insertion and CTAG removal are not performed.
- If CTAG VLAN group is not ignored, CTAG filtering, CTAG insertion and CTAG removal are performed together with STAG filtering, insertion and removal. Both CTAG filtering and STAG filtering apply on the packet.

3.7.3.5 Filtering Identifier Assignment

Single or multiple VLAN groups can be assigned to the same Filtering Identifier (FID) or to different FIDs. There are the following ways to map the traffic to FID.

- Default Customer VLAN ID (either ingress port CTAG VID or ingress CTAG VID)
- Packet's multiple fields via the traffic flow classification

– A packet is associated to an alternative FID based on multiple fields of a packet, for example, ingress port, service VLAN Tag VID, customer VLAN Tag VID, Source MAC, Destination MAC, source IP, destination IP, etc. Please refer to **Chapter 3.7.6** for more details regarding to traffic flow classification.

Please refer to **Shared/Independent VLAN Learning** for more details regarding Shared/Independent VLAN learning functionality.

3.7.3.6 VLAN Filtering

Received frame can be forwarded or discarded based on the VLAN group configuration and configured port attributes. The sub-chapters below describe the available filtering modes that can be applied.

CTAG and STAG Ingress Admit Mode

This mode is applied to ports to limit the ingress traffic to a certain profile, with respect to the embedded STAG and CTAG. The following filtering rules are relevant for both STAG and CTAG. There are separate mode configurations for STAG and CTAG. In case of contradiction, the discard rule has higher priority. For example, when according to CTAG filtering the frame is to be discarded and according to STAG filtering is to be admitted, the final rule is to discard the frame:

- Admit VLAN tagged frames only
  Only Ethernet frames that contain a VLAN tag in the Ethernet header are allowed on this port. If a received frame does not contain a VLAN tag, the frame will be discarded.
  – Note: Priority tag (VID=000_H) is not regarded as a VLAN tag, since it contains no explicit VLAN group. Priority tagged frames are discarded in this mode.
- Admit untagged frames only
  Only packets containing no VLAN tag or containing a priority tag only (VID=000_H) are allowed on this port. If a received frame contains a VLAN tag, the frame will be discarded.
- Admit all
  Both tagged and untagged frames are allowed on the port.

STAG ingress admit mode is configurable via SVINR field in PCE_VCTRL of each port. CTAG ingress admit mode is configurable via VINR field in PCE_VCTRL of each port.

STAG VLAN Group and CTAG VLAN Group Port Members

Port members identify the broadcast domain of the group. The broadcast domain of the received packet will be restricted according to the VLAN membership ports and will be delivered only on ports belonging to the same broadcast domain.

STAG VLAN group membership is configured via traffic flow classification action for the matched STAG VLAN group association. CTAG VLAN group membership is configured via CTAG VLAN membership table.

By default, both STAG VLAN filtering and CTAG VLAN filtering applies. In case of contradiction, the discard rule has higher priority. For example, when according to CTAG filtering a port is not in the port member list, and according to STAG filtering the port is in the port member list, the final rule is that the port is not in the port member list. But STAG VLAN group can determine if CTAG VLAN group is ignored or not. This is configured via traffic flow classification action for the matched STAG VLAN group association. If CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG filtering is not performed. Please refer to **Chapter 3.7.6** for more details regarding to traffic flow classification

CTAG and STAG Membership Filtering Mode

This mode enforces packet forwarding based on the port members in the associated VLAN group.

- Ingress Membership Filtering Mode
  The ingress port of the received frame is compared with the port members of the associated VLAN group. When this filtering mode is enabled, the packet is discarded if the ingress port is not contained in the port

member list. The ingress membership filtering mode for STAG is configurable via SVIMR field in PCE_VCTRL of each port. The ingress membership filtering mode for CTAG is configurable via VIMR field in PCE_VCTRL of each port.

- Egress Membership Filtering Mode
  The egress membership filtering is the primary VLAN functionality. The egress port of the frame is compared with the port members of the associated VLAN group. When this filtering mode is enabled, the packet is discarded if the egress port is not contained in the port member list. When frames are destined to multiple ports (multicast or broadcast packets), ports that are not included in the VLAN member list are excluded from transmission and a copy of the frame is not delivered to these ports. The egress membership filtering mode for STAG is configurable via SVEMR field in PCE_VCTRL of each port. The ingress membership filtering mode for CTAG is configurable via VEMR field in PCE_VCTRL of each port.
- Ingress and Egress Membership Filtering Mode. This mode is a combination of the previous two modes. In this mode, both ingress and egress ports are compared with the port member list of the associated VLAN group.

Cross-VLAN Functionality

Ethernet frames that are classified as cross-VLAN ignore any of the VLAN filtering modes for the ingress or egress ports and as such cross the VLAN boundaries.

Cross-VLAN classification is performed as part of the Traffic Flow classification function. Please refer to **Chapter 3.7.6** for more details.

3.7.3.7 VLAN Tagging and Untagging

Tag members identify the group of egress ports on which the frame associated with the VLAN group should be transmitted as a VLAN-tagged frame. In this case, the associated VLAN is used for the VLAN ID of the transmitted frame.

STAG VLAN Tagging and Untagging

The ports with STAG VLAN enabled are the tag members of all STAG VLAN group. STAG can be configured to be enabled or disabled per port via STEN bit in PCE_PCTRL_2.

CTAG VLAN Tagging and Untagging

The tag members is configured per CTAG VLAN group via VLAN membership table. But STAG VLAN group can determine if CTAG VLAN group is ignored or not. This is configured via traffic flow classification action for the matched STAG VLAN group association. If CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG tagging and untagging is not performed and CTAG is not modified. Please refer to **Chapter 3.7.6** for more details regarding to traffic flow classification.

3.7.3.8 Transparent VLAN Mode

A port that is configured to *Transparent VLAN Mode* (TVM) ignores the explicit VLAN association and treats all received Ethernet frames as untagged frames, regardless of any existing VLAN tag in the Ethernet header. All tagged and untagged traffic on that port is associated with the port-based VLAN group. If the received packet contains a VLAN tag, this tag is treated as a part of the payload. There is separate transparent mode configuration for CTAG ad STAG. If STAG transparent mode is enabled, CTAG must be configured to transparent mode too, otherwise the switch's behavior is undefined. STAG transparent mode is configurable via STVM field in PCE_VCTRL of each port. CTAG transparent mode is configurable via TVM field in PCE_PCTRL_0 of each port.

If transparent VLAN mode is enabled, ingress admit mode must be set to "Admit Untagged Frames Only" or "Admit All", since all frames are treated as if they were untagged frames.

VLAN Stacking

If TVM is enabled, the VLAN tag member attribute has a slightly different functionality for tagged frames. If the received frame contains a VLAN tag and the egress port is one of the VLAN tag members, the port-based VLAN is added to the frame as an additional outer tag. If the egress port is not one of the tag members, the packet is transmitted without modification, with the original VLAN tag (if any).

VLAN ID=0 Handling

It can be configured per ingress port if a frame with a VLAN ID=0 (priority tagged frame) shall be handled like an untagged frame. If enabled, a priority tagged frame in transparent mode would receive a single tag with VID=PVID, if disabled a priority tagged frame in transparent mode would receive a VLAN tag with VID=PVID on top of the priority tag (priority tag is tunneled in the PVID). The PCP of a priority tagged frame is still used even if the frame is handled like an untagged frame. Priority STAG VLAN handling mode is configurable via SVID0 field in PCE_VCTRL of each port. Priority CTAG VLAN handling mode is configurable via VID0 field in PCE_VCTRL of each port.

3.7.3.9 VLAN Security Mode

If VLAN security mode is enabled on an ingress port, all tagged and untagged traffic on that port is associated with the port-based VLAN group. There are separate mode configuration for STAG and CTAG. STAG VLAN security mode is configurable via SVSR field in PCE_VCTRL of each port, CTAG VLAN security mode is configurable via VSR field in PCE_VCTRL of each port.

If the received frame contains a VLAN tag and the egress port is port and tag member of the port-based VLAN group, the port-based VLAN replaces the original VLAN tag in the Ethernet header. If the egress port is port member but not tag member of the port-based VLAN group, the original VLAN tag is stripped prior to transmission. If the frame has been received with more than one VLAN tag, the outer tag is removed.

Please note the difference between the TVM and VLAN security mode for tagged packets:

- Egress port is port and tag member of the port-based VLAN:
  - Transparent VLAN Mode: The port-based VLAN tag is added in addition to any existing VLAN tag. The number of VLAN tags in the frame is increased by one.
  - VLAN Security Mode: The port-based VLAN tag replaces the existing VLAN tag. The number of VLAN tags in the frame remains the same.
- Egress port is port member but not tag member of the port-based VLAN:
  - Transparent VLAN Mode: The frame is transmitted without modification, containing the original VLAN tag. The number of VLAN tags in the frame remains the same.
  - VLAN Security Mode: The original VLAN tag is removed from the frame. The number of VLAN tags in the frame is reduced by one.

3.7.3.10 Reserved VLAN Groups

Any VLAN group in the active VLAN set can be assigned to a reserved VLAN group list by setting the reserved indication in VLAN membership table. The VLAN ID of a frame belonging to a reserved VLAN group can be replaced with the port-based VLAN group. If the frame contains a reserved VLAN tag and the egress port is port member and tag member of the port-based VLAN group, the port-based VLAN ID replaces the original VLAN ID in the Ethernet header.

Please note the difference between the VLAN Security and Reserved VLAN functions: VLAN Security is applied on all traffic received on a certain port and Reserved VLAN is applied for a specific VLAN group on a certain port.

This feature applies only to CTAG.

3.7.3.11 VLAN Translation

Frames received with a certain VLAN ID can be modified on the egress and contain a different VLAN ID. The chapters below describe the relevant functions related to the VLAN modification. Please note, if VLAN modification is applied, the VLAN membership filtering rules are based on the egress (translated) VLAN group.

STAG VLAN Translation

The egress STAG VLAN ID can be one of the following:

- Ingress Port STAG VLAN ID in the following cases
  - Untagged packets
  - Ingress port is in STAG transparent mode
  - Ingress port is in STAG security mode
- Ingress STAG VLAN ID in the following cases
  - Tagged packets if ingress port is not in transparent mode and not in security mode
- Alternative STAG VLAN ID
  - Alternative STAG VLAN ID is configured via traffic flow classification action for the matched STAG VLAN group association

CTAG VLAN Translation

The egress CTAG VLAN ID can be one of the following:

- Ingress Port CTAG VLAN ID in the following cases
  - Untagged packets
  - Ingress port is in CTAG transparent mode
  - Ingress port is in CTAG security mode
  - The ingress CTAG VLAN ID is a reserved VLAN group ID
- Ingress CTAG VLAN ID in the following cases
  - Tagged packets if ingress port is not in transparent mode, not in security mode and the not reserved VLAN group
- Alternative CTAG VLAN ID
  - Alternative CTAG VLAN ID is configured via traffic flow classification action for the matched CTAG VLAN group association

3.7.3.12 VLAN Priority Code Point

A dedicated Class of Service (CoS) can be assigned based on either Service TAG VLAN Priority Code Point (PCP) and Drop Eligibility Indication (DEI) or Customer TAG VLAN Priority Code Point in the received VLAN-tagged frames.

CTAG PCP, STAG PCP and DEI can be regenerated for tagged frames or generated for untagged frames, based on the CoS that is assigned to that packet.

See **Chapter 3.7.5** for more details regarding the CoS assignment and PCP&DEI generation and re-generation.

3.7.3.13 Port Based VLAN Examples

For a port-based VLAN group, the VLAN association is based on the ingress port number.

Every ingress port is configured with a port-based VLAN ID (PVID). The configured PVID has to be part of the active VLAN set. Ingress ports configured with the same PVID belong to the same VLAN group. Any untagged packet that is received on a port will be associated, by default, with the port-based VLAN group configured for that port.

Port-based VLAN Example

Figure 28 shows an example where four LAN stations are connected to a single 4-port switch device. Two VLAN groups are set up with two port members for each group. The active VLAN set contains two groups: port 0 and port 1 are members of VID = 10, port 2 and port 3 are members of VID = 11. Ethernet frames will be exchanged between port 0 and port 1 as well as between port 2 and port 3, but not between port 0/1 and port 2/3.

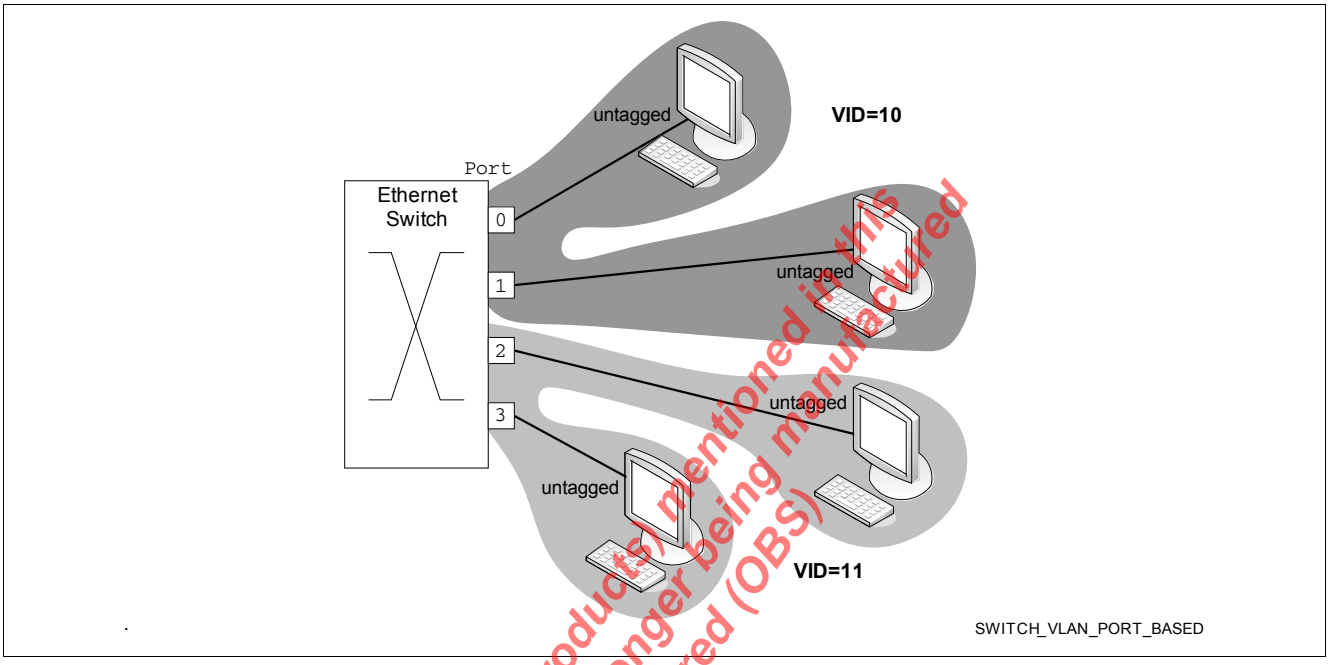


Figure 28 Port-based VLAN Example

3.7.3.14 Single Tag Based VLAN Examples

In a tag-based VLAN group, the VLAN association is based on the outer customer VLAN tag detected in the header of the received Ethernet frame.

Tag-based VLAN Example

Figure 29 shows an example where six LAN stations are connected to a single 6-port switch device. Three VLAN groups are added to the active VLAN set. Port 0 and port 1 are members of the port-based VLAN group with VID =10, port 2 and port 3 are members of the port-based VLAN group with VID = 11. Port 4 is member of the port-based VLAN group with VID = 12. Port 5 is connected to a server and may transmit and receive tagged VLAN packets of any of the defined groups.

Every configured VLAN group adds port 5 as a port and tag member. In this case, packets received from one of the untagged (VLAN unaware) LAN segments are transmitted as tagged Ethernet frames when they are targeted to port 5. The attached VLAN tag is the port-based VID of the ingress port.

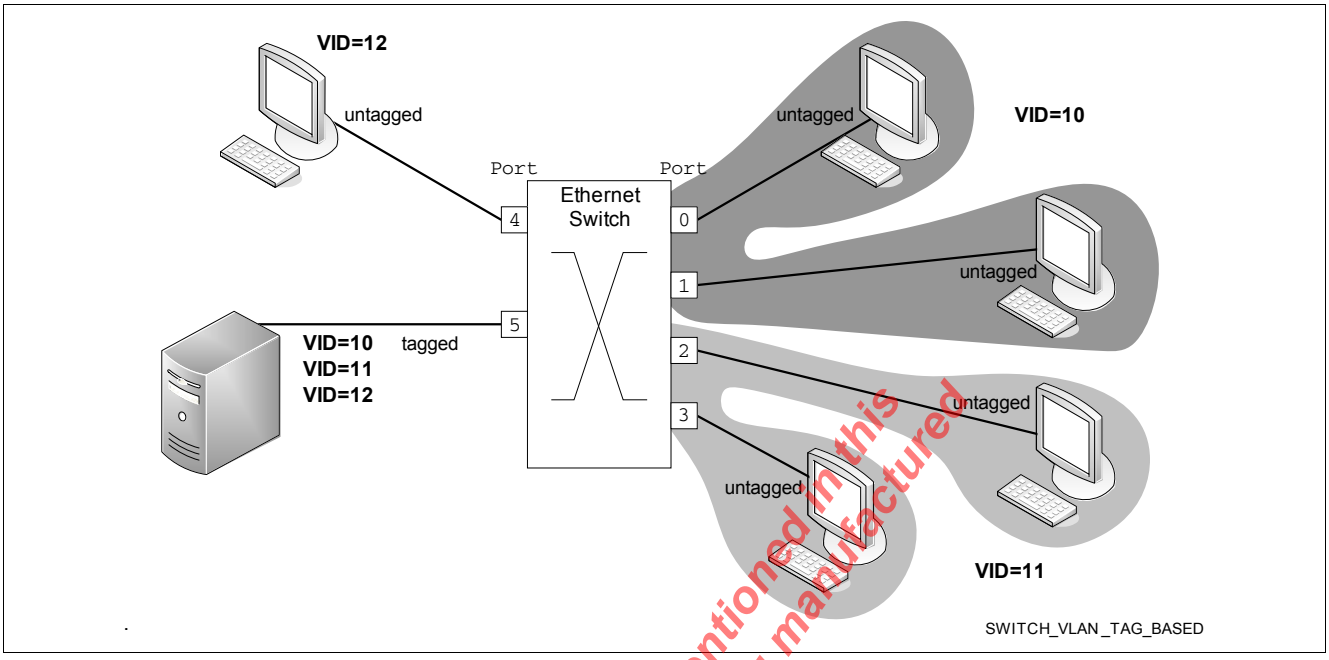


Figure 29 Tag-based VLAN Example

3.7.3.15 Double Tag Based VLAN Examples

In a double tag-based VLAN group, the VLAN association is based on STAG and CTAG detected in the header of the received Ethernet frame.

Figure 30 shows an example where six LAN stations are connected to a single 6-port switch device.

Port 5 is connected to a server and may transmit and may receive double tagged VLAN packets of any of the defined groups.

Table 25 Port Settings

Port	Port STAG Enable	Port SVID	CTAG Transparent Mode	Port CVID
0,1	Disable	301	No	Don't Care
2,3	Disable	302	Yes	11
4	Disable	301	Yes	12
5	Enable	Don't Care	No	Don't Care

Table 26 CTAG VLAN Membership Table

CTAG VLAN ID	CTAG Port Members	CTAG Tag Members
10	0, 1, 5	0,1,5
12	4, 5	5
11	2,3,5	Null

Table 27 Traffic Flow Table

STAG VID Pattern	Port Bitmap Action	Port Bitmap Multiplexing Control	Port Bitmap[1)]	VLAN Action	CTAG Ignore Control
301	1_B	1_B[2)]	0,1,4,5	0_B	Don't care
302	1_B	1_B[3)]	2,3,5	1_B	1_B[4)]

1) When Port Bitmap Multiplexing Control is 1_B, Port BitMap is used as STAG Port Members
2) When Port Bitmap Multiplexing Control is 1_B, Port BitMap is used as STAG Port Members
3) When Port Bitmap Multiplexing Control is 1_B, Port BitMap is used as STAG Port Members
4) When CTAG Ignore Control is 1_B, CTAG VLAN group is ignored and CTAG is treated as transparent.

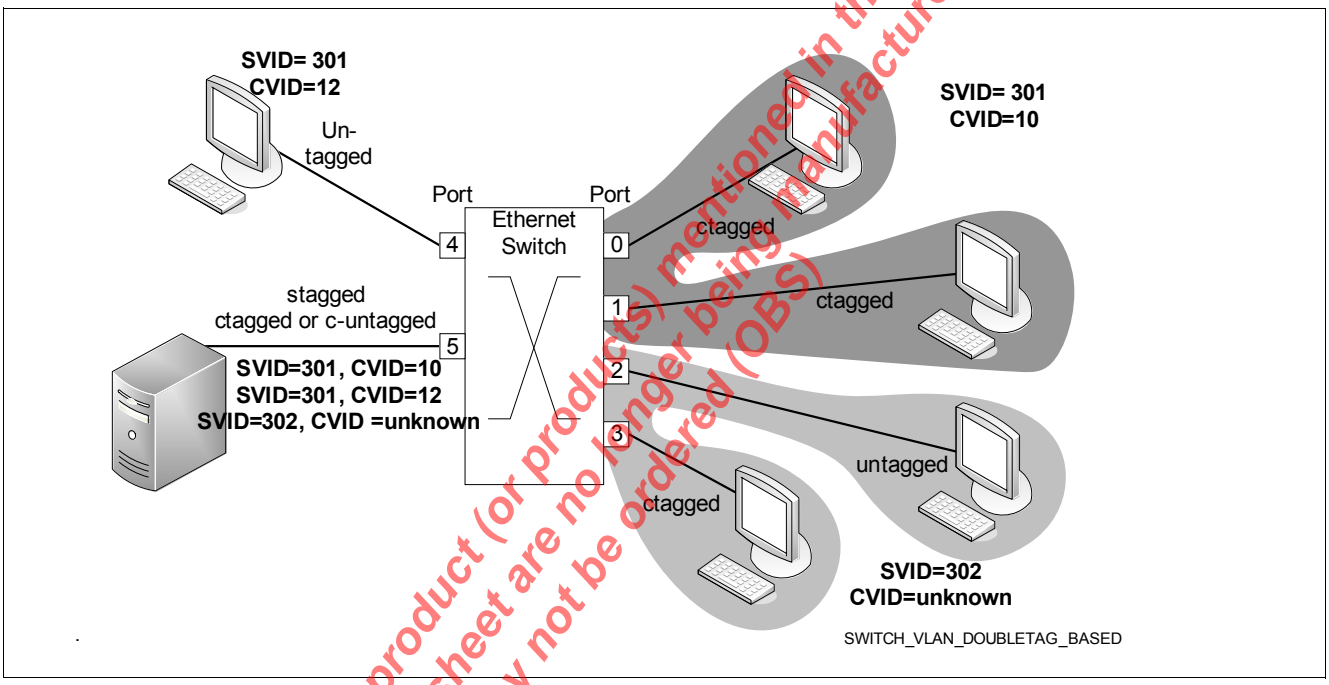


Figure 30 Double Tag and Port based VLAN Example

3.7.4 Multicast Forwarding Functions

Multicast forwarding is a method of forwarding Ethernet frames or IP datagrams to a group of receivers. A basic Ethernet switch floods all received multicast frames to all output ports even if no host on a port is interested in that particular multicast stream. This waste of bandwidth is avoided by the sophisticated multicast handling of the Gigabit Ethernet Switch Macro which allows to forward multicast frames based on L2 or L3 addresses to dedicated ports. In addition the Gigabit Ethernet Switch Macro is able to learn L3 multicast group addresses via IGMPv1/2 snooping in hardware.

The Gigabit Ethernet Switch Macro can be configured to ignore L3 information and forward multicast frames based on MAC destination address only. In this case, L2 multicast addresses must be added to the bridging table with the appropriate port members and is populated by software.

If L3 multicast handling is enabled and the packet contains an IP multicast address, a lookup in the dedicated L3 multicast table is performed. The frame is forwarded to the destination port (or multiple destinations) based on the match result. If the frame contains no IP multicast address or if there was no match in the L3 multicast table, a lookup based on the MAC address is done in the bridging table. A lookup match results in a port map which indicates relevant destination ports. **Table 28** describes frame forwarding decision. If there was no match in the bridging table, the non-IP multicast frame is forwarded according to the default multicast port map (via PCE_PMAP_2). If there is no match in bridging table and no match in L3 multicast table, the IP multicast data frame (IP protocol is not IGMP and MLD) is discarded or forwarded to default multicast port map. IGMP or MLD message frames are forwarded according to IGMP/MLD types.

Note: The lookup in the L2 bridging tables is done with the MAC address regardless if the address is a unicast, multicast or broadcast address. This means that a mix of unicast, multicast and broad cast entries can be entered into the tables and that unicast addresses can also be forwarded to multiple ports. The lookup in the IP multicast table is done with the IP address only if the address is IP multicast.

Table 28 Multicast Forwarding Decision

Forwarding Mode	Packet Type	L3 Multicast Table	Bridging Table	Destination Result
L2 only	Don't Care	Don't Care	No Match	Default multicast port map (configured via PCE_PMAP_2).
L2 only	Don't Care	Don't Care	Match	Bridging Table, matched entry port members.
L2 / L3	IGMP/MLD Control	See **Table 31**.		
L2 / L3	IP Multicast (Excluding IGMP/MLD Control Packets)	Match	Don't Care	L3 Table, matched entry port members.
L2 / L3	Any Multicast (Excluding IGMP/MLD Control Packets)	No Match	Match	Bridging Table, matched entry port members.
L2 / L3	IP Multicast (excluding IGMP/MLD Control Packets)	No Match	No Match	Two Options (configured via UKIPMC bit in PCE_GCTRL_1): 0: Default multicast port map (default mode) 1: Discard
L2 / L3	Non-IP Multicast	No Match	No Match	Default multicast port map.

<Informative> IPv4 multicast addresses are in the group historically called Class D, based on the leading bits of these addresses. The group includes the addresses from 224.0.0.0 to 239.255.255.255, or, equivalently, 224.0.0.0/4. Multicast addresses in IPv6 have the pr*efix* ff00::/8_H. On Layer-2, IPv4 multicast packets are delivered

by using the Ethernet MAC address range $01:00:5e:00:00:00_H$ - $01:00:5e:7f:ff:ff_H$. This is 23 bits of available address space. The first octet includes the broadcast/multicast bit. The lower 23 bits of the 28-bit multicast IP address are mapped into the 23 bits of available Ethernet address space. This means that there is ambiguity in delivering packets. If two hosts on the same subnet each subscribe to a different multicast group whose address differs only in the first 5 bits, Ethernet addresses for both multicast groups will be the same. For IPv6 Multicast addresses, the Ethernet MAC address is derived by the four low order octets OR'ed with the MAC address $33:33:00:00:00:00_H$.

3.7.4.1 Layer-2 Multicast Forwarding

Layer-2 Multicast forwarding function deals with multicast frame forwarding based on the Ethernet MAC Address. The destination port map is looked up in the Bridging table. Multicast addresses will not be added to the Bridging table by automatic learning function and must be configured manually, by appropriate management action. The associated port map will contain all the relevant port members. If the destination MAC address of the received frame matches the entry in the Bridging table and the Forwarding Mode is Layer-2 only or there was no match in the Layer-3 multicast table or the packet is Non-IP multicast, the frame will be delivered to all the destinations specified in the associated port map.

<Informative> MAC Address is defined as multicast if the least significant bit of the most significant byte is set to "1_B". Broadcast Address (MAC address =FF:FF:FF:FF:FF:FF$_H$) is a special case and treated in this description as Multicast.

3.7.4.2 Layer-3 Multicast Forwarding

Layer-3 Multicast function deals with multicast frame forwarding based on the IPv4 or IPv6 Network Address. The destination port map is looked up in the L3 multicast table.

The lookup in the multicast table is performed using the destination IPv4/IPv6 address and optionally the source IPv4/IPv6 address. The addresses in the table are added automatically by hardware based IGMP snooping (see **Chapter 3.7.4.3** for more details) or by appropriate management action. In any source multicast (ASM) as in IGMPv1/IGMPv2/MLDv1 the source IP information is not required, in source specific multicast (SSM) as in IGMPv3/MLDv2 the source IP information is used for the lookup. For SSM the include and exclude mode is supported. In include mode, the packets are forwarded to the multicast group address if they come from a specified IP source address (or multiple addresses). In exclude mode, the packets are forwarded to the multicast group address if they do not come from a specified IP source addresses.

3.7.4.3 IGMP and MLD Snooping

The Gigabit Ethernet Switch Macro supports IGMP (Internet Group Management Protocol) and MLD (Multicast Listener Discovery) snooping. IGMP/MLD snooping is designed to prevent hosts on a local network from receiving traffic for a multicast group they have not explicitly joined. It provides a mechanism to prune multicast traffic from links that do not contain a multicast listener (IGMP/MLD group member). IGMP/MLD snooping requires the Gigabit Ethernet Switch Macro to examine, or snoop, some Layer-3 information in the IGMP/MLD packets sent between the hosts and the router. In addition, adjacent routers also use these protocols to communicate and share routing information. This information exchange can be snooped as well to identify the multicast router port.

The Gigabit Ethernet Switch Macro supports HW-based IGMP snooping mode for the IGMPv1/IGMPv2 protocols. In this mode, L3 multicast addresses are added to the multicast table or removed from it automatically, based on the relevant IGMP reports. No software intervention is required in this mode. See **HW Based IGMP Snooping** for more details.

The Gigabit Ethernet Switch Macro supports SW-based IGMP/MLD snooping mode for the IGMPv1/2/3 or MLDv1/2 protocols. In this mode, specific IGMP/MLD reports can be intercepted by the switch and delivered to the CPU/Network Processor port. The reports are analyzed by the CPU and the L3 multicast table is populated by the SW with appropriate source/destination addresses. See **SW Based IGMP/MLD Snooping** for more details.

HW Based IGMP Snooping

When HW-based IGMP snooping is enabled, the Gigabit Ethernet Switch Macro analyzes all IGMPv1/IGMPv2 packets between hosts connected to the switch and multicast routers in the network. **Table 29** and **Table 30** describe the packet structure of IGMP messages intercepted by the switch, these patterns are added as a dedicated rule to the Traffic Flow Table. **Table 29** describes the messages sent by the multicast host and **Table 30** describes the messages sent by the multicast router.

Table 29 Multicast Host Messages

Field	IGMPv1 Report	IGMPv2 Report	Leave
MAC_DA	01 00 $5E_H$--IP_DA	01 00 $5E_H$--IP_DA	01 00 5E 00 00 02_H
Ethertype	0800_H	0800_H	0800_H
IP Protocol (=IGMP)	02_H	02_H	02_H
IP_SA	Host_IP Address	Host_IP Address	Host_IP Address
IP_DA	Group_IP_Address	Group_IP_Address	224.0.0.2 or Group_IP_Address
Type	12_H	16_H	17_H
Max. Response Time	0	0	0
Group Address	Group_IP_Address	Group_IP_Address	Group_IP_Address

Table 30 Multicast Router Messages

Field	Solicitation	Advertisement	General Query	Group Specific Query
MAC_DA	01 00 5E 00 00 02_H	01 00 5E 00 00 $6A_H$	01 00 5E 00 00 01_H	01 00 $5E_H$--IP_DA
Ethertype	0800_H	0800_H	0800_H	0800_H
IP Protocol (=IGMP)	02_H	02_H	02_H	02_H
IP_SA	Router_IP Address	Router_IP Address	Router_IP Address	Router_IP Address
IP_DA	224.0.0.2	224.0.0.106	224.0.0.1	Group_IP_Address
Type	31_H	30_H	11_H [1)]	11_H

1) For IGMPv1 the type = 1 but together with the version = 1 a IGMPv2 host sees 11_H

When the switch detects an IGMP report or join group message sent from a host for a given multicast group, the switch adds the host's port number to the multicast table entry for that group. When a IGMP leave group message is received from a host, the host's port number is removed from the appropriate table entry when fast leave (also called immediate leave) mode is enabled. See sections below for more details.

Joining Multicast Group:

When the Gigabit Ethernet Switch Macro receives a host membership report on one of the ingress ports and HW-based IGMP snooping is enabled, this port is added to the specified multicast group in the L3 multicast table. When there was no such group entry in the table, a new entry is created with the appropriate group IP address. Received membership report is forwarded to the multicast router port (or multiple router ports).

Report Suppression:

The Gigabit Ethernet Switch Macro supports suppression of membership reports or join messages in order to reduce processing load of the multicast router. When report suppression is enabled, only the first report for specific group is forwarded to the router port. The rest of the reports from the other hosts are discarded. The suppression can be configured per port and can be selected separately for join or report messages.

"Join" message is an IGMP membership report from a host that previously did not participate in a group.

Leaving Multicast Group:

If a host wants to leave a multicast group it can send a Leave message (IGMPv2) or should not send a Report message after a Query (IGMPv1). A Leave message is sent to the all-routers multicast group (224.0.0.2) or to the group a host wants to leave.

Each port in the joined group maintains an aging timer. Repeated Reports refresh the timer. If no Reports are received for a particular group before this timer has expired, the router assumes that the group has no local members and that it need not forward multicast frames for that group. Robustness variable is supported and determines how often the response timer is allowed to expire before the port is actually deleted. If the port map becomes zero the whole entry is deleted from the L3 multicast HW table. The response timer is reset each time a new query was received.

The age time for the entries is derived from the response time received in the IGMP Query messages. For a group specific query the response time is used only for the corresponding group, for a general query the response time is used for all the groups. It can be programmed that the default response time is used instead of the response time from the query message.

The Gigabit Ethernet Switch Macro supports a fast leave (also called immediate leave) feature. When fast leave is enabled and an IGMP Leave is received, the port from which the IGMP packet was received is cleared immediately from the port map of the corresponding group IP address. If the port map is empty, the group IP address and port map are deleted from the L3 multicast HW table. If fast leave is not enabled, the ports and group IP addresses age out if no reports have been detected for a given time.

Note: Enable fast leave mode where only one host is connected to each interface. If fast-leave is enabled where more than one host is connected to an interface, some hosts might be dropped inadvertently.

Router Port Detection:

The Gigabit Ethernet Switch Macro supports automatic detection of the multicast router port, based on the typical multicast router messages described in **Table 30**. If router port detection (auto-learning) is enabled, the learned router port is added as a destination to the snooped IGMP reports received from hosts and as a destination to any multicast frame destined to the hosts.

The default Router Port can also be configured by appropriate management action.

Each learned router port (or multiple ports) maintains an aging timer and can age out if the router message exchange is stopped on a port. The timer is automatically reset each time a new router message is received. If a port does not receive any router messages within the specified time period, the port is deleted from the learned router port map.

Multicast Steam Forwarding:

Table 31 describes typical forwarding destination for the multicast frames. Multicast data frames are typically received from the router port and forwarded based on the match in the L3 multicast table and to the router ports. If there was no match in the L3 multicast table the frames are forwarded based on the L2 addresses or to the default IP/IGMP multicast port map.

Table 31 Typical IGMP/MLD Control Packets Forwarding Destination

IGMP Message Name	Port Map
Report	Multicast router port map
Leave	Multicast router port map
General Query or Group Specific Query	Forwarding port map (based on L3 or L2 multicast table) + Multicast router port map
Unknown General Query or Group Specific Query	Default multicast port map+ Multicast router port map

SW Based IGMP/MLD Snooping

When SW-based IGMP snooping is enabled, IGMP/MLD control frames from Non-CPU ports are forwarded to the CPU port (IGMP/MLD control frame patterns are added as dedicated rules to the Traffic Flow Table as shown in Table 32) and the L3 multicast table is populated by software. IPv4 / IPv6 source and destination addresses can be added to the table and specify the direction of the multicast streams. A source address can be added using one of the following modes:

- Include Mode. In this mode, the forwarding of the multicast frame is based on the source and destination address pair. Specifically: the frame is forwarded to the specified port map only when both addresses (the source and destination) match in the L3 multicast table.
- Exclude Mode. In this mode, the forwarding of the multicast frame is based on destination and source address pair. Specifically: the frame is forwarded to the specified port map only when the source address doesn't match the address in the table and the destination address matches. If a frame contains specified source and destination address, this frame will be discarded. If a frame contains any other source address and a matched destination, this frame will be forwarded.
  - Please note, for any entry added in exclude mode, up to two entries in the L3 multicast table might be created. Exclude entry is implemented using two entries in include mode: one contains an include entry with the wild-card source address and another an include entry with the respective host port cleared in the port map.
- "Don't Care" Mode. In this mode, the source IP address field of the packet is ignored and the multicast frame forwarding is based on the destination IP address alone.

Table 32 IGMP/MLD Messages

Field	IGMPv1/v2/v3 Host Messages	IGMPv1/v2/v3 Router Messages	MLDv1/v2 Host Messages	MLDv1/v2 Router Messages
IP Type	IPv4	IPv4	IPv6	IPv6
IP Protocol	2	2	58	58
Type	18, 24, 25, 34	17, 48, 49	131 - 132	130, 151 - 153

Table 33 Typical IGMP/MLD Messages Forwarding Destination

Source Port	IGMP/MLD Message Name	Port Map
Non-CPU	All messages	CPU Port
CPU	Host Messages	Router port map
CPU	Router Messages	Forwarding port map (based on L3 or L2 multicast table or default multicast port map)

3.7.5 Quality of Service Functions

The Gigabit Ethernet Switch Macro provides extensive support for Quality of Service functionality. Particularly, traffic class assignment based on multiple flow parameters, ingress traffic policing, multiple egress queues per port with strict or WFQ scheduling, traffic shaping and weighted random early discard (WRED) functions are supported.

Next chapters describe in more details the QoS functions supported by the switch.

3.7.5.1 Class of Service Assignment

The Gigabit Ethernet Switch Macro supports classification of the incoming traffic into traffic classes or classes of service (CoS). Each traffic class can be managed (e.g., remarked, policed, shaped) differently, ensuring preferential treatment for higher-priority traffic on the network. The Gigabit Ethernet Switch Macro is able to assign the traffic class of the received packet, based on the following parameters:

- **Ingress Port:** CoS is based on the ingress port number of the received packet. This mode is used by default when no other criteria can be matched.
- **STAG PCP&DEI and CTAG PCP (VLAN Priority Code Point):** CoS is based on the VLAN priority code point placed in the VLAN tag of the incoming packet. The Gigabit Ethernet Switch Macro provides a global STAG PCP&DEI to Traffic Class assignment table and a global CTAG PCP to traffic class assignment table. In the tables, any STAG VLAN PCP/DEI or CTAG VLAN PCP combination is mapped to an appropriate class of service. Traffic class mapping from STAG VLAN PCP/DEI can be enabled per ingress port (via SPCP bit in PCE_PCTRL_2). Traffic class mapping from CTAG PCP can be enabled per ingress port (via PCP bit in PCE_PCTRL_2).
  - If the packet contains no STAG it can be configured to choose other methods for the traffic class classification (e.g., DSCP, CTAG PCP or ingress port).
  - If the packet contains no CTAG it can be configured to choose other methods for the traffic class classification (e.g., DSCP, STAG PCP&DEI or ingress port).
- **DSCP (Differentiated Services Code Point):** CoS is based on the Differentiated code point placed in the IP header of the incoming packet. The Gigabit Ethernet Switch Macro provides a global DSCP to traffic class assignment table. In this table any IP DSCP 6 bits combination is mapped to an appropriate class of service.
  - Note: If the packet contains no IP header it can be configured to choose other methods for the traffic class classification (e.g.CTAG PCP, STAG PCP/DEI or default traffic class).
  - If more than one classification methods are enabled, the highest traffic class mapped from different fields is selected.
- **Traffic Flow:** Any combination of the following traffic flow parameters entered to the Traffic Flow table can be used to assign the class of service. When a flow with an appropriate traffic class assignment action matches for a given ingress frame, this assignment has higher priority over the default CoS assignments. In this case the traffic class will be assigned based on the traffic flow rule.
  - Destination MAC address (with nibble-mask support)
  - Source MAC address (with nibble-mask support)
  - STAG VLAN ID (with nibble mask or range support)
  - CTAG VLAN ID (with nibble mask or range support)
  - Ethertype
  - IP protocol and parser flags
  - IP packet length or length range
  - STAG PCP & DEI
  - CTAG PCP
  - IP DSCP
  - Source IP address (with nibble-mask support)
  - Destination IP address (with nibble-mask support)
  - Application field 1, for example, Source TCP/UDP port (with range support)
  - Application field 2, for example, Destination TCP/UDP (with range support)

Up to 16 different traffic classes can be supported and mapped individually to appropriate QoS queue. See **Chapter 3.7.5.3** for more details regarding queue mapping. **Figure 31** describes the traffic class assignment selection order vs configuration.

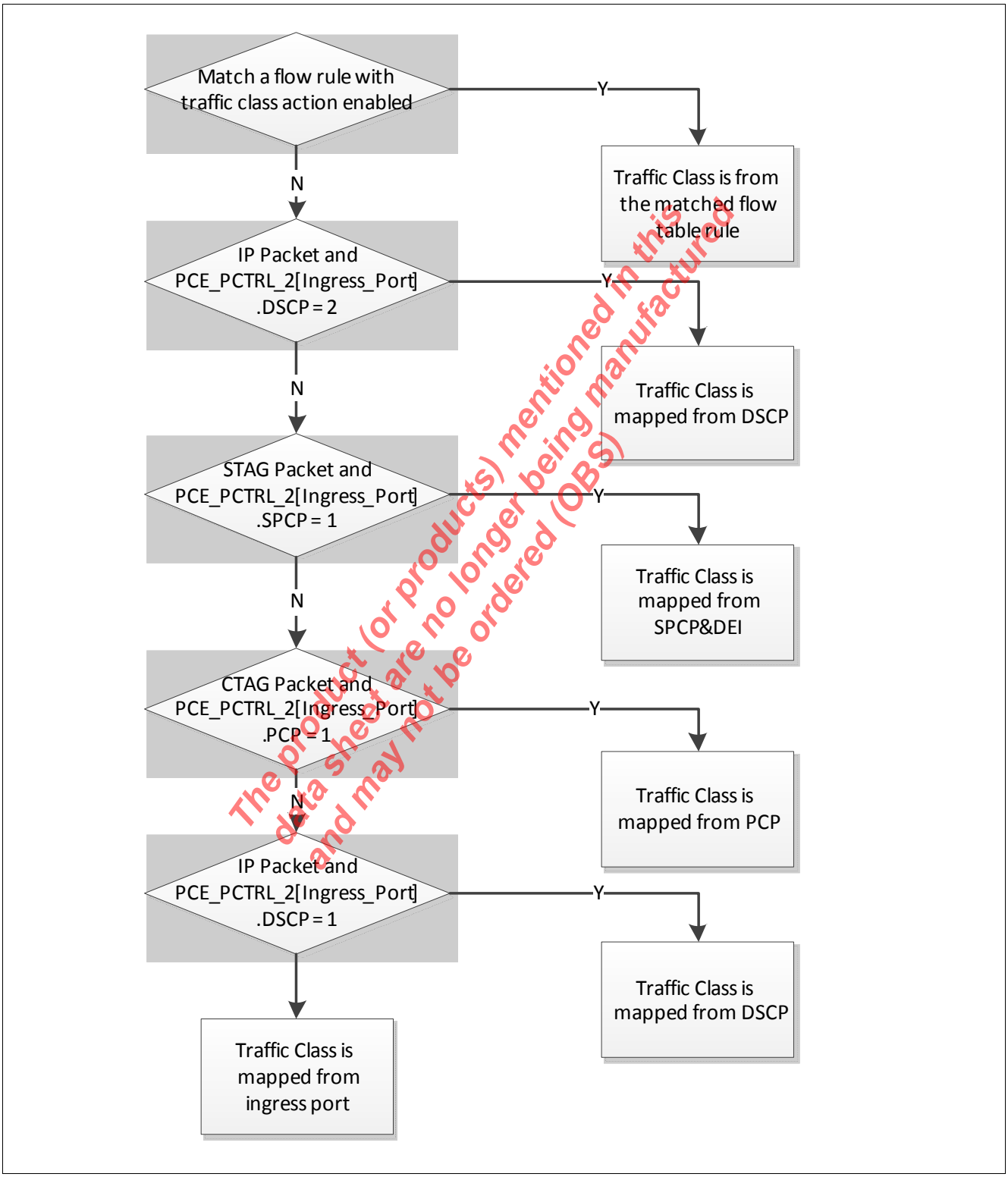


Figure 31 Traffic Class Assignment

3.7.5.2 Remarking Function

The Gigabit Ethernet Switch Macro supports the remarking of the DSCP, (re)generation of STAG PCP&DEI, and (re)generation of CTAG PCP in the egress frame. The modification of the code points in the outgoing packets is based on both traffic class and egress port. The Gigabit Ethernet Switch Macro provides a dedicated mapping table to assign the new DSCP, CTAG PCP and STAG PCP&DEI according to according to traffic class as well as egress port. **Figure 32** shows how DSCP (including drop precedence), CTAG PCP, STAG PCP and STAG DEI can be remarked based on any of the class of service assignment parameter.

Remarking can be enabled per ingress port. Remarking can also be disabled per egress port and per code point. In addition, the Traffic Flow table allows to disable remarking explicitly for certain flows.

Figure 33 shows the remarking DSCP flow diagram. **Figure 34** shows the remarking Drop Precedence flow diagram. **Figure 35** shows the STAP PCP remarking flow diagram. **Figure 36** shows the STAP DEI remarking flow diagram. **Figure 37** shows the CTAG PCP remarking flow diagram.

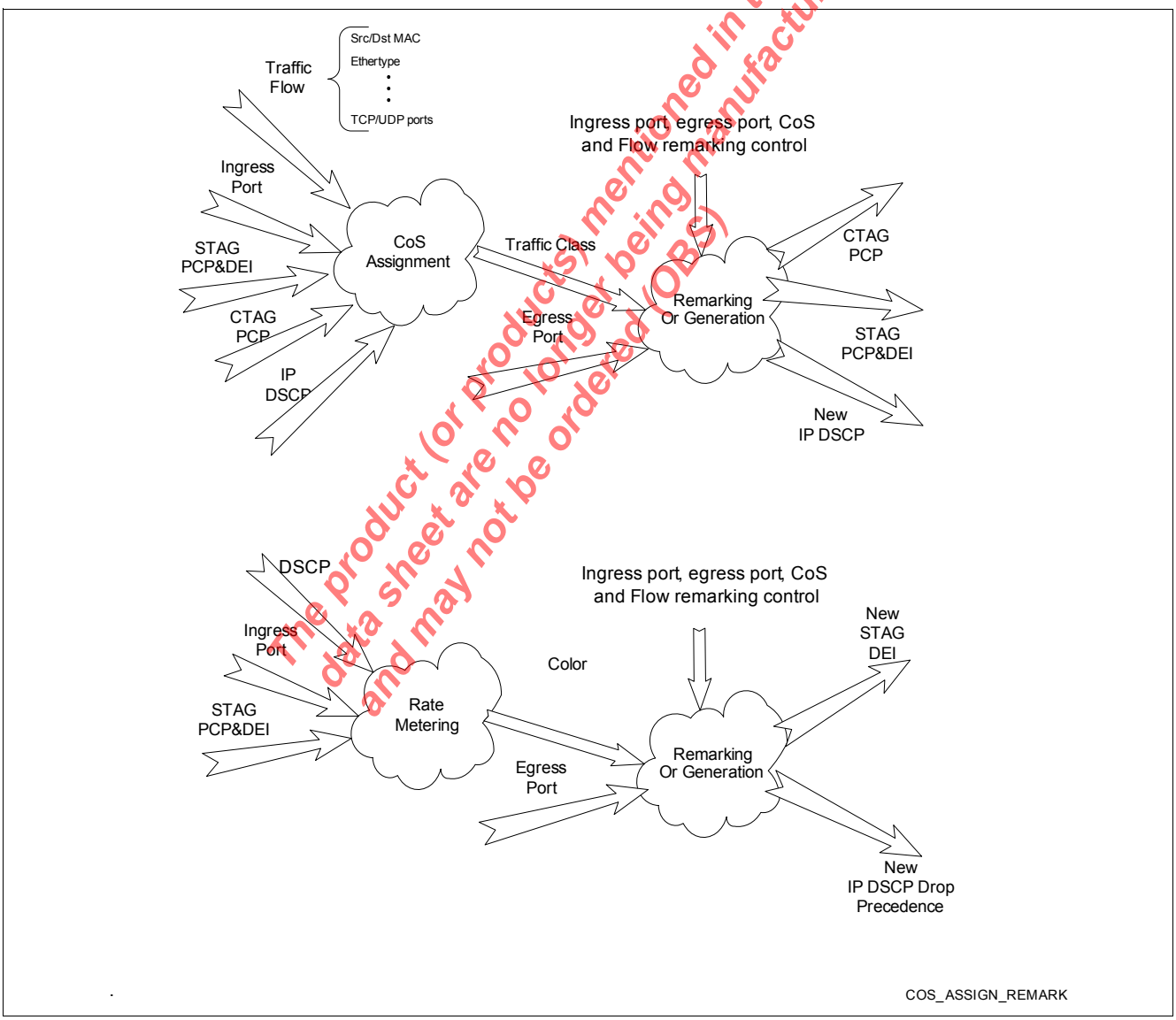


Figure 32 PCP/DSCP /DEI Remarking

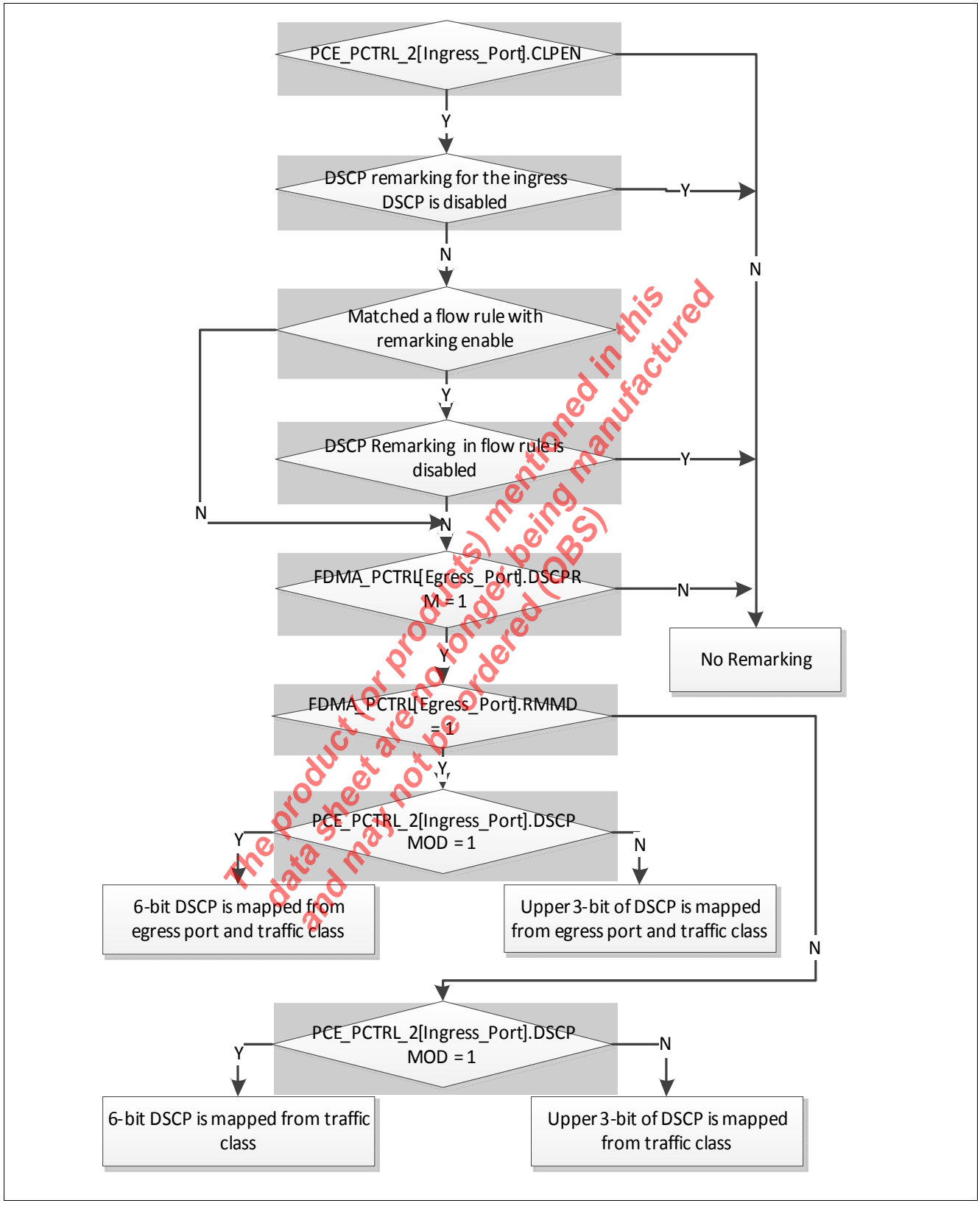


Figure 33 DSCP Remarking Flow Diagram

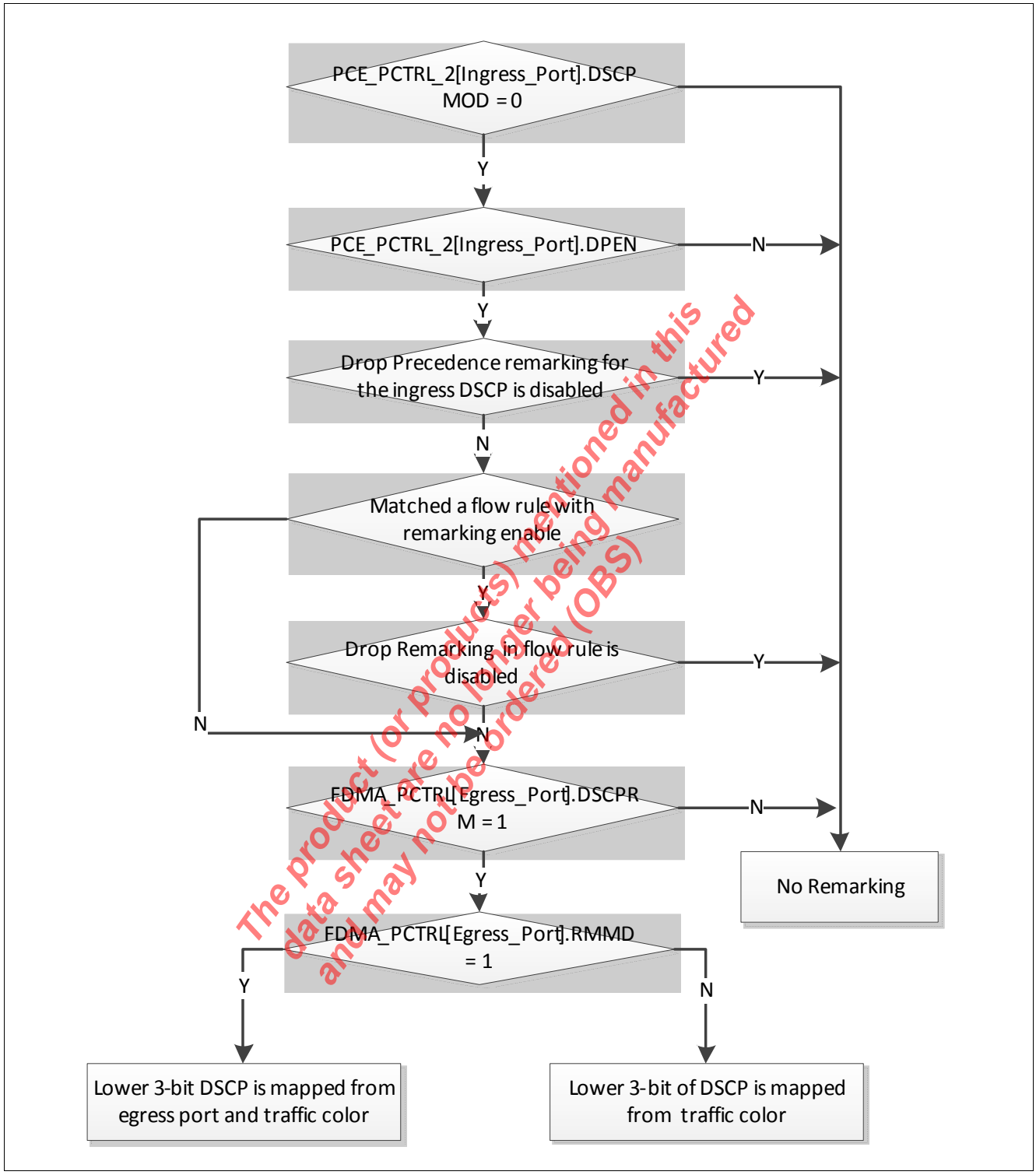


Figure 34 Drop Precedence Remarking Flow Diagram

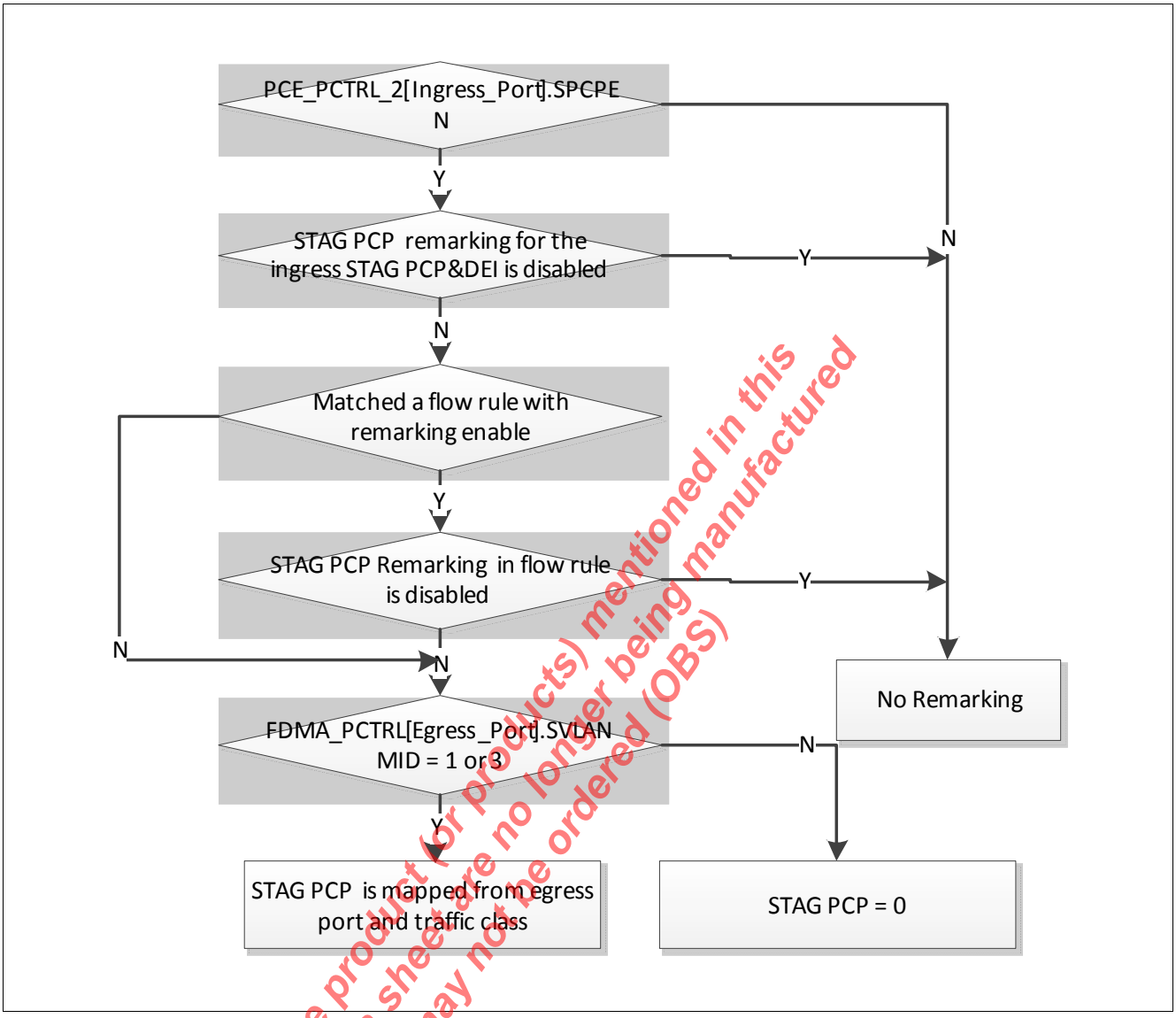


Figure 35 STAG PCP Remarking Flow Diagram

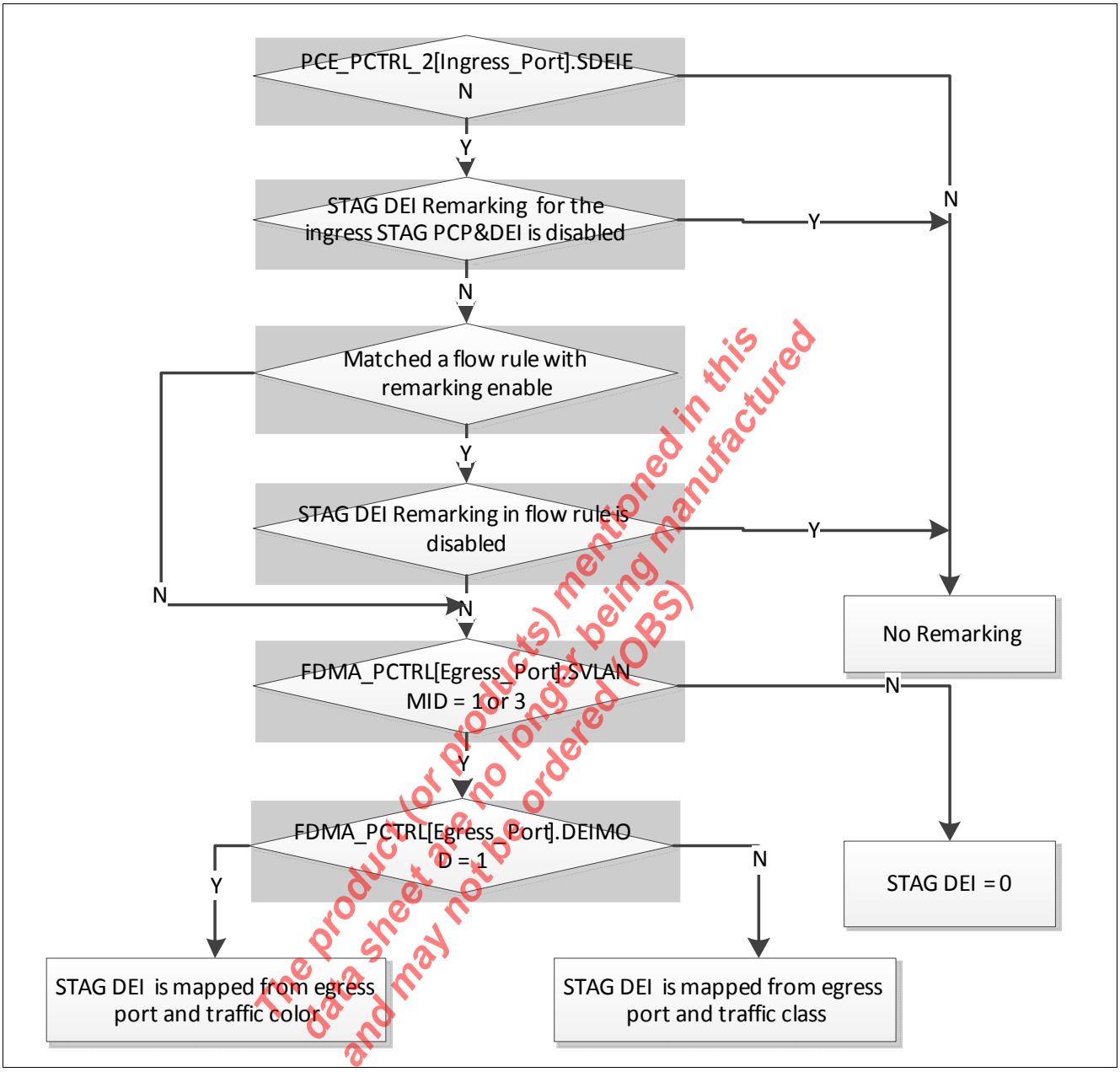


Figure 36 STAG DEI Remarking Flow Diagram

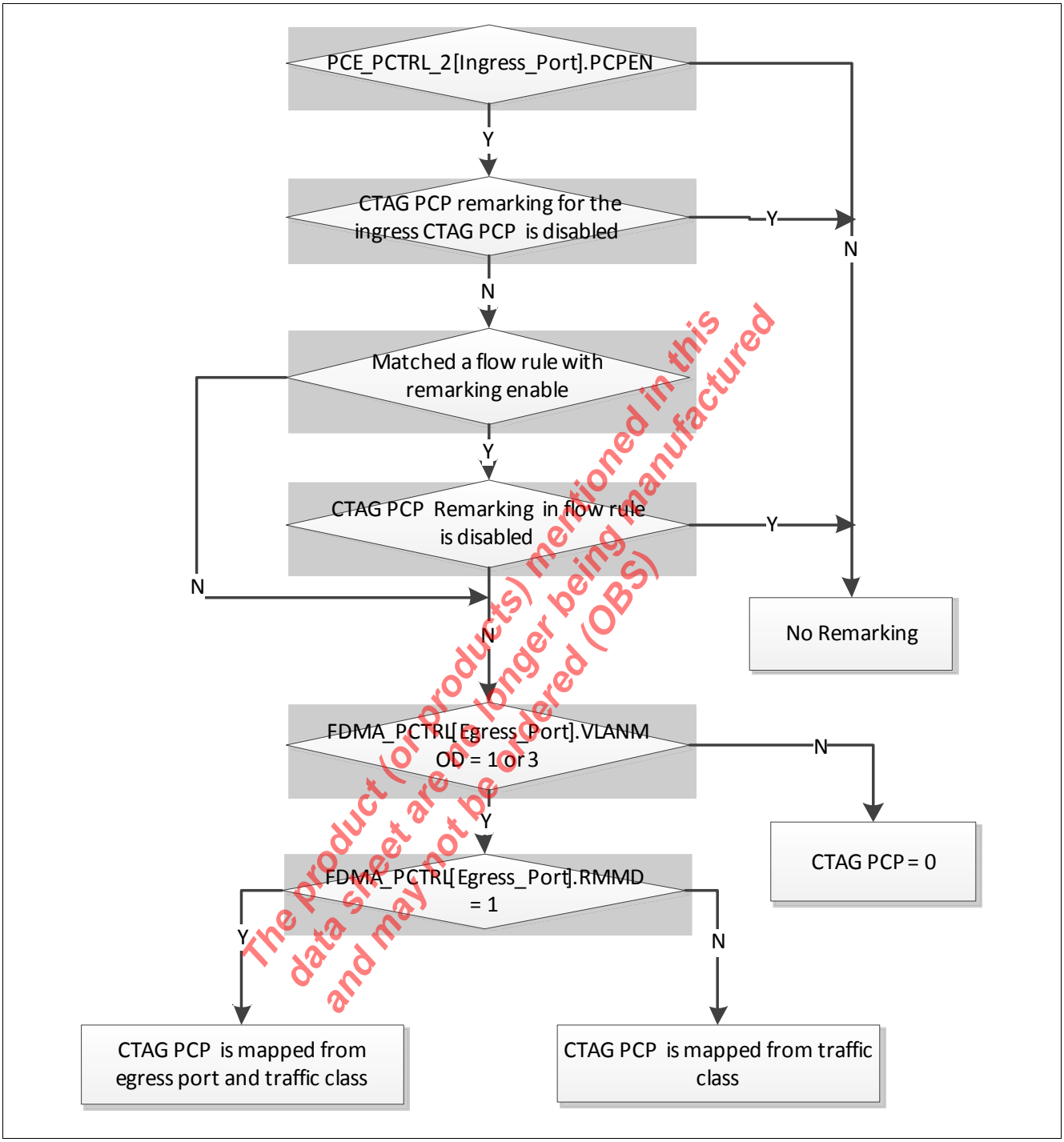


Figure 37 CTAG PCP Remarking Flow Diagram

3.7.5.3 Queue Mapping

The Gigabit Ethernet Switch Macro supports 32 egress QoS queues that can be flexibly assigned to egress ports and traffic classes. The sections below provide more details on the queue mapping functionality.

Queue to Port Mapping

Per default egress port 0 to 7 has 4 Quality of Service queues. For certain applications it might be desired to have a different number of QoS queues on specific ports. The Gigabit Ethernet Switch Macro supports flexible queue

to port mapping. Each queue from the 32 queue pool can be assigned to any port. This way the default configuration can be changed so that one port, for example, contains 8 queues. Please note, in certain configurations there might be unassigned (unused) queues. However, the overall number of 32 queues for all ports cannot be exceeded. In addition, an active port must have at least one queue and can have maximum 16 queues assigned to it.

Traffic Class to Queue Mapping

Incoming frames are being stored in the appropriate queues based on the traffic class assignment. The mapping of the traffic class to queue is specified in a dedicated queue mapping table per egress port. The mapping of the traffic classes to queues is related to the number of the queues available on certain port. For example, on one port 4 traffic classes could be mapped to 4 different queues, on another port all 4 traffic classes could be mapped to one single queue of this port.

3.7.5.4 Rate Metering

The Gigabit Ethernet Switch Macro supports 16 instances of a single rate Three Color Meter (srTCM). Each meter can measure the rate of a packet stream and mark the packets either green, yellow, or red. When there is no metering instance assigned to a traffic stream, this stream is considered to be green in the color-blind mode. In color-aware mode the stream is colored based on the drop-precedence encoded in the frame. See sections below for more details.

The color markings can be used later for policing in the active congestion management function, see Chapter 3.7.5.7 for more details. In addition the markings can be used to remark the drop precedence of the outgoing packet in the DSCP and STAG DEI.

Marking is based on a Committed Information Rate (CIR) and two associated burst sizes, a Committed Burst Size (CBS) and an Excess Burst Size (EBS). A packet is marked green if it doesn't exceed the CBS, yellow if it does exceed the CBS, but not the EBS, and red otherwise. Please note, in color-aware mode (see dedicated section below) the packet may already contain a color. In this case, for a yellow colored frame only the EBS is checked and if exceeded the packet becomes red. For packets received with a red color - the CBS/EBS plays no role, the packet remains red.

Only single meter instance can be assigned to measure the rate of a traffic flow.

The Gigabit Ethernet Switch Macro supports the following meter assignments:

- **Port:** A Meter can be assigned to the ingress or egress port or port pair, particularly:
  - Ingress port. The meter assigned to a specific ingress port. All packets received on that port are metered with the same meter instance.
  - Egress port. The meter assigned to a specific egress port. Any packets destined to that port are metered with the same meter instance. Please note, the multicast packets get metered if a meter is assigned to one of the destination ports.
  - Ingress-Egress port pair. The meter assigned to a specific packet route, from specific ingress port to a specific egress port.
- **Traffic Flow:** Any combination of the following traffic flow parameters entered to the Traffic Flow table can be used to assign the metering instances.
  - Destination MAC address (with nibble-mask support)
  - Source MAC address (with nibble-mask support)
  - STAG VLAN ID (with nibble mask or range support)
  - CTAG VLAN ID (with nibble mask or range support)
  - Ethertype
  - IP protocol and parser flags
  - IP packet length or length range
  - STAG PCP & DEI
  - CTAG PCP

  - IP DSCP
  - Source IP address (with nibble-mask support)
  - Destination IP address (with nibble-mask support)
  - Application field 1, for example, Source TCP/UDP port (with range support)
  - Application field 2, for example, Destination TCP/UDP (with range support)
- **Storm Control:** (see also **Chapter 3.7.5.10**) If storm control is enabled a meter can be assigned to
  - unknown unicast traffic
  - unknown multicast traffic
  - broadcast traffic

Figure 38 describes a metering algorithm of a single metering instance.

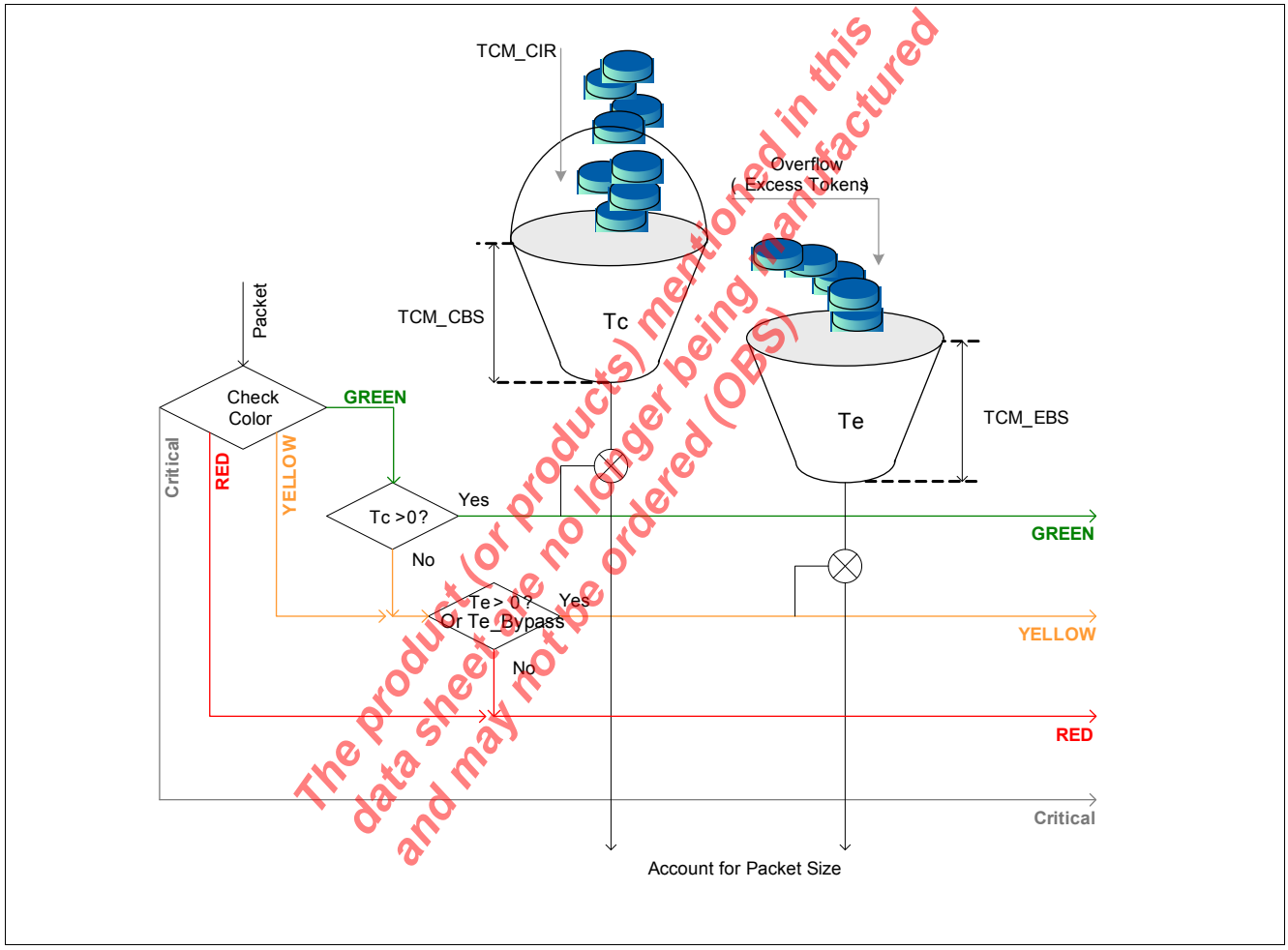


Figure 38 Metering Algorithm

Critical Frames

Frame can be classified as critical based on specific DSCP encoding in the appropriate DSCP mapping table or based on a rule configured in the Traffic Flow table. Critical frames bypass the metering instance and do not trigger the active congestion management function.

Color-aware/ Color-blind modes

The Gigabit Ethernet Switch Macro supports color-awareness modes to be configured per ingress port. In the color-aware mode, the meter assumes that some preceding entity has pre-colored the incoming packet stream so that each packet is either green, yellow, or red. The ingress color of the incoming frame is based on either DSCP

value or STAG PCP&DEI value. It is retrieved from the appropriate DSCP mapping table or STAG PCP&DEI mapping table. Non-IP and Non-STAG packets are treated as pre-colored to green.

In color-blind mode, all packets are treated as green.

DSCP Drop Precedence Remarking

It can be enabled by both ingress port and egress port configuration to reflect the metering results by replacing the lower 3 bits of the received DSCP field with the value of appropriate color decided by the metering instance for the received packet. The mapping of the color to the lower 3 bits of the DSCP can be configured per egress port. Please refer to **Chapter 3.7.5.2** for more details.

DEI (Re)generation

It can be enabled by both ingress port and egress port configuration to reflect the metering result by setting the STAG DEI field of the packet with the value of appropriate color decided by the metering instance for the received packet. The mapping of the color to the DEI can be configured per egress port. Please refer to **Chapter 3.7.5.2** for more details.

Metering based Flow Control

When a metering instance is assigned to an ingress port, the conformance rate of this port can be used for triggering flow control. In other words, once the tokens in Tc bucket is below 8000_H, the start flow control can be generated on that port. When the tokens in Tc bucket is more than TCM_EBS*64, the stop flow control can be generated on that port.

Please note, to achieve that functionality the assigned meter instance number must correspond to the respective ingress port. All ingress packets from the rate flow control enabled port must be green color.

Conforming status for each port are readable via MTEBP bit in PCE_TCM_STAT register. Any change of conforming status can trigger the interrupt.

3.7.5.5 Rate Shaping

The Gigabit Ethernet Switch Macro supports 32 instances of rate shaper. Each rate shaper can be configured to Token Bucket mode or Credit Rate shaper mode. Each shaper mode can be configured via RSMOD bit in RS_CTRL. Each shaper can measure the rate of an egress queue and prevent the queues which exceeded the configured rate from being scheduled for the next packet transmission. Shaping is based on a Committed Information Rate (CIR) and an associated Committed Burst Size (CBS). A queue can be selected for transmission only if it doesn't exceed the CBS for a given CIR.

Up to two shaping instances can be assigned to measure the egress rate of a specific queue or number of queues. Two shapers are typically being assigned to measure the peak and committed rate and typically have different CIR settings. Any number of queues can share the same shaping instance, in this case the committed rate and the burst size are shared among the assigned queues.

If there is no shaper assigned to a queue, the queue rate is not monitored. It is recommended to assign a shaper for queues with high scheduling weights or strict priority queues. See **Chapter 3.7.5.6** for more details regarding queue scheduling.

3.7.5.6 Queue Scheduling

The scheduling function determines which queue is allowed to emit a packet. Queue scheduling is done after the rate shaping. The Gigabit Ethernet Switch Macro supports the following scheduling types for each one of the 32 egress QoS queues:

- **Weighted Fair Queueing (WFQ):** For a given port, packets in the WFQ queues will be scheduled for transmission in accordance with their configured weight. The weight represents a ratio for transmission. The

higher the weight of one queue compared to an other, the more often this queue will be scheduled for transmission.
  – For example, a queue with weight 4000 will be served twice more often than the queue with weight 2000.
- **Strict High Priority:** For a given port, packets in the strict high priority queue will be scheduled for transmission before any packet in the WFQ queue. If there are multiple strict high priority queues configured for a port, the queues with a higher physical number will be scheduled first.
- **Strict Low Priority:** For a given port, packets in the strict low priority queue will be scheduled for transmission after any packet in the WFQ queue. If there are multiple strict low priority queues configured for a port, the queues with a higher physical number will be scheduled first.

3.7.5.7 Congestion Management

The Gigabit Ethernet Switch Macro provides protection for the internal buffer from congestion and overflow.

If the shared buffer is fully occupied and doesn't have enough resources to receive any new frame, the incoming frames on all ports will be discarded, until the congestion condition is relieved.

In addition, the Gigabit Ethernet Switch Macro provides two segment thresholds per color globally, per color per each egress port and per color per each egress queue. Based on the configured thresholds and the global, port or queue segment filling level a decision is made for every incoming packet, whether the packet with a given color can be enqueued or not. This protection mechanism is called Active Congestion Management (ACM).

The color of the packets is decided based on the conformance rate in the metering instance (see **Chapter 3.7.5.4**). The thresholds are checked with accordance to the incoming packet color. e.g., red thresholds for red colored packets, yellow for yellow and green for green.

Gigabit Ethernet Switch Macro is able to reserve buffer per egress queue. This allows the protection of queues against congestion caused by other queues and ports. It provides a minimum buffer guarantee for each queue. A green frame can bypass ACM and is always accepted by the queue if the reserved buffer threshold of the queue is not exceeded.

Critical frames bypass the ACM and will be enqueued regardless of the filling level. Critical frames will not be enqueued only in case of buffer full event.

ACM function discards the frames early (before the buffer full event) with certain drop probability. ACM thresholds provide the following functionality:

- MIN Threshold. If the filling level of the queue is below this threshold (excluding the threshold value), the packet with the appropriate color is not discarded and will be enqueued.
- MAX Threshold. If the filling level of the queue is above this threshold (excluding the threshold value), the packet with the appropriate color is discarded.
- ½(MAX-MIN) Threshold. when filling level of the queue is between the MIN and MAX thresholds, the packet is discarded with certain probability. The drop probability profile can be selected globally between 25%, 50% and 75%. When the filling level is below half the distance between MIN and MAX thresholds, the packet is discarded with lower probability (P_{min}), when the filling level is above half the distance between MIN and MAX thresholds, the packet is discarded with higher probability (P_{max}). Specifically, the following drop probability profiles can be selected globally:
  – P0: P_{min} = 25%, P_{max} = 75% (default).
  – P1: P_{min} = 25%, P_{max} = 50%.
  – P2: P_{min} = 50%, P_{max} = 50%.
  – P3: P_{min} = 50%, P_{max} = 75%.

Please note, when MIN = MAX, the drop probability changes from 0% to 100% at once.

Figure 39 shows drop probability as a function of queue filling level and configured thresholds.

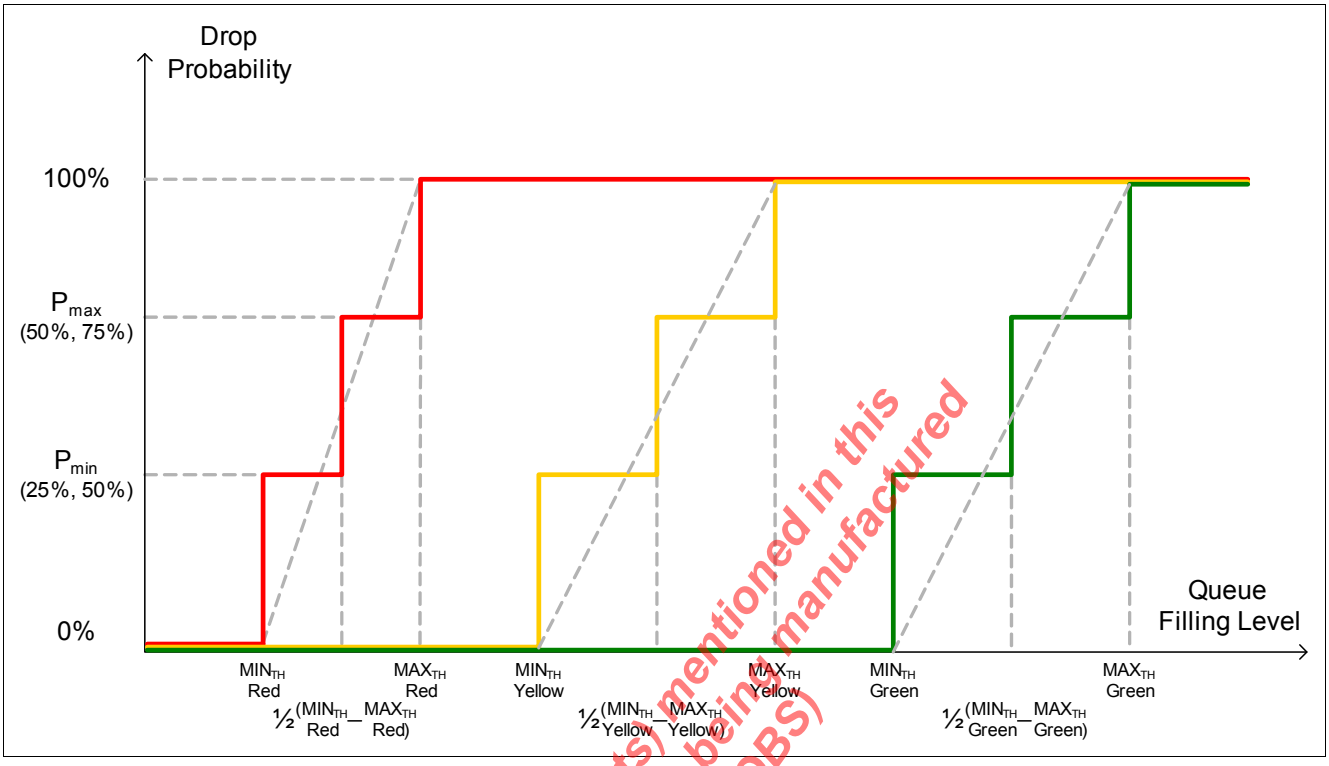


Figure 39 Drop Precedence Thresholds

Note: The thresholds for "Red" frames shown in the figure are below the threshold for "Yellow" frames and the thresholds for "Yellow" are below the thresholds for "Green" frames. This is how it would be usually configured in a real application scenarios. The thresholds can be configured MIN_{TH}=MAX_{TH}, in this case the frames are dropped as soon as they pass the drop threshold.

3.7.5.8 Ingress Port Congestion Based Flow Control

Flow control is activated when the ingress port local buffer congestion level exceeds a programmable local threshold (via SDMA_PFCTHR9 of each port) and deactivated when the local buffer congestion level drops below a programmable local threshold (via SDMA_PFCTHR8 of each port). The flow control applies to each port individually.

All ingress port congestion status are readable via SDMA_CGNBP register. Any change of congestion status can trigger the interrupt.

3.7.5.9 Overview of the Resource Protection Mechanism

The Gigabit Ethernet Switch Macro provides several mechanism to protects its limited resources. The limited resources are:

- number of segments (total 512 segments)
- number of packet pointers (total 1024 pointers)

The limitation can be on different levels:

- Global Packet Pointers Usage
- Global Shared Segment Buffer Usage
- Ingress Port Shared Segment Buffer Usage
- Egress Port Shared Segment Buffer Usage
- Egress Queue Shared Segment Buffer Usage

The limiting mechanisms are:

- Flow Control
- Buffer Reservation
- Tail Drop
- WRED

Resource Protection

One method to protect the GSWIP from running out of resources is by issuing Flow Control. Several thresholds are provided.

There are three level flow control thresholds. When any one of the start flow control conditions below is met, start flow control is triggered on a port. When all the stop flow control conditions below are met, stop flow control is triggered on a port.

- Flow control based on global buffer filling level
- Flow control based on ingress port buffer filling level
- Flow control based on ingress port metering result

Flow Control can be used together with the WRED thresholds. In this case the Flow Control thresholds and the WRED thresholds have to be coordinated. With WRED it is possible to configure a global color threshold, per port per color threshold or per queue per color threshold for red/yellow/green packets. If the max threshold is exceeded the frame is dropped. Filling levels between the min threshold and max threshold are dropped with a global configurable drop probability. Filling levels below the min threshold do not result in a drop. WRED can be used to avoid a situation where one queue uses up all the resources and affect the traffic on other queues. Typically a system is configured with a certain oversubscription which gives each queue enough resources to operate in a bursty environment but the situation that ports affect each other can not be avoided.

If frame drops shall be avoided the only possibility is to use Flow Control. Flow control threshold should be lower than the WRED and tail drop threshold.

Critical frames are still accepted by WRED even if the thresholds are exceeded.

Green frames are still accepted by WRED if the egress queue buffer usage is below the reserve buffer threshold.

Table 34 Resource Protection Options

Level	Mechanism	Resource	Number of Thresholds	Granularity	Register (default values)
Global Packet Pointer Usage	Flow Control	Packet pointers	1 (THR7)	Global	SDMA_FCTHR7(MAX)
	Tail Drop	Packet pointers	3 (one per color)	Global per color	BM_DROP_GTH_0 (MAX) red BM_DROP_GTH_1 (MAX) yellow BM_DROP_GTH_2 (MAX) green

Table 34 Resource Protection Options (cont'd)

Level	Mechanism	Resource	Number of Thresholds	Granularity	Register (default values)
Global Shared Segment Buffer Usage	Flow Control	Segments	4 (THR1-4)	Global	SDMA_FCTHR1 (0x82) SDMA_FCTHR2 (0xAC) SDMA_FCTHR3 (0xAC) SDMA_FCTHR4 (0xAC)
	Tail Drop	Segments	2 (THR5-6)	Global	SDMA_FCTHR5 (MAX) SDMA_FCTHR6 (MAX)
	WRED[1) 2)]	Segments	6 (two per color)	Global per color	BM_WRED_RTH_0 (MAX) BM_WRED_RTH_1 (MAX) BM_WRED_YTH_0 (MAX) BM_WRED_YTH_1 (MAX) BM_WRED_GTH_0 (MAX) BM_WRED_GTH_0 (MAX)
Ingress Port Shared Segment Buffer Usage	Flow Control	Segments	Two per port	Per ingress port	SDMA_PFCTH8 (MAX) SDMA_PFCTH9 (MAX)
Egress Port Shared Segment Buffer Usage	WRED	Segments	Two per port per color	Per egress port and per color	BM_PWRED_RTH_0 (MAX) BM_PWRED_RTH_1 (MAX) BM_PWRED_YTH_0 (MAX) BM_PWRED_YTH_1 (MAX) BM_PWRED_GTH_0 (MAX) BM_PWRED_GTH_0 (MAX)
Queue	Buffer Reservation	Segments	One per queue	Per queue	PQM Context Table • reservation threshold (0)
	WRED	Segments	Two per queue per color	Per queue and per color	PQM Context Table • red max threshold (0x50) • red min threshold (0x50) • yellow max threshold (0x50) • yellow min threshold (0x50) • green max threshold (0x50) • green min threshold (0x50)

1) The drop probability can only be configured globally BM_QUEUE_GCTRL.DPROB (00 => Pmin = 25%, Pmax = 75%).

2) Tail Drop can be realized by setting the min/max thresholds equal.

ACM and Flow Control

ACM and Flow control can be configured individually. Typically the two features are used exclusively.

- ACM is used to avoid that a single queue can use up all the resources. If a limit is exceeded additional frames to this queue are dropped. Frame switching between other ports is still possible.
- Flow Control is used to avoid frame drops. Before the global resource is used up the peers are informed to stop frame transmission.
- With buffer reservation and suitable ACM WRED threshold, non-congested queues are protected and do not stopped by congested queues.

3.7.5.10 Storm Control

The Gigabit Ethernet Switch Macro supports a broadcast storm control function. Broadcast storm is defined as an excessive amount of broadcast, multicast, or unknown unicast Ethernet frames that are received on a switch port. Due to the massive replication of data frames, broadcast storm can significantly degrade the system performance. Broadcast storm can also be a form of Denial-of-Service (DoS) attack.

The storm control function can effectively police specific traffic type and protect the resources from being flooded by the broadcast traffic.

The selected metering instance is configured to the required policed rate of the broadcast storm. The following traffic types can be selected for the storm control function:

- Broadcast frames
- Unknown Multicast frames
- Unknown Unicast frames

When the rate of the selected frame types exceeds the rate configured in the meter instance, the frames marked as yellow or red. When the active congestion management thresholds configured appropriately, the storm frames will be discarded.

3.7.6 Flow Classification Function

The Gigabit Ethernet Switch Macro includes a powerful packet classification engine that performs multi-field classification based on up to 64 programmable rules.

Traffic Flow Table

Traffic Flow table contains up to 64 programmable rules. Rules can be configured per ingress port but can also be shared between ports. Each rule consists of a pattern and action sections, as depicted in **Figure 40**. A Pattern specifies certain combination of packet header fields. The Parser extracts the packet header fields from the received packet and provides them to the Traffic Flow table. If a pattern matches, the enabled actions apply. The pattern search continues until all actions are satisfied. This allows the definition of multiple pattern for different actions. Each action can be specifically enabled or disabled for a given pattern.

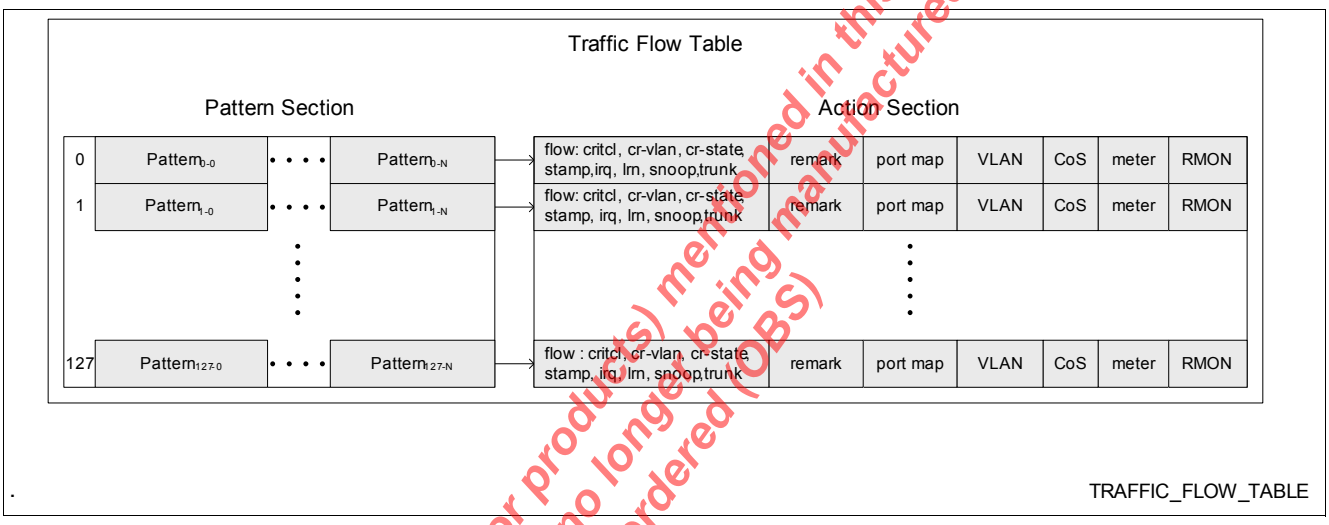


Figure 40 Traffic Flow Table

Rules location in the table defines their priority, rule entries with lower index number have higher priority. The Traffic Flow table is searched in a following way:

- **Pattern Match:** Pattern row is considered matched if all the fields in the pattern have been matched or configured to be ignored (not enabled). If a pattern row matches, the appropriate action row is checked for that pattern. Please note, multiple pattern rows in the table might match the search, however, only the first pattern in the table that is matched for certain action is applied.
- **Action Match:**
  Each action in the action row can be enabled or disabled for certain pattern row match. If the action is enabled and the pattern row matched, this action will be applied for the classified packet. The search in the table terminates only if all the actions in the action section have been found. If not, the search continues for the next pattern match and the corresponding action match. An additional option is to enable the action and to select a default behavior for that action, i.e., the search for another enabled action is terminated. Please note, for a given packet classification only one pattern may match one specific action, however, multiple patterns may match multiple different actions, i.e., the action section is searched independently for each action type. See the following examples for more clarification:
  – 1st example: Consider two rules added to the table, one has a source MAC address in the pattern and a CoS assignment in the action section. Another rule (at different index) has an Ethertype in the pattern section and the action is a VLAN group association. If an incoming frame matches both patterns, both actions will be applied for this frame.
  – 2nd example: Consider a similar scenario as in the first example, whereas the only the action is VLAN group association for both pattern rows. In this case only the rule with the lowest index will be applied, i.e., similar action is executed with priority of the rule depending on the location in the table.

Pattern Section

The pattern section contains the packet header fields and other parameters that can identify the incoming packet flow. Specifically, the following pattern fields are supported:

- Ingress port number. The parameter compared with the ingress port number of the incoming packet.
- Source MAC Address or part of the MAC Address specified by a programmable nibble mask[1)].
- Destination MAC Address or part of the MAC Address specified by a programmable nibble mask[1)].
- STAG VID or part of the STAG VID specified by a programmable nibble mask or a range.
- CTAG VID or part of the CTAG VID specified by a programmable nibble mask or a range.
- Ethernet type.
- IP Protocol and Parser Flags.
- PPPoE Session ID.
- IP Packet Length or length range.
- Source IP Address or part of the IP Address specified by a programmable nibble mask[1)].
- Destination IP Address or part of the IP Address specified by a programmable nibble mask[1)].
- CTAG PCP Code. This parameter is directly compared with the PCP code of the VLAN tag of the received frame. When the received frame contains no VLAN/Priority Tag the parameter will not match.
- STAG PCP&DEI. This parameter is directly compared with the PCP&DEI of the VLAN tag of the received frame. When the received frame contains no VLAN/Priority Tag the parameter will not match.
- DSCP Code. This parameter compared directly with the DSCP code in the IP header. When the received packet contains no IP header the parameter will not match.
- The first 4 bytes of the packet content following the IP header or first 4 bytes of packet content following the Ethertype for non IP and non PPPoE packets or first 4 bytes of packet content following the PPPoE header for non IP and PPPoE packets. For TCP/UDP the 4 bytes following the IP header are the TCP/UDP source and destination ports. Any part of this content can be masked-out by a programmable nibble mask[1)].

Each field in pattern section can be enabled or disabled for the search. When parameter is disabled, corresponding pattern is not compared. The pattern is considered to be matched by default for any value of the corresponding packet field.

Note: If an IP packet is carried in a PPPoE frame, the Ethertype is 0x8864 but there is no explicit Parser Flag for IP_indication and no PPP_protocol field that shows that the PPPoE carried IP. A rule might want to forward all IPoPPPoE to a specific port. If there would be a PPP_protocol field this rule could be defined by the a match on Ethertype=0x8864 AND PPP_protocol=0x0021. Since there is no PPP_protocol field such a rule can be defined by configuring an "always match" entry in the IP address table (an entry with all masks active). If there is an IP in the PPPoE frame the "always match" entry matches, if there is no IP in the PPPoE frame the IP address table is not searched and the result is a "no_match" indication. With this match indications and the Ethertype=0x8864 the IP_indication flag and PPP_protocol field is not needed.

Actions Section

Action section contains the actions that can be applied to an incoming packet. Specifically, the following actions are supported:

- **Port Bitmap (used as Port Map/Port Member/Flow_ID):** The received packet (packet flow) can be redirected to a single or multiple egress ports based on a pattern match. Redirection includes the packet discard option when the packet is redirected to the NULL port (all zero port map). Based on the port bitmap multiplexing control in the action, this field is also used as STAG port member which identifies the broadcast domain. The broadcast domain of the received packet will be restricted according to the this field on top of the other filtering function. If the Flow_ID action is configured, the field holds the Flow_ID instead of the port map or port member. The Flow_ID can be written into the egress special tag.

1) Note: mask resolution is nibble, i.e., every 4 bits can be masked out.

- **Traffic Class Assignment (CoS):** Traffic class of the received packet can be assigned or changed from a default assignment based on the pattern match.
- **VLAN Assignment:** VLAN classification of the received packet can be assigned or changed from a default assignment based on the pattern match. Both service VLAN tag and customer VLAN tag are supported.
- **Metering Assignment:** A Metering instance can be assigned or changed from a default assignment based on the pattern match.
- **RMON Assignment:** Dedicated packet counters can be assigned to a specific flow. The counters are incremented each time the pattern is matched.
- **Flow Actions:** The following additional flow actions can be assigned only in the flow table (by default these actions are disabled):
  - Cross VLAN packet indication. Certain packet can be identified as cross VLAN. VLAN filtering rules will be ignored for these packets, e.g, cross VLAN packets may cross VLAN boundaries.
  - Cross state packet indication. Certain packet can be configured to ignore the port state of the ingress or egress port. These packets will be forwarded even when all the “regular“ frames are discarded.
  - Critical packet indication. Packets identified as critical will bypass active congestion management function (ACM) and will be enqueued to a certain queue regardless of the filling level of that queue.
  - Time stamping. Ingress/egress time stamp can be recorded for packets identified by matched pattern. The time stamps are sampled during packet reception/transmission and can be retrieved by the management action.
  - Interrupt request assertion. An external interrupt can be asserted based on a pattern match.
  - Learning action. Learning function can be forced to be enabled or disabled.
  - Snooping action. A specific IGMP snooping action can be selected for the IGMP messages. Note, relevant only for the IGMP hardware based snooping.
  - Flow_ID action. A Flow indication can be configured which is written into the egress Special Tag (see **Chapter 3.7.7.5**).
  - Forwarding Multiplexing Control. These control signals select the appropriate Port-Map in Forwarding Classification.
  - Port Bitmap Multiplexing Control. This control signal select the port bitmap mode: used as STAG Port-Map or Port-Member in Forwarding Classification.
  - Trunking Link Selection. The destination trunking link can be assigned or changed from a default assignment based on the pattern match.

Each single action in the action section can be enabled or disabled for the search. When an action is disabled, the table search continues until another pattern matches for this action. When no other pattern matches, the corresponding action is not applied.

3.7.7 Operation, Administration, and Management Functions

This chapter summarizes the functions that are provided to control and monitor the data traffic through the switch.

3.7.7.1 Monitoring Counters

Multiple counters are provided per port to monitor incoming and outgoing data traffic as well as errors or special events. Each port provides the same set of counters. There are two main groups of counters, which are a set of standard Ethernet counters (aka “RMON Counters”) and a group of counters that can be assigned to programmable traffic flows. See sections below for more details.

Standard (RMON) Counters

The Gigabit Ethernet Switch Macro supports 34 standard frame counters of 32-bit each and 3 byte counters of 64-bit each. The counters are not cleared on read, instead complete set of port counters can be cleared by the appropriate management action. It can be configured if the 8 byte special tag is excluded from the byte counters. See **Table 35** for the list of standard RMON counters.

Table 35 Standard RMON Counters

Short Name	Long Name	Description
Receive Counters		
nRxUnicastPkts	Received Unicast Ethernet frames	Counts the total number of valid[1)] Unicast Ethernet frames received on the ingress port.
nRxTotalPkts	Received Total Ethernet frames or Broadcast Ethernet frames	Counts the total number of valid[1)] Ethernet frames or total number of valid Broadcast Ethernet frames received on the ingress port. The mode is configurable via BCAST_CNT bit in BM_RMON_CTRL
nRxMulticastPkts	Received Multicast Ethernet frames	Counts the total number of valid[1)] Multicast Ethernet frames (not including Broadcast frames) received on the ingress port.
nRxFCSErrorPkts	Received CRC errors	Counts the total number of Ethernet frames that have been received with an FCS error.
nRxUnderSizeGoodPkts	Received good undersized Ethernet frames	Counts the total number of Ethernet frames received with Undersize Error but with correct FCS.
nRxUnderSizeErrorPkts	Received bad undersized Ethernet frames	Counts the total number of Ethernet frames received with Undersize Error and bad FCS.
nRxOversizeGoodPkts	Received good oversized Ethernet frames	Counts the total number of Ethernet frames received with Oversize Error but with correct FCS.
nRxOversizeErrorPkts	Received bad oversized Ethernet frames	Counts the total number of Ethernet frames received with Oversize Error and bad FCS.

Table 35 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nRxGoodPausePkts	Received good Pause Ethernet frames	Counts the total number of received valid[1)] Ethernet Pause frames.
nRxAlignErrorPkts	Received alignment errors	Counts the total number of packets received with a • alignment error or • length errors or • phy_rx errors or • all errors of above The error which shall be counted can be configured globally. Error ignore flags are not considered (counting is done) only in the "all" case. An alignment error is specified as a non-integral number of octets.
nRx64BytePkts	Received frame size 64 byte	Counts the total number of valid[1)] Ethernet frames received with the minimum valid length of 64 byte.
nRx127BytePkts	Received frame size 65-127 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 65 to 127 byte.
nRx255BytePkts	Received frame size 128-255 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 128 to 255 byte.
nRx511BytePkts	Received frame size 256-511 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 256 to 511 byte.
nRx1023BytePkts	Received frame size 512-1023 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 512 to 1023 byte.
nRxMaxBytePkts	Received frame size larger than 1023 byte	Counts the total number of valid[1)] Ethernet frames received with a length of 1024 byte or more. *Note: If Jumbo frames are enabled on the related port, these frames are also included in this counter.*
nRxDroppedPkts	Receive dropped Ethernet frames	Counts the total number of frames discarded due to the lack of shared resources, i.e., in case of complete buffer congestion.
nRxFilteredPkts	Received filtered Ethernet frames	Counts the total number of Ethernet frames discarded due to a violation detected by the Classification Engine, i.e., frame filtering based on matched multifield classification rule.
nRxGoodBytes	Received good bytes	Total number of bytes received in valid[1)] Ethernet frames. This is a 64-bit counter.

Table 35 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nRxBadBytes	Received bad bytes	Total number of bytes received in invalid Ethernet frames. This is a 64-bit counter.
Transmit Counters		
nTxACMDiscardPkts	Transmit Queue ACM Discard frames	Counts the total number of packets discarded by the ACM mechanism (Active Congestion Management) due to exceeded thresholds on the egress QoS queues.
nTxUnicastPkts	Transmitted Unicast Ethernet frames	Counts the total number of Unicast Ethernet frames transmitted on the egress port.
nTxTotalPkts	Transmitted Total Ethernet frames or Broadcast Ethernet frames	Counts the total number of total frames or Broadcast frames transmitted on the egress port. The mode is configurable via BCAST_CNT bit in BM_RMON_CTRL.
nTxMulticastPkts	Transmitted Multicast Ethernet frames	Counts the total number of Multicast Ethernet frames (not including Broadcast frames) transmitted on the egress port.
nTx64BytePkts	Transmitted frame size 64 byte	Counts the total number of Ethernet frames transmitted with the minimum valid length of 64 byte.
nTx127BytePkts	Transmitted frame size 65-127 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 65 to 127 byte.
nTx255BytePkts	Transmitted frame size 128-255 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 128 to 255 byte.
nTx511BytePkts	Transmitted frame size 256-511 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 256 to 511 byte.
nTx1023BytePkts	Transmitted frame size 512-1023 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 512 to 1023 byte.
nTxMaxBytePkts	Transmitted frame size larger than 1023 byte	Counts the total number of Ethernet frames transmitted with a length of 1024 byte or more. *Note: If Jumbo frames are enabled on the related port, these frames are also included in this counter.*
nTxCollCount	Transmitted total collision number	Counts the total number of Ethernet frames transmitted on the egress port after any "Collision" event.
nTxSingleCollCount	Transmitted single collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Single Collision" event.

Table 35 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nTxMultCollCount	Transmitted multiple collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Multiple Collision" event.
nTxLateCollCount	Transmitted late collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Late Collision" event.
nTxExcessCollCount	Transmitted excessive collisions	Counts the total number of Ethernet frames transmitted on the egress port after an "Excessive Collision" event.
nTxPauseCount	Transmitted Pause frames	Counts the total number of "Pause" frames transmitted on the egress port.
nTxDroppedPkts	Transmit dropped frames	Counts the total number of packets discarded due to port disable, excess collision or late collision.
nTxGoodBytes	Transmitted good bytes	Total number of bytes transmitted in Ethernet frames. This is a 64-bit counter.

1) Every packet that is received without any reception error is considered to be valid. This includes Unicast, Multicast and Broadcast packets.

Traffic Flow Counters

There is a set of 24 packet-based counters available per port, where each can be assigned to a dedicated traffic flow, as specified in the Traffic Flow table. Each traffic flow is defined by an entry in the traffic flow table, counters are connected with a traffic flow in a flexible way. The counter number is entered as one of the table actions. See **Chapter 3.7.6** for more details.

3.7.7.2 Port Mirroring

The Gigabit Ethernet Switch Macro supports port monitoring to assist system debugging or enable software-controlled functionality. Data that is received on a selected port can be mirrored to another selected port (the monitoring port).

Mirroring Function

Mirroring means that the received frame is processed and forwarded as normal, but a copy of that frame is in addition sent to the monitoring port. The options given by the Port Mirroring function are:

- Copy data that is received on a selected port to the monitoring port.
- Copy data that is received on a selected group of ports to the monitoring port.
- Copy data that is transmitted on a selected port to the monitoring port.
- Copy data that is transmitted on a selected group of ports to the monitoring port.
- Copy data that is received or transmitted on a selected port to the monitoring port.
- Copy data that is received or transmitted on a selected group of ports to the monitoring port.

See figures below for illustration.

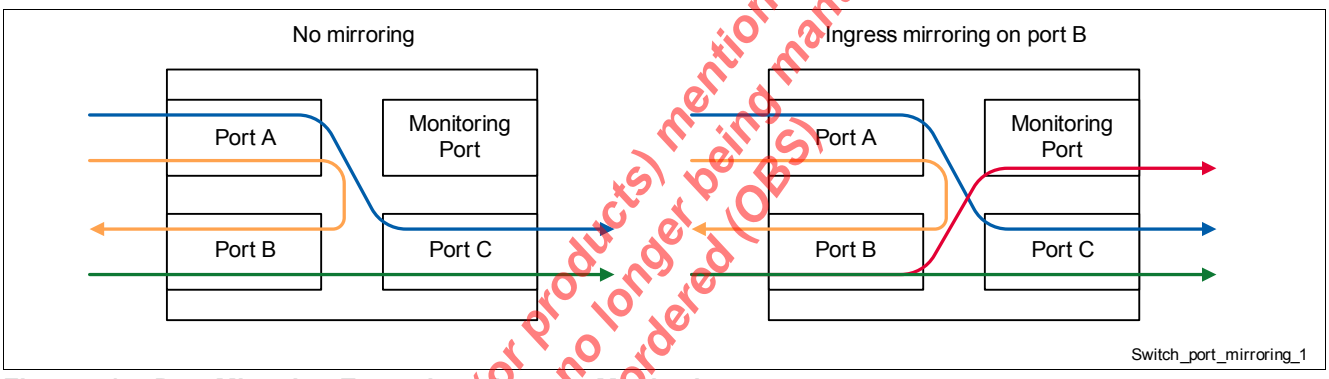


Figure 41 Port Mirroring Examples – Ingress Monitoring

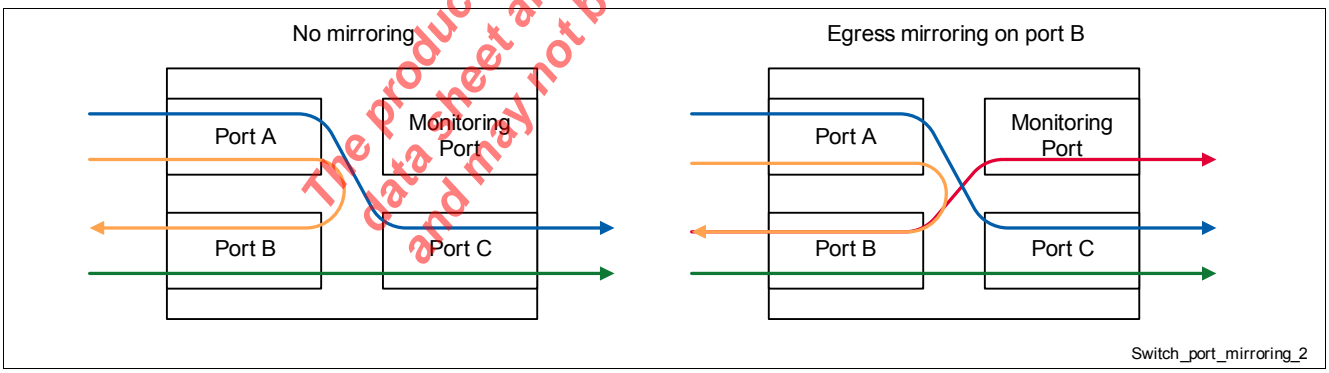


Figure 42 Port Mirroring Examples – Egress Monitoring

Mirroring can also be used to create diagnostic loopbacks, if the ingress port is identical to the monitoring port.

Error Monitoring

Mirroring function can be used to monitor frames that are otherwise dropped due to reception errors, packet filtering, or violation of certain classification rules. In this case the received frame is only delivered to the monitoring port and not to the target egress port that is defined in the egress port map.

Error monitoring can be explicitly enabled for the following type of violations:

- Frame dropped by the classification engine (the destination port map is all-zero)
- Frame contains L2 reception errors

- Frame contains an unknown VLAN ID (the frame carries a VLAN ID that has not been defined in the active VLAN table)
- VLAN Ingress rule violation (acceptable frame filter, i.e. “admit all tagged”)
- Ingress or egress VLAN membership violation (the frame carries a known VLAN ID, but the port is not member of the VLAN group)
- Port state violation
- MAC learning limit violation (the maximum number of MAC addresses to be learned for the port has been exceeded)
- MAC port lock or spoofing detection violation (the MAC source address has already been learned on another port)

3.7.7.3 Wake-on-LAN Functionality

Wake-on-LAN functionality (WoL) is used to wake up a network device by sending a dedicated Layer-2/Layer-3 data packet. The Gigabit Ethernet Switch Macro detects such packets on its Ethernet input ports and triggers an interrupt. This interrupt can be used to wake up an external device, such as a router connected to the switch. Particularly, the following functions are provided:

- Detects “magic packets”
  - Addressed to a dedicated unicast MAC destination address
  - Addressed to a known multicast destination address
  - Addressed to the broadcast MAC destination address
- Password protection can be enabled for magic packets
- Programmable target MAC address
- WoL Interrupt
- WoL packet receive port indication
- WoL enable/disable per port
- Magic packets are forwarded as any other packets (for example based on the MAC destination address) but may as well be dropped if the frame classification is set up accordingly.

In addition to these standard WoL functions, a wake-up can be triggered by making an entry in the Flow Engine and programing a corresponding action to generate an interrupt. This allows to wake up for any frame pattern. Typical patterns are:

- a specified MAC destination address
- a specified MAC source address
- ARP request packets
- directed IPv4/IPv6 packets

The structure of the typical Layer-2 “magic packets” is shown in **Figure 43**. However the fixed pattern followed by the specific unicast address and an optional password can appear in any field location in a packet, including Layer-3 part.

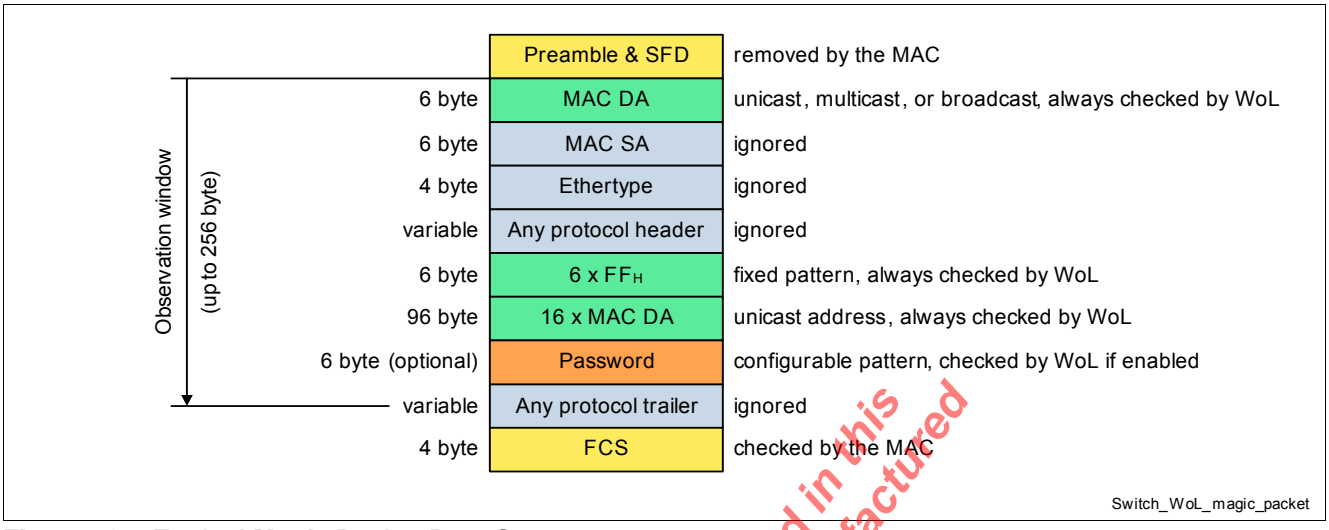


Figure 43 Typical Magic Packet Data Structure

The WoL sequence starts with a synchronization pattern of 6 × FF, followed by 16 repetitions of the target system's MAC address. This must be the unicast address, while the MAC destination address in the layer-2 header may be either the unicast address, the broadcast address, or a multicast address of a group that contains the target system's address. After the WoL pattern, any protocol-specific trailer may follow and the frame must be terminated by a valid frame checksum (FCS). The frame size must be less or equal to the maximum allowed frame size.

As an option, a password can be defined that is checked for the received WoL frames. If the password does not match the configured value, the frame is ignored. The password has the same size as the MAC address (6 byte). The frame structure of a typical Layer-2 password-protected WoL frames is shown in **Figure 44**.

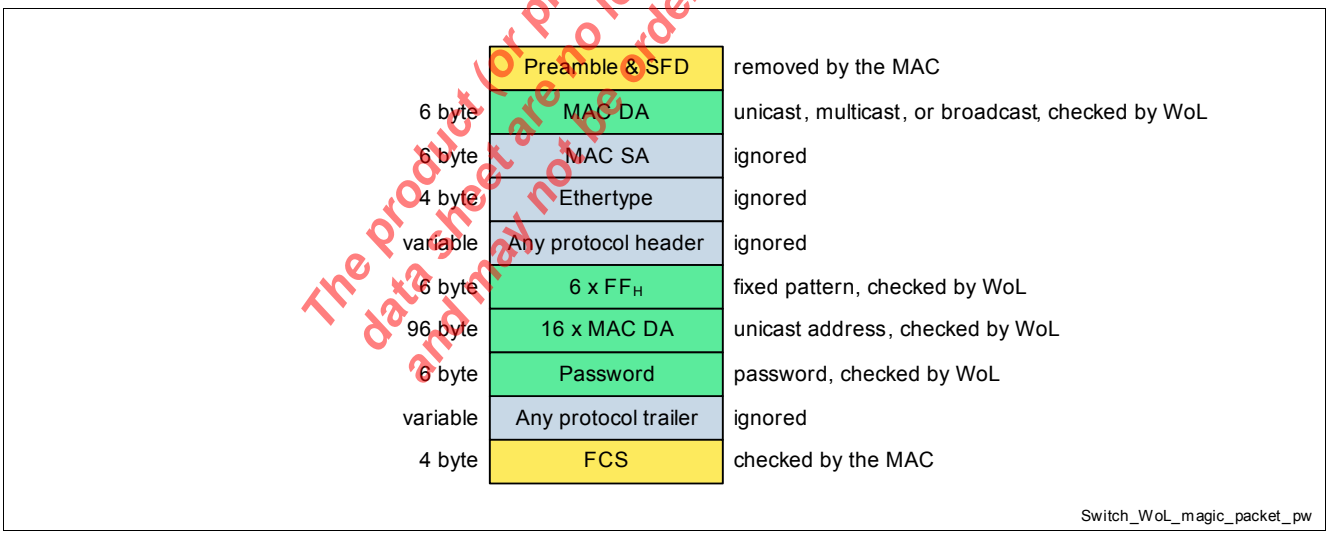


Figure 44 Magic Packet Data Structure – Password Protection

3.7.7.4 Time Stamp Functionality

A 94-bit global timer is implemented. It has three parts: a 32-bit second field, a 30-bit nano-second field and a 32-bit fractional-nano-second field. The global timer can be modified directly, adjusted with a positive/negative value or adjusted with a frequency offset via the following registers: TIMER_FS_LSB, TIMER_FS_MSB, TIMER_NS_LSB, TIMER_NS_MSB, TIMER_SEC_LSB, TIMER_SEC_MSB and TIMER_CTRL.

The Gigabit Ethernet Switch Macro can record a time stamp during frame reception and transmission to support IEEE 1588v2. The time stamp is recorded in hardware at the moment of reception (on ingress) or transmission (on egress) of the first byte of destination MAC address on the attached interface, as described in the **Figure 45**.

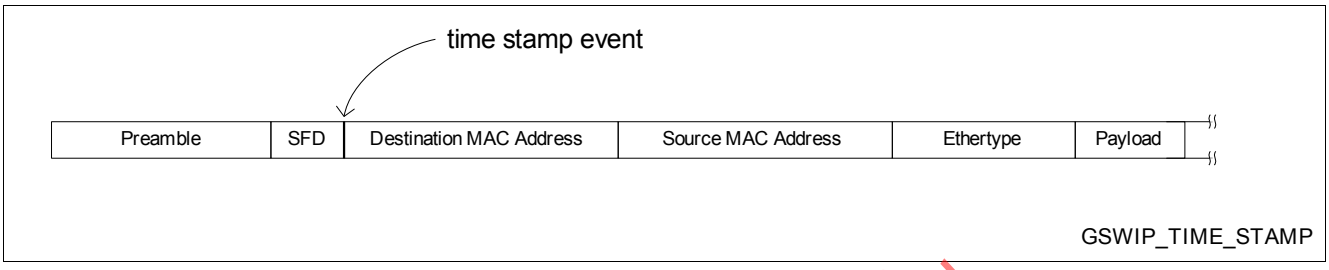


Figure 45 Time stamp event location in the frame

In order to have the time stamp recorded for a specific frame type, an appropriate rule must be added to the Traffic Flow table and a time stamp action selected for ingress time stamp, egress or both. In addition, an interrupt can be generated at the event of the time stamp record. The current timestamp value (2 least significant bit of second field and 30-bit nano-second field) is stored in a register, per port one register for the ingress arrival time (SDMA_TSTAMP0 and SDMA_TSTAMP1) and for the egress departure time (FDMA_TSTAMP0 and FDMA_TSTAMP1) is provided. The time stamp can be retrieved by an appropriate management action.

3.7.7.5 Special Tag Functionality

The special tag is used to override the forwarding and QoS functionality of the switch on the ingress side and to provide additional frame-status information on the egress side.

The special tag is identified by the special Ethertype which is located after the source MAC address in the frame. This allows the transmission of the frame via an Ethernet network to a remote receiver. The special tag content has a fixed length of 6 bytes. For internal communication or point-to-point communication it can be configured per egress port if the frame contains additional content in place of the Ethertype. This option is only available at egress direction, in ingress direction always an Ethertype is expected. See **Figure 46** for illustration.

Pause Frames which are generated by the MAC do not contain a special tag. This can result in a mix of frames with and without special tag on one egress port. Frames with a special tag which do not use the special Ethertype can be distinguished from pause frames since the pause frames have an Ethertype of 0x8808 while the first nibble after the MAC addresses is 0 for frames with a special tag.

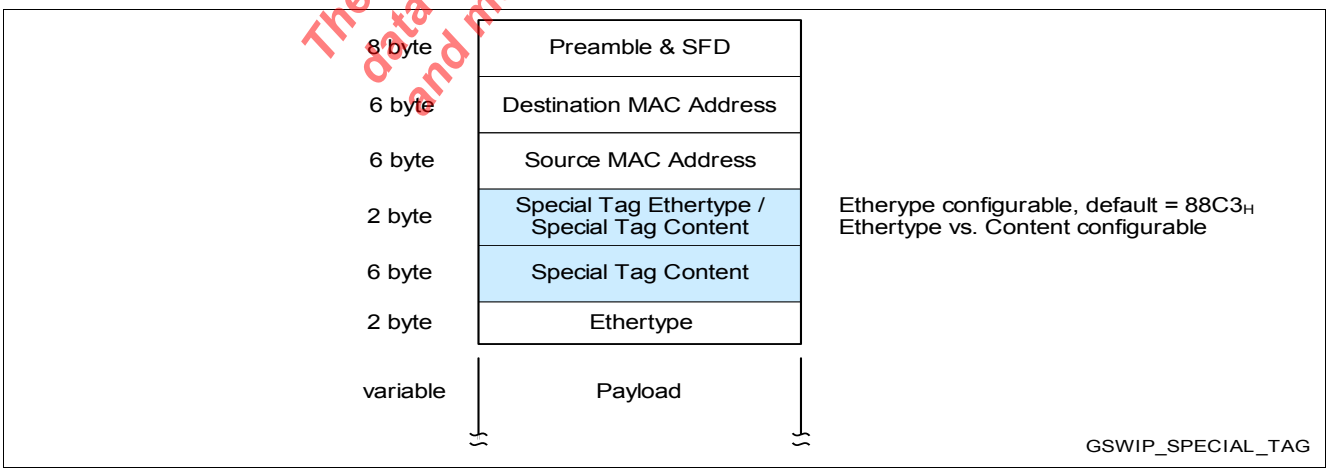


Figure 46 Special tag location in the frame

Note: Typically, the special tag is used on the CPU port of the switch.

The content format of the special tag is different for the ingress and the egress, the egress special tag comes in two formats (internal and external format). The sections below describe the different formats of the tag.

Ingress Special Tag

The ingress special tag is used to override the classification function and the default frame forwarding of the switch. The special tag detection on ingress can be enabled or disabled per port. When the detection is disabled, the frame containing a special tag is treated as regular frame and the content of the frame is ignored.

When the ingress special tag detection is enabled, the content of the tag is used for the frame forwarding decision. The ingress special tag must always have an special tag Ethertype. See **Table 36** for more details on the special tag content.

Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.

Table 36 Special Tag Ingress Format

Byte	Bit	Description
0	[7:0]	**Ethertype byte** 1 (configurable, default: 88_H)
1	[7:0]	**Ethertype byte** 2 (configurable, default: $C3_H$)
2	7	**Port map enable** (1_B = use port map, 0_B = use port mask)
	6	**Traffic class enable** (1_B = use traffic class, 0_B = ignore)
	5	**Time stamp enable** (1_B = generate time stamps, 0_B = ignore)
	4	**Force no learning** (1_B = address is not learned, 0_B = ignore)
	[3:0]	**Target traffic class** (egress priority)
3	[7:0]	**Target egress port map** (low bits)
4	[7:0]	**Target egress port map** (Reserved)
5	[7:5]	**Reserved** (all zero)
	4	**Interrupt enable** (1_B = generate an interrupt, 0_B = ignore)
	[3:0]	**Source Port** (virtual port)
6	[7:0]	**Reserved** (all zero)
7	[7:0]	**Reserved** (all zero)

Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.

Table 37 and **Table 38** describes the encoding of the "*port map enable*" and "*traffic class enable*" fields of the special tag content.

Table 37 Port Map Coding

Port Map Enable	Resulting Port Map
0	The egress port map is based on the forwarding classification result. The Port map in the special tag is used as a filter (AND mask) on the final egress port map in the forwarding function => if a bit in the special tag port map is not set for certain egress port this port is excluded from the final egress port map.
1	The port map determined by forwarding classification result in switch is overruled. The port map in the special tag is used as the egress port map.

Table 38 Traffic Class Map Coding

Traffic Class Enable	Resulting Traffic Class
0	The traffic class is based on the classification result in switch.
1	The traffic class is taken from the special tag (classified Traffic Class ignored).

Additional action flags in the ingress special tag:

- Time-stamp Action. This action flag is used to trigger the latching of the time-stamps for the received packet.
- Interrupt Action. This action generates an interrupt upon the packet reception.
- Force No Learning. This action is used to disable the learning of the source MAC address of the received frame in the MAC bridging table.

The special tag detected on the ingress side is not delivered to the egress side. The tag is removed prior to transmission.

Egress Special Tag

The egress special tag contains status and debug information of the switch. The special tag transmission on egress can be enabled or disabled per egress port. When egress special tag is disabled, no special tag is inserted in the egress frame. When egress special tag function is enabled, each egress frame that is transmitted on that port will contain the special tag.

The egress special tag can be transmitted in one of the two formats:

- **External format.** This format contains Ethertype (2 bytes) and content (6 bytes).
- **Internal format**. This format contains no Ethertype and only content (8 bytes).

The external format can be used to transport the special tag via a network, the internal format is typically used for directly attached devices like a CPU which know how handle the special frame format. See **Table 39** and **Table 40** for more details regarding the egress special tag format.

Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.

Table 39 Special Tag Egress External Format (with Ethertype)

Byte	Bit	Description
0	[7:0]	**Ethertype** byte 1 (configurable, default: 88_H)
1	[7:0]	**Ethertype** byte 2 (configurable, default: $C3_H$)
2	[7:4]	**Traffic Class** The traffic class of the packet determined by the switch classification engine.
	[3:0]	**Ingress port number** (000_B = port 0, …, 110_B = port 6, ...)
3	7	**PPPoE Session Packet** 0_B The packet is not PPPoE session packet 1_B The packet is PPPoE session packet
	6	**IPv4 Packet** 0_B The packet is IPv6 packet if IP offset != 0 1_B The packet is IPv4 packet if IP offset != 0
	[5:0]	**IP Offset**[1]. It defines the byte offset of the first byte in IP field relative to the first byte of Destination MAC address of the egress packet
4	[7:0]	**Destination Logical Port Map (low bits)**
5	[7:0]	**Destination Logical Port Map (Reserved)**

Table 39 Special Tag Egress External Format (with Ethertype) (cont'd)

Byte	Bit	Description
6	7	**Mirror indication**, signals if the frame has been mirrored. 0_B **NORM** normal frame 1_B **MIRR** mirrored frame
	6	**Known L2 unicast/multicast** 0_B The packet's destination MAC does not match one entry in bridging table. 0_B The packet's destination MAC matches one entry in bridging table.
	[5:0]	**Packet Length High Bits**[1)] The total number of bytes in the egress packet.
7	[7:0]	**Packet Length Low Bits**[1)] The total number of bytes in the egress packet.

1) Please note that if a packet is modified at the egress side (packet header modification) with new bytes inserted or removed, the Is Tagged Flag, IP Offset and Packet Length fields are updated accordingly and contain the adjusted value for the transmitted frame. The IP_Offset and the Packet_Length includes the length of the special tag.

Table 40 Special Tag Egress Internal Format (without Ethertype)

Byte	Bit	Description
0	[7:4]	**Reserved** (all zero). Serves also as code to distinguish Pause frames generated by the MAC from frames with special tag without Ethertype since Pause frames start with "8" and not 0.
	3	**Receive error** indication (MAC error) 0_B **OK** Frame is Ok 1_B **ERR** Frame contains a MAC error
	2	**Drop indication**, signals if a mirrored packet has been dropped (delivered only to the mirror port) or has been forwarded (delivered normally and to the mirror port) 0_B **FWD** frame has been forwarded 1_B **DROP** frame has been dropped
	[1:0]	**Drop precedence**, defines if the frame shall be eligible for dropping. 00_B **CRT** Critical frame indication 01_B **GRN** drop precedence low 10_B **YEL** drop precedence medium 11_B **RED** drop precedence high
1	[7:0]	**Flow/Error Indication** • **Flow Indication** (if Receive error = OK and Drop Indication = FWD) • **Error Indication** – errored frames (if Receive error = ERR) – dropped frames (if Receive error = OK and Drop Indication = DROP) The error code for discarded or errored frames are described in **Table 41**
2	[7:4]	**Traffic Class** The traffic class of the packet determined by the switch classification engine.
	[3:0]	**Ingress port number** (000_B = port 0, …, 110_B = port 6, ...)

Table 40 Special Tag Egress Internal Format (without Ethertype) (cont'd)

Byte	Bit	Description
3	7	**PPPoE Session Packet** 0_B The packet is not PPPoE session packet 1_B The packet is PPPoE session packet
	6	**IPv4 Packet** 0_B The packet is IPv6 packet if IP offset != 0 1_B The packet is IPv4 packet if IP offset != 0
	[5:0]	**IP Offset**[1)]. It defines the byte offset of the first byte in IP field relative to the first byte of Destination MAC address of the egress packet
4	[7:0]	**Destination Logical Port Map (low bits)**
5	[7:0]	**Destination Logical Port Map (Reserved)**
6	7	**Mirror indication**, signals if the frame has been mirrored. 0_B **NORM** normal frame 1_B **MIRR** mirrored frame
	6	**Known L2 unicast/multicast** 0_B The packet's destination MAC does not match one entry in bridging table. 0_B The packet's destination MAC matches one entry in bridging table.
	[5:0]	**Packet Length High Bits**[1)] The total number of bytes in the egress packet.
7	[7:0]	**Packet Length Low Bits**[1)] The total number of bytes in the egress packet.

1) Please note that if a packet is modified at the egress side (packet header modification) with new bytes inserted or removed, the Is Tagged Flag, IP Offset and Packet Length fields are updated accordingly and contain the adjusted value for the transmitted frame. The IP_Offset and the Packet_Length includes the length of the special tag.

Table 41 Error Codes

Bit Position	Error Type
Error Indication for Frames with MAC Error (byte 0, bit 3 = ERR, byte 0, bit 2 = don't care)	
7	Undefined, reserved for future use, set to 0_B
6	Receive error
5	Is pause frame
4	FCS error
3	Length error
2	Alignment error
1	Frame too long
0	Frame too short
Violation Indication for Dropped Frames (byte 0, bit 3 = OK, byte 0, bit 2 = DROP)	
0	Egress Port State Violation
1	Ingress Port-State Violation
2	Port-Lock Violation
3	MAC Learning Limitation Violation
4	VLAN Egress Membership Violation

Table 41 Error Codes (cont'd)

Bit Position	Error Type
5	VLAN Ingress Membership Violation
6	VLAN Ingress Tag Rule Violation
7	Unknown VLAN Violation
Flow Indication for Good Frames (byte 0.3 = OK, byte 0.2 = FWD)	
07:0	Flow Identification

4 Registers

4.1 Top Level PDI Registers

Table 42 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Top Level PDI Registers, GPHY Shell Registers			
GPHY0_FCR	GPHY0 Firmware Address Offset Register	$F700_H$	4000_H
GPHY1_FCR	GPHY1 Firmware Address Offset Register	$F710_H$	
GPHY2_FCR	GPHY2 Firmware Address Offset Register	$F720_H$	
GPHY3_FCR	GPHY3 Firmware Address Offset Register	$F730_H$	
GPHY4_FCR	GPHY4 Firmware Address Offset Register	$F740_H$	
GPHY0_CFG	GPHY0 General Configuration Register	$F701_H$	0000_H
GPHY1_CFG	GPHY1 General Configuration Register	$F711_H$	
GPHY2_CFG	GPHY2 General Configuration Register	$F721_H$	
GPHY3_CFG	GPHY3 General Configuration Register	$F731_H$	
GPHY4_CFG	GPHY4 General Configuration Register	$F741_H$	
GPHY0_AFETX_CTRL	GPHY0 AFE TX Path Control Register	$F702_H$	0000_H
GPHY1_AFETX_CTRL	GPHY1 AFE TX Path Control Register	$F712_H$	
GPHY2_AFETX_CTRL	GPHY2 AFE TX Path Control Register	$F722_H$	
GPHY3_AFETX_CTRL	GPHY3 AFE TX Path Control Register	$F732_H$	
GPHY4_AFETX_CTRL	GPHY4 AFE TX Path Control Register	$F742_H$	
GPHY0_FCR_SD	GPHY0 Firmware Address Offset Shadow Register	$F703_H$	4000_H
GPHY1_FCR_SD	GPHY1 Firmware Address Offset Shadow Register	$F713_H$	
GPHY2_FCR_SD	GPHY2 Firmware Address Offset Shadow Register	$F723_H$	
GPHY3_FCR_SD	GPHY3 Firmware Address Offset Shadow Register	$F733_H$	
GPHY4_FCR_SD	GPHY4 Firmware Address Offset Shadow Register	$F743_H$	
GPHY0_GPS	GPHY0 General Pin Strapping Register	$F708_H$	$00FF_H$
GPHY1_GPS	GPHY1 General Pin Strapping Register	$F718_H$	
GPHY2_GPS	GPHY2 General Pin Strapping Register	$F728_H$	
GPHY3_GPS	GPHY3 General Pin Strapping Register	$F738_H$	
GPHY4_GPS	GPHY4 General Pin Strapping Register	$F748_H$	
GPHY0_BFDEV	GPHY0 Base Frequency Deviation Configuration Register	$F709_H$	3333_H

Table 42 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
GPHY1_BFDEV	GPHY1 Base Frequency Deviation Configuration Register	$F719_H$	
GPHY2_BFDEV	GPHY2 Base Frequency Deviation Configuration Register	$F729_H$	
GPHY3_BFDEV	GPHY3 Base Frequency Deviation Configuration Register	$F739_H$	
GPHY4_BFDEV	GPHY4 Base Frequency Deviation Configuration Register	$F749_H$	
GPHY0_STATUS	GPHY0 General Status Register	$F70F_H$	0000_H
GPHY1_STATUS	GPHY1 General Status Register	$F71F_H$	
GPHY2_STATUS	GPHY2 General Status Register	$F72F_H$	
GPHY3_STATUS	GPHY3 General Status Register	$F73F_H$	
GPHY4_STATUS	GPHY4 General Status Register	$F74F_H$	
Top Level PDI Registers, (R)GMII Registers			
MII_CFG_5	xMII Interface 5 Configuration Register	$F100_H$	2044_H
MII_CFG_6	xMII Interface 6 Configuration Register	$F10A_H$	
PCDU_5	RGMII 5 Clock Delay Configuration Register	$F101_H$	0000_H
PCDU_6	RGMII 6 Clock Delay Configuration Register	$F10B_H$	
RTXB_CTL_5	xMII5 Interface Receive Transmit Buffer Control Register	$F120_H$	0009_H
RXB_CTL_6	xMII6 Interface Receive Buffer Control Register	$F125_H$	
MII_MUX_CFG	Pin and Port Multiplexing Configuration	$F130_H$	0000_H
PKT_INS	Packet Insertion Register	$F140_H$	0000_H
PKT_EXT_READ	Packet Extraction Read Register	$F141_H$	0000_H
PKT_EXT_CMD	Packet Extraction Command Register	$F142_H$	0000_H
PCDU5_TX_KVAL	PCDU5 TX K Value	$F160_H$	0040_H
PCDU6_TX_KVAL	PCDU6 TX K Value Register	$F170_H$	
PCDU5_TX_MREQ	PCDU5 TX M Required	$F161_H$	0000_H
PCDU6_TX_MREQ	PCDU6 TX M Required Register	$F171_H$	
PCDU5_TX_MBLK	PCDU5 TX M Blank	$F162_H$	0002_H
PCDU6_TX_MBLK	PCDU6 TX M Blank Register	$F172_H$	
PCDU5_TX_DELLEN	PCDU5 TX Delay Length	$F163_H$	0000_H
PCDU6_TX_DELLEN	PCDU6 TX Delay Length Register	$F173_H$	
PCDU5_RX_KVAL	PCDU5 RX K Value	$F168_H$	0040_H
PCDU6_RX_KVAL	PCDU6 RX K Value Register	$F178_H$	
PCDU5_RX_MREQ	PCDU5 RX M Required	$F169_H$	0000_H
PCDU6_RX_MREQ	PCDU6 RX M Required Register	$F179_H$	
PCDU5_RX_MBLK	PCDU5 RX M Blank	$F16A_H$	0002_H
PCDU6_RX_MBLK	PCDU6 RX M Blank Register	$F17A_H$	

Table 42 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
PCDU5_RX_DELLEN	PCDU5 RX Delay Length	$F16B_H$	0000_H
PCDU6_RX_DELLEN	PCDU6 RX Delay Length Register	$F17B_H$	
Top Level PDI Registers, MDIO Master Registers			
GSWIP_CFG	GSWIP Configuration Register	$F400_H$	0000_H
MMDIO_CTRL	MDIO Master Control Register	$F408_H$	0000_H
MMDIO_READ	MDIO Master Read Data Register	$F409_H$	0000_H
MMDIO_WRITE	MDIO Master Write Data Register	$F40A_H$	0000_H
MMDC_CFG_0	MDC Master Clock Configuration Register 0	$F40B_H$	$007F_H$
MMDC_CFG_1	MDC Master Clock Configuration Register 1	$F40C_H$	0109_H
PHY_ADDR_0	PHY Address Register PORT 0	$F415_H$	1800_H
MMDIO_STAT_0	PHY MDIO Polling Status per PORT	$F416_H$	0000_H
MMDIO_STAT_1	PHY MDIO Polling Status per PORT 1	$F417_H$	
MMDIO_STAT_2	PHY MDIO Polling Status per PORT 2	$F418_H$	
MMDIO_STAT_3	PHY MDIO Polling Status per PORT 3	$F419_H$	
MMDIO_STAT_4	PHY MDIO Polling Status per PORT 4	$F41A_H$	
MMDIO_STAT_5	PHY MDIO Polling Status per PORT 5	$F41B_H$	
MMDIO_STAT_6	PHY MDIO Polling Status per PORT 6	$F41C_H$	
PHY_ADDR_1	PHY Address Register PORT 1	$F414_H$	1801_H
PHY_ADDR_2	PHY Address Register PORT 2	$F413_H$	1802_H
PHY_ADDR_3	PHY Address Register PORT 3	$F412_H$	1803_H
PHY_ADDR_4	PHY Address Register PORT 4	$F411_H$	1804_H
PHY_ADDR_5	PHY Address Register PORT 5	$F410_H$	1805_H
PHY_ADDR_6	PHY Address Register PORT 6	$F40F_H$	1806_H
ANEG_EEE_0	EEE auto negotiation overrides	$F41D_H$	0000_H
ANEG_EEE_1	EEE auto negotiation overrides	$F41E_H$	
ANEG_EEE_2	EEE auto negotiation overrides	$F41F_H$	
ANEG_EEE_3	EEE auto negotiation overrides	$F420_H$	
ANEG_EEE_4	EEE auto negotiation overrides	$F421_H$	
ANEG_EEE_5	EEE auto negotiation overrides	$F422_H$	
ANEG_EEE_6	EEE auto negotiation overrides	$F423_H$	
Top Level PDI Registers, MDIO Slave Registers			
SMDIO_CFG	MDC Slave Configuration Register	$F480_H$	$01F1_H$
SMDIO_BADR	MDC Slave Target Base Address Register	$F481_H$	00000_H
Top Level PDI Registers, SPI Master Registers			
MSPI_CFG	SPI Master Interface Configuration Register	$F510_H$	8019_H
MSPI_OP	SPI Master Operating Mode Configuration Register	$F511_H$	0000_H
MSPI_MANCTRL	SPI Master Manual Mode Control Register	$F512_H$	0000_H
MSPI_ISR	SPI Master Interrupt Status Register	$F513_H$	0000_H

Table 42 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
MSPI_IER	SPI Master Interrupt Enable Register	$F514_H$	0000_H
MSPI_DIN01	SPI Master Data In 0/1 Register	$F518_H$	0000_H
MSPI_DIN23	SPI Master Data In 2/3 Register	$F519_H$	0000_H
MSPI_DIN45	SPI Master Data In 4/5 Register	$F51A_H$	0000_H
MSPI_DIN67	SPI Master Data In 6/7Register	$F51B_H$	0000_H
MSPI_DOUT01	SPI Master Data Out 0/1 Register	$F51C_H$	0000_H
MSPI_DOUT23	SPI Master Data Out 2/3 Register	$F51D_H$	0000_H
MSPI_DOUT45	SPI Master Data Out 4/5 Register	$F51E_H$	0000_H
MSPI_DOUT67	SPI Master Data Out 6/7 Register	$F51F_H$	0000_H
Top Level PDI Registers, SPI Slave Registers			
SSPI_CFG	SPI Slave Configuration Register	$F580_H$	0200_H
Top Level PDI Registers, UART Registers			
UART_CFG	UART Configuration Register	$F680_H$	0001_H
UART_BD	UART Baudrate Register	$F681_H$	$087A_H$
UART_FDIV	UART Baudrate Fractional Divider Register	$F682_H$	0024_H
UART_PROMPT	UART PROMPT Register	$F683_H$	$003E_H$
UART_ERRCNT	UART Error Counter Register	$F684_H$	0000_H
Top Level PDI Registers, Clock Generation Unit Registers			
SYSPLL_CFG0	SYS PLL Configuration 0 Register	$F980_H$	0140_H
SYSPLL_CFG1	SYS PLL Configuration 1 Register	$F984_H$	0000_H
SYSPLL_CFG2	SYS PLL Configuration Register 2	$F988_H$	6666_H
SYSPLL_CFG3	SYS PLL Configuration Register 3	$F98C_H$	0140_H
SYSPLL_MISC	SYSPLL Miscellaneous Control Register	$F990_H$	0022_H
GPC0_CONF	GPC0 Configuration Register	$F948_H$	0000_H
GPC1_CONF	GPC1 Configuration Register	$F94C_H$	
SYSCLK_CONF	SYCCLK Configuration Register	$F950_H$	0000_H
Top Level PDI Registers, Reset Control Unit Registers			
RESET_STATUS	Reset Status Register	$FA00_H$	8000_H
RST_REQ	Reset Request Register	$FA01_H$	$002F_H$
MANU_ID	MANU ID Register	$FA10_H$	0713_H
PNUM_ID	PNUM ID Register	$FA11_H$	$x003_H$
GPIO_DRIVE0_CFG	GPIO PAD Driver Strength 0 Control Register	$FA70_H$	$3FFF_H$
GPIO_DRIVE1_CFG	GPIO PAD Driver Strength 1 Control Register	$FA71_H$	0000_H
GPIO_SLEW_CFG	GPIO PAD Slew Control Register	$FA72_H$	0000_H
GPIO2_DRIVE0_CFG	GPIO2 PAD Driver Strength 0 Control Register	$FA74_H$	$7FFF_H$
GPIO2_DRIVE1_CFG	GPIO2 PAD Driver Strength 1 Control Register	$FA75_H$	0000_H
GPIO2_SLEW_CFG	GPIO2 Slew Control Register	$FA76_H$	0000_H
RGMII_SLEW_CFG	RGMII PAD Slew Control Register	$FA78_H$	0000_H

Table 42 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
PS0	Pin Strapping Register	$FA80_H$	$XXXX_H$
PS1	Pin Strapping Register 1	$FA81_H$	$XXXX_H$
Top Level PDI Registers, GPIO Registers			
GPIO_OUT	GPIO Data Output Register	$F380_H$	0000_H
GPIO_IN	GPIO Data Input Register	$F381_H$	0000_H
GPIO_DIR	GPIO Direction Register	$F382_H$	0000_H
GPIO_ALTSEL0	Port 0 Alternate Function Select Register 0	$F383_H$	0000_H
GPIO_ALTSEL1	Port 0 Alternate Function Select Register 1	$F384_H$	$003C_H$
GPIO_OD	GPIO Open Drain Control Register	$F385_H$	$3FFF_H$
GPIO_PUDSEL	GPIO Pull-Up/Pull-Down Select Register	$F386_H$	$3FFF_H$
GPIO_PUDEN	GPIO Pull-Up/Pull-Down Enable Register	$F387_H$	$3FFF_H$
GPIO2_OUT	GPIO2 Data Output Register	$F390_H$	0000_H
GPIO2_IN	GPIO2 Data Input Register	$F391_H$	0000_H
GPIO2_DIR	GPIO2 Direction Register	$F392_H$	0000_H
GPIO2_ALTSEL0	Port 2 Alternate Function Select Register 0	$F393_H$	0000_H
GPIO2_ALTSEL1	Port 2 Alternate Function Select Register 1	$F394_H$	0000_H
GPIO2_OD	GPIO2 Open Drain Control Register	$F395_H$	$7FFF_H$
GPIO2_PUDSEL	GPIO2 Pull-Up/Pull-Down Select Register	$F396_H$	$7FFF_H$
GPIO2_PUDEN	GPIO2 Pull-Up/Pull-Down Enable Register	$F397_H$	$7FFF_H$
Top Level PDI Registers, ICU Registers			
IM0_ISR	IM0 Interrupt Status Register	$F3C0_H$	0000_H
IM0_EINT0_IER	IM0 EINT0 Interrupt Enable Register	$F3C2_H$	0000_H
IM0_EINT1_IER	IM0 EINT1 Interrupt Enable Register	$F3C3_H$	0000_H
EIU_EXIN_CONF	EIU External Interrupt Controller Register	$F3C4_H$	0000_H
Top Level PDI Registers, LED Registers			
LED_MD_CFG	LED Single Color LED Mode Register	$F3E0_H$	0000_H
LED_BRT_CTRL	LED Brightness Control Register	$F3E1_H$	$F430_H$
LED_LSENS_CTRL	LED Light Sensing Control Register	$F3E2_H$	$0D09_H$

The register is addressed wordwise.

Table 43 Register Access Types

Mode	Symbol
Interrupt status register, latching high, cleared by writing a ONE	lhsc
Hardware status, read-only	rh
Read/write register with input from and output to hardware	rwh
Standard read/write register with output to hardware	rw

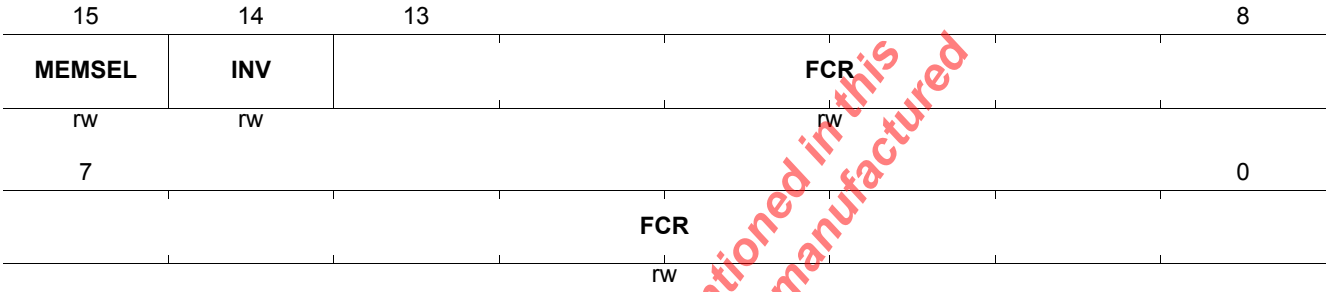
4.1.1 GPHY Shell Registers

This chapter provides the registers that are needed for GPHY configuration.

GPHY0 Firmware Address Offset Configuration Register

This register is used to store GPHY0 firmware address offset.

GPHY0_FCR	Offset	Reset Value
GPHY0 Firmware Address Offset Register	$F700_H$	4000_H



Field	Bits	Type	Description
MEMSEL	15	rw	**GPHY Code Memory Mode** **Constants** 0_B **INT** GPHY Macro loads firmware memory from internal ROM or internal RAM. 1_B **EXTROM** GPHY Macro loads firmware memory by external E2PROM.
INV	14	rw	**Firmware Address Inversion** **Constants** 0_B **NOINV** Firmware address is not inverted. 1_B **INV** Firmware address is inverted when access internal ROM or internal RAM.
FCR	13:0	rw	**Firmware Address Offset MSB** **It stores PHY0 firmware offset address bit 17 to 4. The lower 4 address bits is 0.**

Similar Registers

The following registers are identical to the Register **GPHY0_FCR** defined above.

Table 44 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_FCR	GPHY1 Firmware Address Offset Register	$F710_H$	
GPHY2_FCR	GPHY2 Firmware Address Offset Register	$F720_H$	
GPHY3_FCR	GPHY3 Firmware Address Offset Register	$F730_H$	
GPHY4_FCR	GPHY4 Firmware Address Offset Register	$F740_H$	

GPHY0 General Configuration Register

This register is used to store GPHY0 general configuration register.

GPHY0_CFG	Offset	Reset Value
GPHY0 General Configuration Register	$F701_H$	0000_H

Field	Bits	Type	Description
IDCNMI	1	rwh	**IDC Non-maskable Interrupt** This is an interrupt to the IDC which is non-maskable. As such this is the highest priority interrupt possible. It can be used for emergency applications. This signal is cleared when interrupt is acknowledged. 0_B **NIL** NMI interrupt is not pending. 1_B **INT** NMI interrupt is pending.
MDINTP	0	rw	**MDIO Interrupt Polarity** This type of information is evaluated by the integrated controller to allow configuration of the MDIO interrupt polarity by the instantiating SOC. For automatic configuration of the MDIO Interrupt polarity this configuration bit could be connected to the input of the MDIO interrupt pad. This field must be configured to 0_B. 0_B **HIGH** MDIO Interrupt is active high. 1_B **LOW** MDIO Interrupt is active low.

Similar Registers

The following registers are identical to the Register **GPHY0_CFG** defined above.

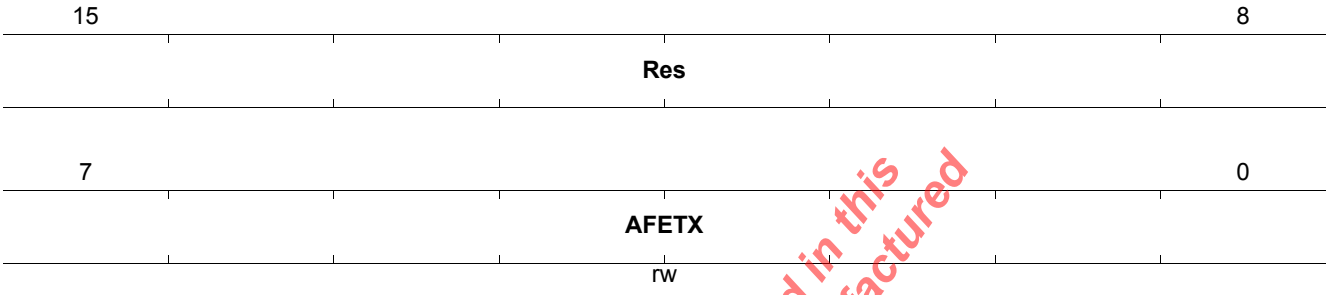
Table 45 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_CFG	GPHY1 General Configuration Register	$F711_H$	
GPHY2_CFG	GPHY2 General Configuration Register	$F721_H$	
GPHY3_CFG	GPHY3 General Configuration Register	$F731_H$	
GPHY4_CFG	GPHY4 General Configuration Register	$F741_H$	

GPHY0 AFE TX Path Control Register

This register is used to store the control information for GPHY0 AFE TX Path.

GPHY0_AFETX_CTRL	Offset	Reset Value
GPHY0 AFE TX Path Control Register	$F702_H$	0000_H



Field	Bits	Type	Description
AFETX	7:0	rw	**Control for AFE TX** Use this input to configure AFE TX path parameters.

Similar Registers

The following registers are identical to the Register GPHY0_AFETX_CTRL defined above.

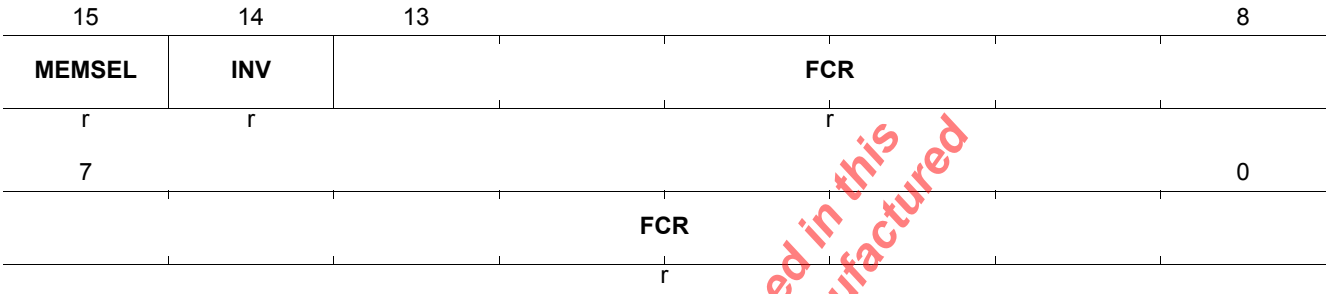
Table 46 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_AFETX_CTRL	GPHY1 AFE TX Path Control Register	$F712_H$	
GPHY2_AFETX_CTRL	GPHY2 AFE TX Path Control Register	$F722_H$	
GPHY3_AFETX_CTRL	GPHY3 AFE TX Path Control Register	$F732_H$	
GPHY4_AFETX_CTRL	GPHY4 AFE TX Path Control Register	$F742_H$	

GPHY0 Firmware Address Offset Configuration Shadow Register

This register is used to store GPHY0 firmware address offset shadow value.

GPHY0_FCR_SD	Offset	Reset Value
GPHY0 Firmware Address Offset Shadow Register	$F703_H$	4000_H



Field	Bits	Type	Description
MEMSEL	15	r	**GPHY Code Memory Mode** **Constants** 0_B **INT** GPHY Macro loads firmware memory from internal ROM or internal RAM. 1_B **EXTROM** GPHY Macro loads firmware memory by external E2PROM.
INV	14	r	**Firmware Address Inversion** **Constants** 0_B **NOINV** Firmware address is not inverted. 1_B **INV** Firmware address is inverted when access internal ROM or internal RAM.
FCR	13:0	r	**Firmware Address Offset MSB** **It stores PHY0 firmware offset address bit 17 to 4. The lower 4 address bits is 0.**

Similar Registers

The following registers are identical to the Register **GPHY0_FCR_SD** defined above.

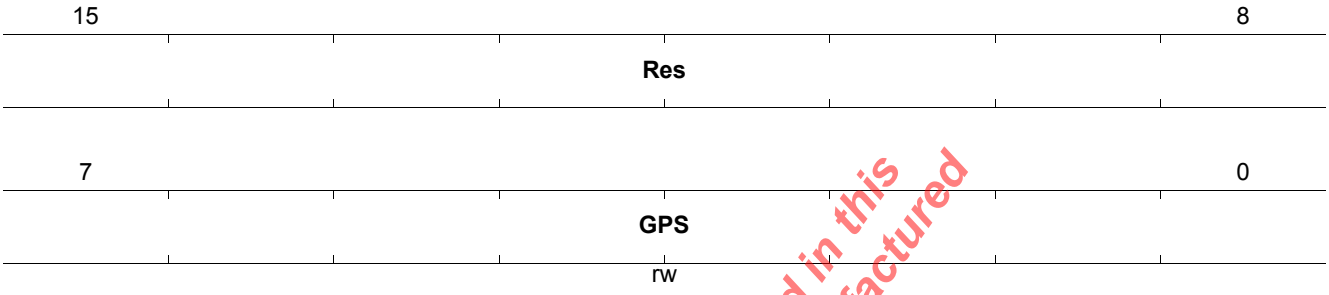
Table 47 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_FCR_SD	GPHY1 Firmware Address Offset Shadow Register	$F713_H$	
GPHY2_FCR_SD	GPHY2 Firmware Address Offset Shadow Register	$F723_H$	
GPHY3_FCR_SD	GPHY3 Firmware Address Offset Shadow Register	$F733_H$	
GPHY4_FCR_SD	GPHY4 Firmware Address Offset Shadow Register	$F743_H$	

GPHY0 General Pin Strapping Register

This register is used to store general pin strapping configuration register.

GPHY0_GPS	Offset	Reset Value
GPHY0 General Pin Strapping Register	$F708_H$	$00FF_H$



Field	Bits	Type	Description
GPS	7:0	rw	**General Pin Strapping** **This connects GPHY general pin strapping bit 7 to 0.**

Similar Registers

The following registers are identical to the Register GPHY0_GPS defined above.

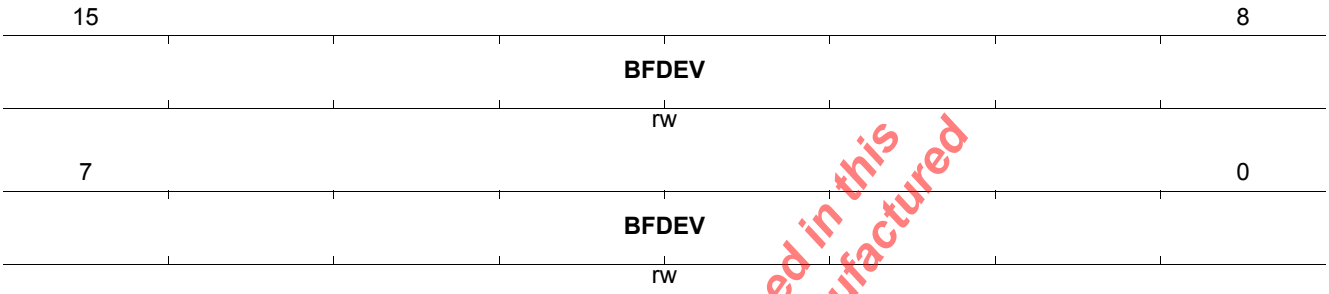
Table 48 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_GPS	GPHY1 General Pin Strapping Register	$F718_H$	
GPHY2_GPS	GPHY2 General Pin Strapping Register	$F728_H$	
GPHY3_GPS	GPHY3 General Pin Strapping Register	$F738_H$	
GPHY4_GPS	GPHY4 General Pin Strapping Register	$F748_H$	

GPHY0 Base Frequency Deviation Configuration Register

This register is used to store base frequency deviation configuration register.

GPHY0_BFDEV	Offset	Reset Value
GPHY0 Base Frequency Deviation Configuration Register	$F709_H$	3333_H



Field	Bits	Type	Description
BFDEV	15:0	rw	**Base Frequency Deviation** Use this input to specify base frequency deviation from nominal base.

Similar Registers

The following registers are identical to the Register GPHY0_BFDEV defined above.

Table 49 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_BFDEV	GPHY1 Base Frequency Deviation Configuration Register	$F719_H$	
GPHY2_BFDEV	GPHY2 Base Frequency Deviation Configuration Register	$F729_H$	
GPHY3_BFDEV	GPHY3 Base Frequency Deviation Configuration Register	$F739_H$	
GPHY4_BFDEV	GPHY4 Base Frequency Deviation Configuration Register	$F749_H$	

GPHY0 General Status Register

This register is used to store GPHY0 general status register.

GPHY0_STATUS	Offset	Reset Value
GPHY0 General Status Register	$F70F_H$	0000_H

Field	Bits	Type	Description
IDCPWD	1	r	**IDC Power Down** **Constants** 0_B **PUP** IDC is powered up. 1_B **PDOWN** IDC is powered down.
IDCIDLE	0	r	**IDC Idle** **Constants** 0_B **ACT** IDC is active. 1_B **IDLE** IDC is idle.

Similar Registers

The following registers are identical to the Register **GPHY0_STATUS** defined above.

Table 50 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_STATUS	GPHY1 General Status Register	$F71F_H$	
GPHY2_STATUS	GPHY2 General Status Register	$F72F_H$	
GPHY3_STATUS	GPHY3 General Status Register	$F73F_H$	
GPHY4_STATUS	GPHY4 General Status Register	$F74F_H$	

4.1.2 (R)GMII Registers

This chapter provides the control registers of the (R)GMII Interfaces.

xMII Interface 5 Configuration Register

This register controls the settings of the xMII Interface.

MII_CFG_5	Offset	Reset Value
xMII Interface 5 Configuration Register	$F100_H$	2044_H

15	14	13	12	11	10	9	8
RST	EN	ISOL	CLKDIS	Res	CRS		RGMII_IBS
rwh	rw	rw	rw		rw		rw

7	6	4	3	0
Res	MIIRATE		MIIMODE	
	rw		rw	

Field	Bits	Type	Description
RST	15	rwh	**Hardware Reset** Resets all related hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers. **Constants** 0_B **OFF** reset is off 1_B **ON** reset is active
EN	14	rw	**xMII Interface Enable** The corresponding interface can only be enabled if the disable signal at macro boundary is inactive. Otherwise the interface is disabled. **Constants** 0_B **DIS** disable the interface 1_B **EN** enable the interface
ISOL	13	rw	**ISOLATE xMII Interface** Set to 0 for normal operation. In ISOLATE all xMII Output Pins are set to be disabled **Constants** 0_B **EN** Interface is active 1_B **ISO** Interface outputs are isolated
CLKDIS	12	rw	**Link Down Clock Disable** For power save in case of link down signaled by MDIO, the clocks in the xMII module and in the xMII Interface can be switched off automatically. The automatic switching off can be enabled by setting this parameter to “On”. **Constants** 0_B **OFF** No automatic disable in case of link down 1_B **ON** Disable clocks in case of link down and switch interface off

Field	Bits	Type	Description
CRS	10:9	rw	**CRS Sensitivity Configuration** These Bits are only valid in PHY Mode. CRS can be configured depending on RX and TX activity and Half/Full Duplex Modes (HDX/FDX) **Constants** 00_B **MD0** HDX:TX+RX, FDX:RX 01_B **MD1** HDX:TX+RX, FDX:0 10_B **MD2** HDX:RX, FDX:RX 11_B **MD3** HDX:RX, FDX:0
RGMII_IBS	8	rw	**RGMII In Band Status** If RGMII mode is selected, this bit controls if the In Band Status Bits Link, Clock Speed duplex are transmitted during IPG Could be set to “On” in case of connected to an external MAC. RGMII in band status extraction is always on regardless of this setting. **Constants** 0_B **OFF** RGMII In Band Status is off 1_B **ON** RGMII In Band Status is on
MIIRATE	6:4	rw	**xMII Interface Clock Rate** Selects the data and clock rate for the xMII interface. **Constants** 000_B **M2P5** 2.5 MHz 001_B **M25** 25 MHz 010_B **M125** 125 MHz 100_B **Auto** Automatically clock rate based on speed
MIIMODE	3:0	rw	**xMII Interface Mode** This selects the xMII interface mode. **Constants** 0001_B **GMII** GMII mode, connected to external PH. 0100_B **RGMII** RGMII mode, connected to external PHY or MAC.

Similar Registers

The following registers are identical to the Register **MII_CFG_5** defined above.

Table 51 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
MII_CFG_6	xMII Interface 6 Configuration Register	$F10A_H$	

RGMII 5 Clock Delay Configuration Register

This register controls the settings of the receive and transmit clock delay.

PCDU_5	Offset	Reset Value
RGMII 5 Clock Delay Configuration Register	$F101_H$	0000_H

Field	Bits	Type	Description
DELMD	10	rw	**PCDU Delay Setting Mode** **Constants** 0_B **DELAY** Setting clock delay directly 1_B **MK** Setting M, K values
RXDLY	9:7	rw	**Configure Receive Clock Delay** Configure the delay of RX_CLK_D versus RX_CLK in steps of 500 ps. The resulting delay is TD = unsigned(RXDLY) * 500 ps
TXDLY	2:0	rw	**Configure Transmit Clock Delay** Configure the delay of TX_CLK_D versus TX_CLK in steps of 500 ps. The total configured delay is TD=unsigned(TXDLY)*500 ps.

Similar Registers

The following registers are identical to the Register **PCDU_5** defined above.

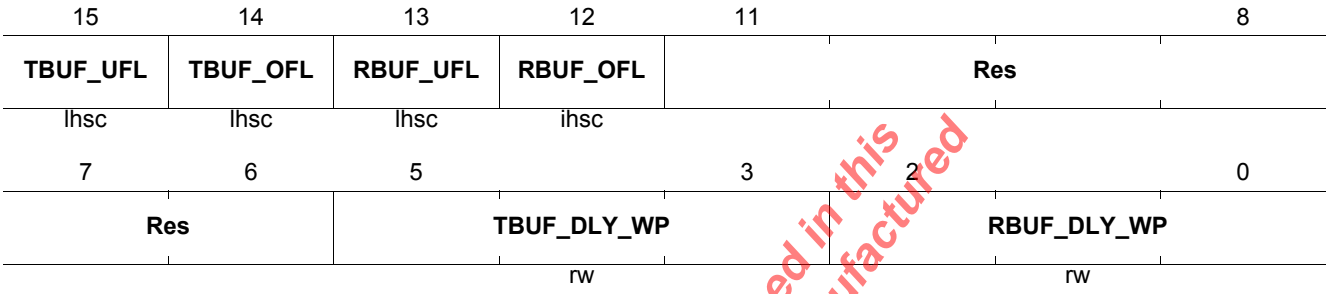
Table 52 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU_6	RGMII 6 Clock Delay Configuration Register	$F10B_H$	

xMII5 Interface Receive Transmit Buffer Control Register

This register is used to configure the internal receive buffer and check under and overflow.

RTXB_CTL_5	Offset	Reset Value
xMII5 Interface Receive Transmit Buffer Control Register	$F120_H$	0009_H



Field	Bits	Type	Description
TBUF_UFL	15	lhsc	**Transmit Buffer Underflow Indicator** Indicates if one or more transmit buffer underflow events have been detected. Constants 0_B **NONE** NONE Underflow never detected 1_B **UFL** UFL Underflow occurred at least once
TBUF_OFL	14	lhsc	**Transmit Buffer Overflow Indicator** Indicates if one or more transmit buffer overflow events have been detected. Constants 0_B **NONE** NONE Overflow never detected 1_B **OFL** OFL Overflow occurred at least once
RBUF_UFL	13	lhsc	**Receive Buffer Underflow Indicator** Indicates if one or more receive buffer underflow events have been detected. **Constants** 0_B **NONE** Underflow is never detected 1_B **UFL** Underflow occurred at least once
RBUF_OFL	12	lhsc	**Receive Buffer Overflow Indicator** Indicates if one or more receive buffer overflow events have been detected. **Constants** 0_B **NONE** Overflow is never detected 1_B **OFL** Overflow occurred at least once
TBUF_DLY_WP	5:3	rw	**TX Buffer Delay Write Pointer** This register is used to configure the initial delay of the write pointer in the transmit buffer. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.

Field	Bits	Type	Description
RBUF_DLY_WP	2:0	rw	**RX Buffer Delay Write Pointer** This register is used to configure the initial delay of the write pointer in the receive buffer. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.

Similar Registers

The following registers are identical to the Register **RTXB_CTL_5** defined above.

Table 53 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
RXB_CTL_6	xMII6 Interface Receive Buffer Control Register	$F125_H$	

Pin and Port Multiplexing Configuration

This register is used to configure Pin and Port Multiplexing.

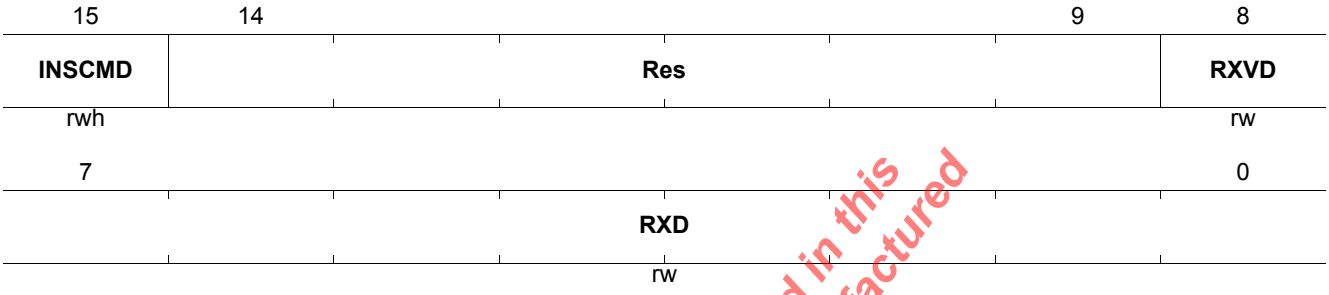
MII_MUX_CFG	Offset	Reset Value
Pin and Port Multiplexing Configuration	$F130_H$	0000_H

Field	Bits	Type	Description
PIE	9	rw	**Packet Insertion and Extraction Mode** This is to select packet insertion and extraction mode. 0_B **DIS** Packet insertion and extraction mode is disabled. 1_B **EN** Packet insertion and extraction mode is enabled. GSWIP port 6 is connected to packet insertion and extraction mode.
GPHY0_ISO	0	rw	**GPHY0 Isolation Mode** This is to enable or disable GPHY isolation mode. 0_B **DIS** Isolation mode is disabled, GPHY0 is connected to switch fabric. 1_B **EN** Isolation mode is enabled, GPHY0 is connected to RGMII5.

Packet Insertion Register

This register is used to insert packet to port 6.

PKT_INS	Offset	Reset Value
Packet Insertion Register	$F140_H$	0000_H

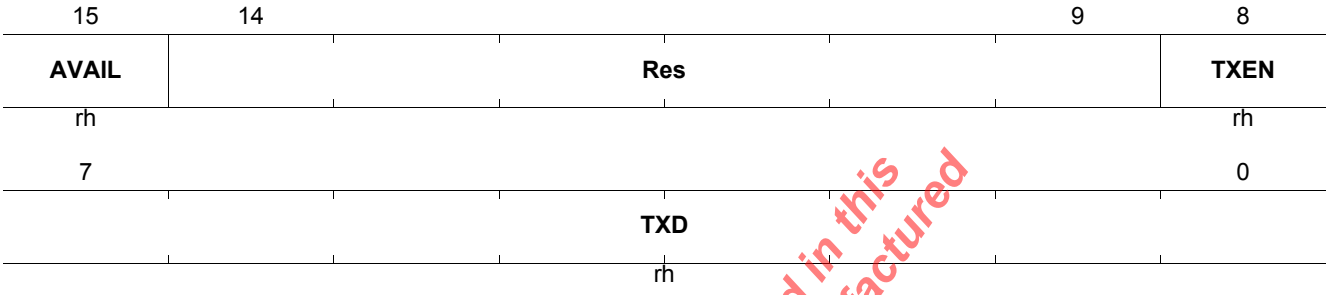


Field	Bits	Type	Description
INSCMD	15	rwh	**Packet Insertion Command** 0_B **NIL** Packet insertion is not triggered. 1_B **CMD** Start Packet insertion. CPU write '1' to this bit to trigger the insertion. This is a single cycle pulse and the bit is self clearing.
RXVD	8	rw	**RX Valid** This is to indicate if the data byte is valid or not. 0_B **GAP** The data byte is not valid. Writing IPG. 1_B **VLD** The data byte is valid. Wring Preamble, SFD and packet data.
RXD	7:0	rw	**RX Data** Data Byte to be inserted. Including IPG, Preamble, SFD and packet data.

Packet Extraction Read Register

This register is used to extract packet from port 6.

PKT_EXT_READ	Offset	Reset Value
Packet Extraction Read Register	$F141_H$	0000_H

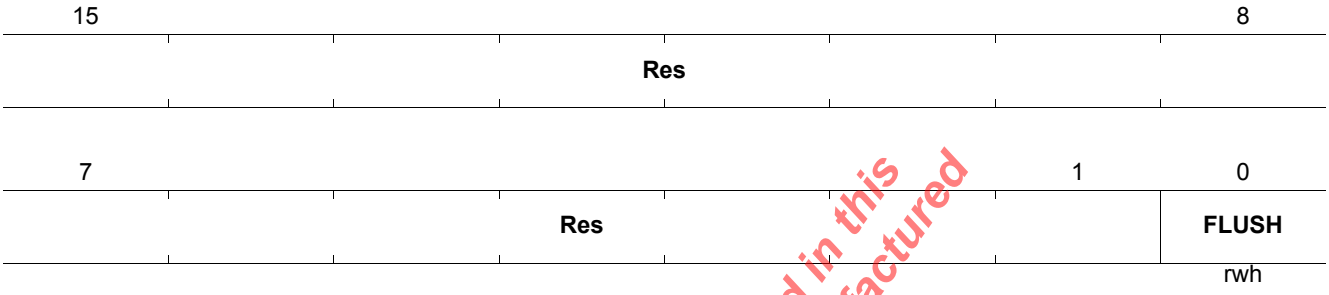


Field	Bits	Type	Description
AVAIL	15	rh	**Packet Available** This is to indicate a new packet is available to be extracted. When packet available, an interrupt is set. 0_B **NAVL** Packet is not available to be available. 1_B **AVL** Packet is available to be available.
TXEN	8	rh	**TX Data Valid** This is to indicate the extracted data byte is valid 0_B **NIL** The extracted byte is not valid 1_B **EN** The extracted byte is valid.
TXD	7:0	rh	**TX Data** Data byte extracted.

Packet Extraction Command Register

This register is used to extract packet from port 6.

PKT_EXT_CMD	Offset	Reset Value
Packet Extraction Command Register	$F142_H$	0000_H

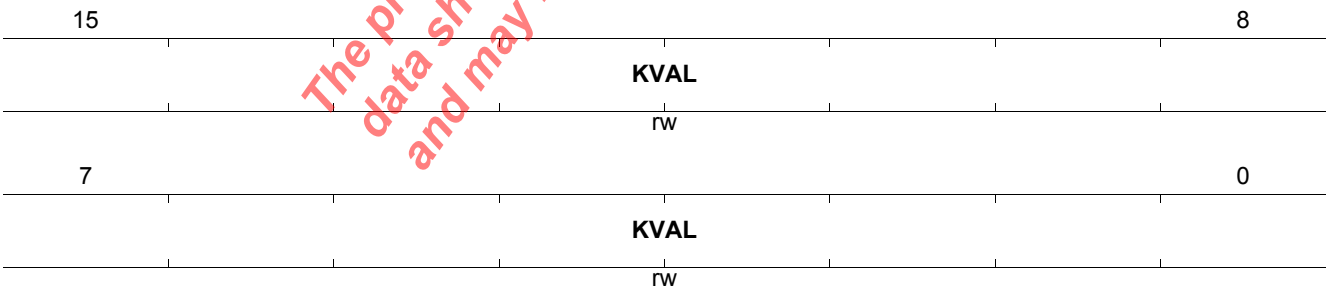


Field	Bits	Type	Description
FLUSH	0	rwh	**Packet Extraction Flush Command** This is to indicate to flush the rest of the current packet 0_B **NIL** The flush command is not triggered 1_B **CMD** The flush command is triggered. This bit is self-clearing and it is cleared until the flush of the current packet is done.

PCDU5 TX K Value Register

This register is used to configure TX K value.

PCDU5_TX_KVAL	Offset	Reset Value
PCDU5 TX K Value	$F160_H$	0040_H



Field	Bits	Type	Description
KVAL	15:0	rw	**K Value for TX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_TX_KVAL** defined above.

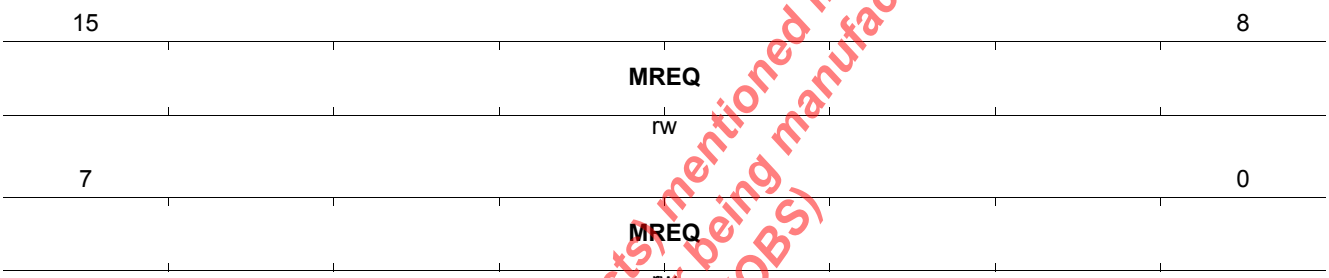
Table 54 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_TX_KVAL	PCDU6 TX K Value Register	$F170_H$	

PCDU5 TX M Required Register

This register is used to configure TX M Required.

PCDU5_TX_MREQ **Offset** **Reset Value**
PCDU5 TX M Required **$F161_H$** **0000_H**



Field	Bits	Type	Description
MREQ	15:0	rw	**M Required for TX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_TX_MREQ** defined above.

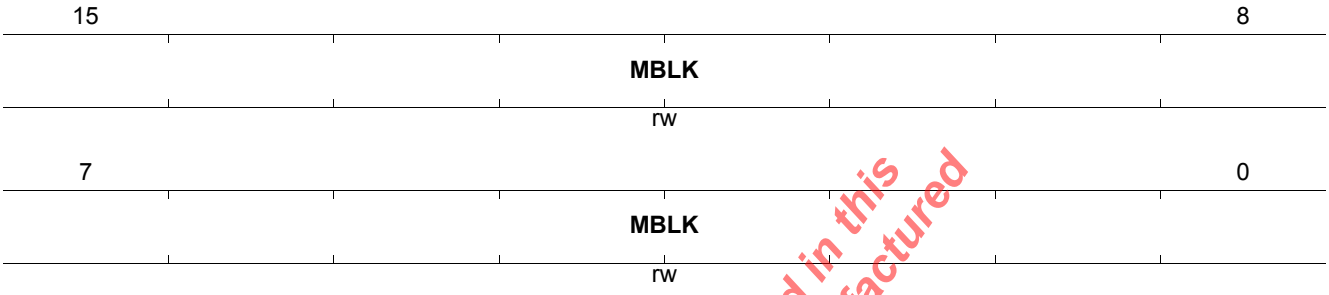
Table 55 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_TX_MREQ	PCDU6 TX M Required Register	$F171_H$	

PCDU5 TX M Blank Register

This register is used to configure TX M Blank.

PCDU5_TX_MBLK	Offset	Reset Value
PCDU5 TX M Blank	$F162_H$	0002_H



Field	Bits	Type	Description
MBLK	15:0	rw	**M Blank for TX Delay Path**

Similar Registers

The following registers are identical to the Register PCDU5_TX_MBLK defined above.

Table 56 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_TX_MBLK	PCDU6 TX M Blank Register	$F172_H$	

PCDU5 TX Delay Length Register

This register is used to configure TX Delay Length.

PCDU5_TX_DELLEN	Offset	Reset Value
PCDU5 TX Delay Length	$F163_H$	0000_H

Field	Bits	Type	Description
DEL_LEN	5:0	rh	**Delay Length for TX Delay Path**

Similar Registers

The following registers are identical to the Register PCDU5_TX_DELLEN defined above.

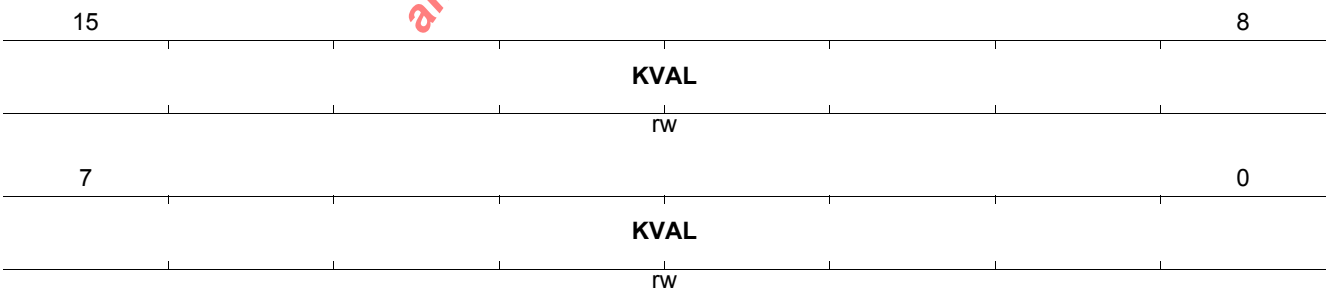
Table 57 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_TX_DELLEN	PCDU6 TX Delay Length Register	$F173_H$	

PCDU 5 RX K Value Register

This register is used to configure RX K value.

PCDU5_RX_KVAL	Offset	Reset Value
PCDU5 RX K Value	$F168_H$	0040_H



Field	Bits	Type	Description
KVAL	15:0	rw	**K Value for RX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_RX_KVAL** defined above.

Table 58 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_RX_KVAL	PCDU6 RX K Value Register	$F178_H$	

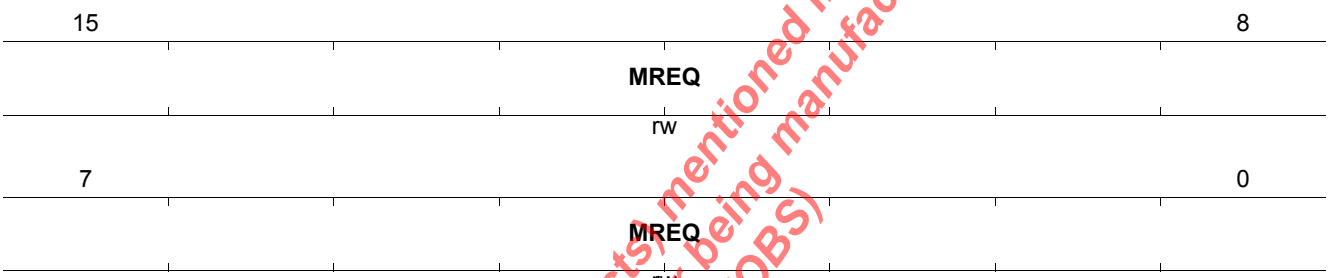
PCDU5 RX M Required Register

This register is used to configure RX M Required.

PCDU5_RX_MREQ — **PCDU5 RX M Required**

Offset $F169_H$

Reset Value 0000_H



Field	Bits	Type	Description
MREQ	15:0	rw	**M Required for RX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_RX_MREQ** defined above.

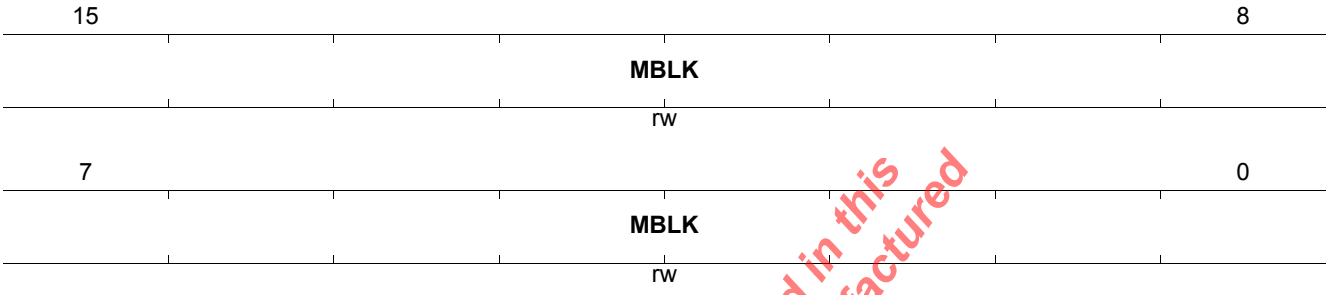
Table 59 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_RX_MREQ	PCDU6 RX M Required Register	$F179_H$	

PCDU5 RX M Blank Register

This register is used to configure RX M Blank.

PCDU5_RX_MBLK	Offset	Reset Value
PCDU5 RX M Blank	$F16A_H$	0002_H



Field	Bits	Type	Description
MBLK	15:0	rw	**M Blank for RX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_RX_MBLK** defined above.

Table 60 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_RX_MBLK	PCDU6 RX M Blank Register	$F17A_H$	

PCDU5 RX Delay Length Register

This register is used to configure RX Delay Length.

PCDU5_RX_DELLEN	Offset	Reset Value
PCDU5 RX Delay Length	$F16B_H$	0000_H

Field	Bits	Type	Description
DEL_LEN	5:0	rh	**Delay Length for RX Delay Path**

Similar Registers

The following registers are identical to the Register **PCDU5_RX_DELLEN** defined above.

Table 61 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCDU6_RX_DELLEN	PCDU6 RX Delay Length Register	$F17B_H$	

4.1.3 MDIO Master Registers

This chapter provides the registers that are needed to control the MDIO Master Interface.

GSWIP Configuration Register

This register is used to configuration GSWIP port enable and disable.

GSWIP_CFG	Offset	Reset Value
GSWIP Configuration Register	$F400_H$	0000_H

15	14	13	12	11	10	9	8
SE	P6	P5	P4	P3	P2	P1	P0
rw	rw	rw	rw	rw	rw	rw	rw

7					2	1	0
Res						HWRES	SWRES
						rwh	rwh

Field	Bits	Type	Description
SE	15	rw	**Global Switch Macro Enable** If set to OFF, the switch macro is inactive and frame forwarding is disabled.Register configuration and memory access is enabled in the OFF state.A register programming must activate the switch by setting this bit.This is used for setting all relevant registers before enabling the data traffic **Constants** 0_B **Disable** Macro is disabled 1_B **Enable** Macro is enabled
P6	14	rw	**Port 6 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P5	13	rw	**Port 5 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P4	12	rw	**Port 4 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P3	11	rw	**Port 3 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled

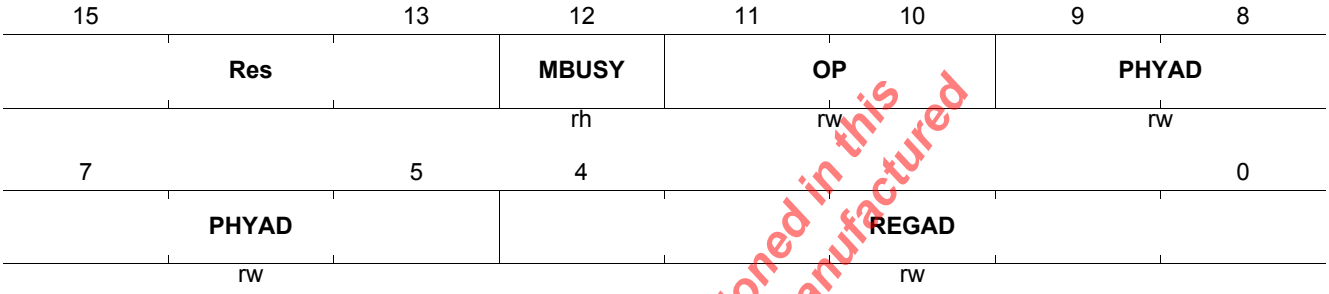
Field	Bits	Type	Description
P2	10	rw	**Port 2 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P1	9	rw	**Port 1 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P0	8	rw	**Port 0 Disable Configuration** **Constants** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
HWRES	1	rwh	**Global Switch Macro Hardware Reset** Reset all hardware modules including the register settings. This reset acts similar to the hardware reset and is cleared by HW after Reset is executed. **Constants** 0_B **OFF** reset is off 1_B **ON** reset is active
SWRES	0	rwh	**Global Switch Macro Software Reset** Reset all GSWIP hardware modules excluding the register settings.This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. **Constants** 0_B **OFF** reset is off 1_B **ON** reset is active

MDIO Master Indirect Control Register

This register is used to access devices that are connected to the serial MDIO master interface, internally or externally.

Each write access to this register starts a transmission, either read or write.

MMDIO_CTRL	Offset	Reset Value
MDIO Master Control Register	$F408_H$	0000_H

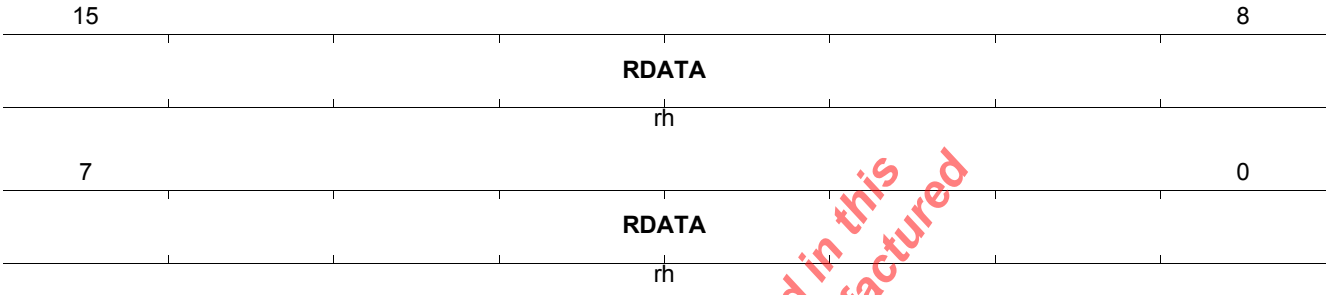


Field	Bits	Type	Description
MBUSY	12	rh	**MDIO Busy** This bit is set by hardware upon each write access to the register, which starts a transmission. As soon as a new command can be accepted, this bit is cleared by hardware. During write access, this bit is ignored and can be written to either value, 0 or 1. **Constants** 0_B **IDLE** the bus is available 1_B **BUSY** the bus is busy
OP	11:10	rw	**Operation Code** Selects the operation command. The value is directly mapped into the serial access frame. **Constants** 00_B **RES0** reserved, do not use 01_B **WR** write access 10_B **RD** read access 11_B **RES3** reserved, do not use
PHYAD	9:5	rw	**PHY Address** PHY address of the target device. The value is directly mapped into the serial access frame.
REGAD	4:0	rw	**Register Address** Register address in the target device. The value is directly mapped into the serial access frame.

MDIO Master Indirect Read Data Register

This register is used to read back data across the serial MDIO master interface, internally or externally.

MMDIO_READ	Offset	Reset Value
MDIO Master Read Data Register	$F409_H$	0000_H

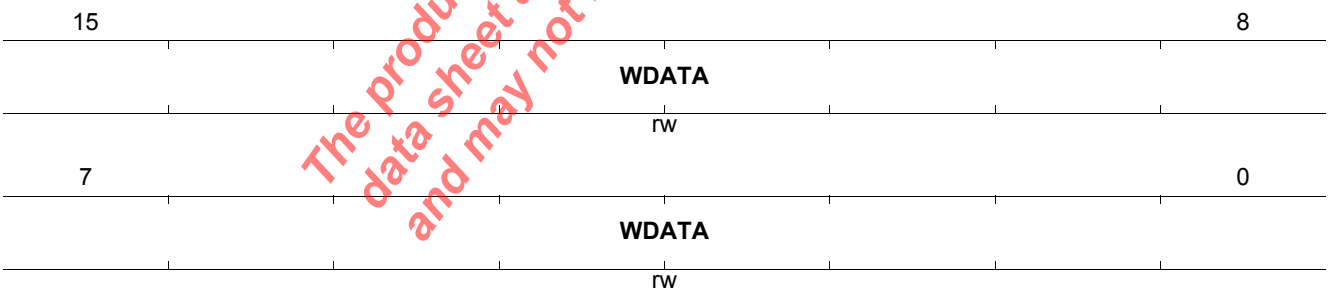


Field	Bits	Type	Description
RDATA	15:0	rh	**Read Data** A read access is triggered by writing to MDIO_CTRL (OP = RD, MBUSY = BUSY). After MBUSY = IDLE, data can be read.

MDIO Master Indirect Write Data Register

This register is used to write data across the serial MDIO master interface, internally or externally.

MMDIO_WRITE	Offset	Reset Value
MDIO Master Write Data Register	$F40A_H$	0000_H

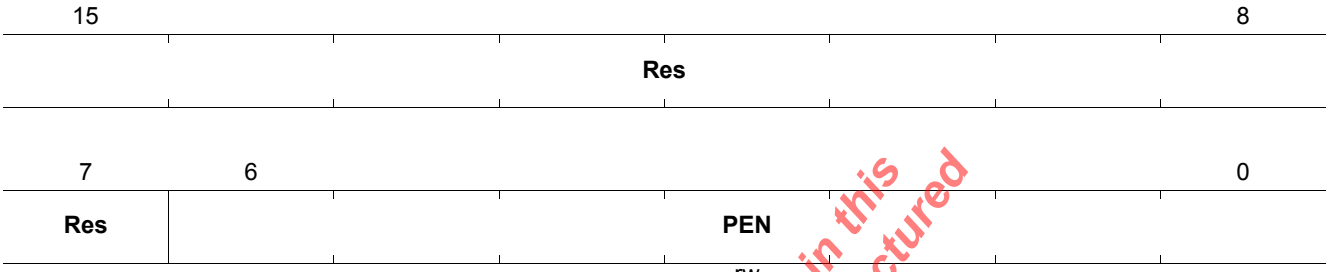


Field	Bits	Type	Description
WDATA	15:0	rw	**Write Data** A write access is triggered by writing to MDIO_CTRL (OP = WR, MBUSY = BUSY). This register must be written before the write command is given.

MDC Master Configuration Register 0

This register is used to control the MDC clock output and polling state machine.

MMDC_CFG_0	Offset	Reset Value
MDC Master Clock Configuration Register 0	$F40B_H$	$007F_H$

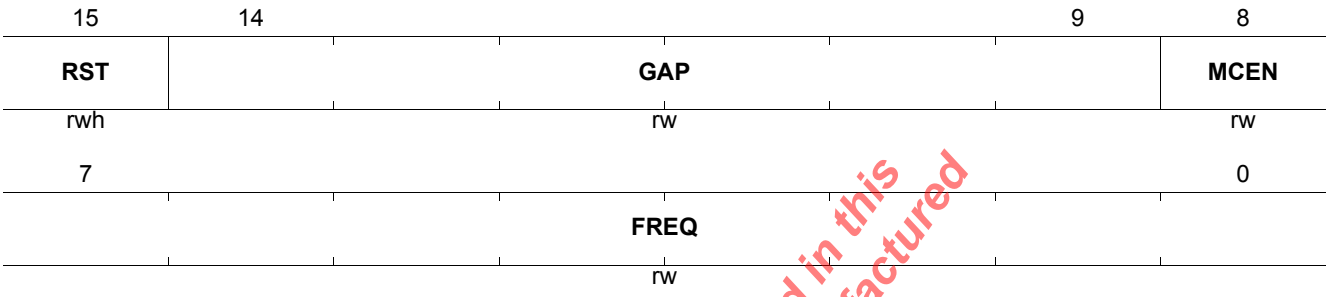


Field	Bits	Type	Description
PEN	6:0	rw	**Polling State Machine Enable** Enables the state machine to read PHY information automatically on this port. Unused ports should be disabled to reduce the polling latency. **Constants** 0_B **DIS** automatic PHY polling is disabled on this port 1_B **EN** automatic PHY polling is enabled on this port (default)

MDC Master Clock Configuration Register 1

This register is used to configure clocking rate for the MDIO master interfaces.

MMDC_CFG_1	Offset	Reset Value
MDC Master Clock Configuration Register 1	$F40C_H$	0109_H



Field	Bits	Type	Description
RST	15	rwh	**MDIO Hardware Reset** Reset all hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. **Constants** 0_B **OFF** reset is off 1_B **ON** reset is active
GAP	14:9	rw	**Autopolling Gap** This register configures the number of cycles between each auto-polling read access. The number of MDIO clock cycles is 256*GAP.
MCEN	8	rw	**Management Clock Enable** Enables the MDC clock driver. The driver can be disabled to save power if no external devices are connected to the MDIO master interface. If the MDC clock is disabled, the MDIO pad is switched to input mode and the MDIO drivers are also disabled. **Constants** 0_B **DIS** clock driver is disabled 1_B **EN** clock driver is enabled (default)

Field	Bits	Type	Description
FREQ	7:0	rw	**MDIO Interface Clock Rate** Selects the interface data and clock rate for the MDIO master interface. The MDC clock frequency calculates as: fMDC = Sys_clock_freq/5/((value + 1)*2). This frequency changes when system clock frequency changes. The following values are the frequencies when system clock is 250 MHz. **Constants** 00000000_B**S0** 25.0 MHz 00000001_B**S1** 12.50 MHz 00000010_B**S2** 8.333 MHz 00000011_B**S3** 6.250 MHz 00000100_B**S4** 5.000 MHz 00000101_B**S5** 4.167 MHz 00000110_B**S6** 3.571 MHz 00000111_B**S7** 3.125 MHz 00001000_B**S8** 2.778 MHz 00001001_B**S9** 2.500 MHz(default) 00001010_B**S10** 2.273 MHz 00001011_B**S11** 2.083 MHz 00001100_B**S12** 1.923 MHz 00001101_B**S13** 1.786 MHz 00001110_B**S14** 1.667 MHz 00001111_B**S15** 1.563 MHz 11111111_B**S255** 97.6 kHz

PHY Address Register PORT 0

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values

PHY_ADDR_0	Offset	Reset Value
PHY Address Register PORT 0	$F415_H$	1800_H

15	14	13	12	11	10	9	8
Res	LNKST		SPEED		FDUP		FCONTX
	rw		rw		rw		rw

7	6	5	4				0
FCONTX	FCONRX		ADDR				
rw	rw		rw				

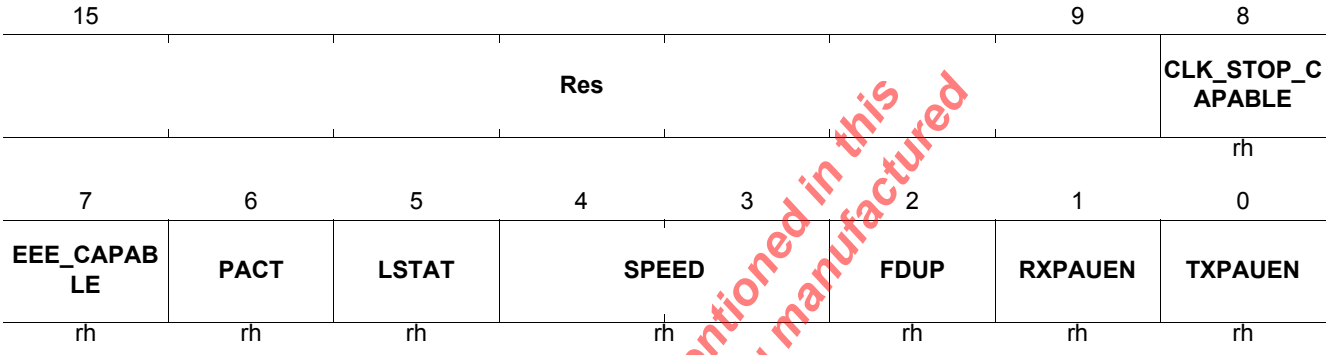
Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 9**.

PHY MDIO Polling Status per PORT

This register provides information about the current status of the attached Ethernet PHY retrieved by using the auto-polling process.

This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register.

MMDIO_STAT_0	Offset	Reset Value
PHY MDIO Polling Status per PORT	$F416_H$	0000_H



Field	Bits	Type	Description
CLK_STOP_CAPABLE	8	rh	**PHY supports TX Clock Stop** **Constants** 0_B **DIS** Clock stop is not supported 1_B **EN** Clock is supported
EEE_CAPABLE	7	rh	**PHY and link partner support EEE for current speed** **Constants** 0_B **DIS** EEE is not supported 1_B **EN** EEE is supported
PACT	6	rh	**PHY Active Status** Indicates if the external PHY is responding to MDIO accesses. This status information is retrieved from the attached Ethernet PHY by polling MDIO registers. **Constants** 0_B **INACTIVE** the PHY is inactive or not present 1_B **ACTIVE** the PHY is active and responds to MDIO accesses
LSTAT	5	rh	**Link Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. **Constants** 0_B **DOWN** the link is down 1_B **UP** the link is up
SPEED	4:3	rh	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps or above 11_B **RES** reserved

Field	Bits	Type	Description
FDUP	2	rh	**Full Duplex Status** Indicates if the attached PHY runs in half- or full-duplex mode. This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. **Constants** 0_B **HALF** half-duplex mode 1_B **FULL** full-duplex mode
RXPAUEN	1	rh	**Receive Pause Enable Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. **Constants** 0_B **DIS** the link partner does not send pause frames 1_B **EN** the link partner sends pause frames
TXPAUEN	0	rh	**Transmit Pause Enable Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. **Constants** 0_B **DIS** the link partner does not accept pause frames 1_B **EN** the link partner accepts pause frames

Similar Registers

The following registers are identical to the Register MMDIO_STAT_0 defined above.

Table 62 Similar Registers

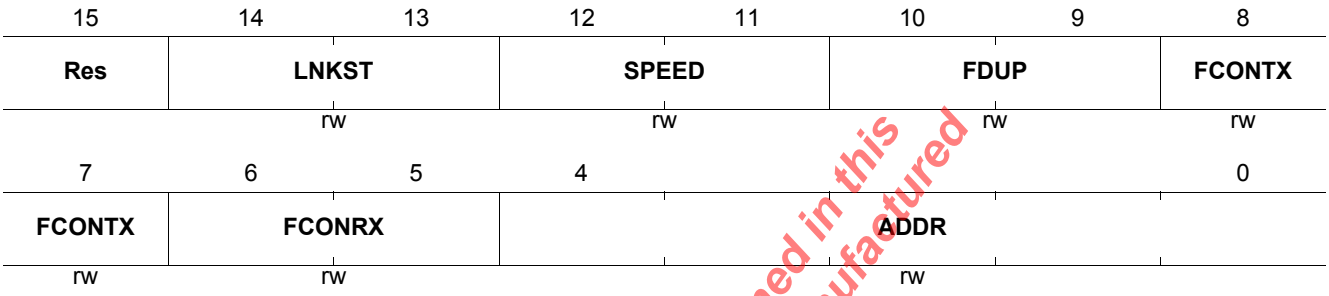
Register Short Name	Register Long Name	Offset Address	Page Number
MMDIO_STAT_1	PHY MDIO Polling Status per PORT 1	$F417_H$	
MMDIO_STAT_2	PHY MDIO Polling Status per PORT 2	$F418_H$	
MMDIO_STAT_3	PHY MDIO Polling Status per PORT 3	$F419_H$	
MMDIO_STAT_4	PHY MDIO Polling Status per PORT 4	$F41A_H$	
MMDIO_STAT_5	PHY MDIO Polling Status per PORT 5	$F41B_H$	
MMDIO_STAT_6	PHY MDIO Polling Status per PORT 6	$F41C_H$	

PHY Address Register PORT 1

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values

PHY_ADDR_1	Offset	Reset Value
PHY Address Register PORT 1	$F414_H$	1801_H



Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only

Field	Bits	Type	Description
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 9**.

PHY Address Register PORT 2

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values.

PHY_ADDR_2 — **Offset** $F413_H$ — **Reset Value** 1802_H

PHY Address Register PORT 2

15	14	13	12	11	10	9	8
Res	LNKST		SPEED		FDUP		FCONTX
	rw		rw		rw		rw

7	6	5	4				0
FCONTX	FCONRX		ADDR				
rw	rw		rw				

Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only

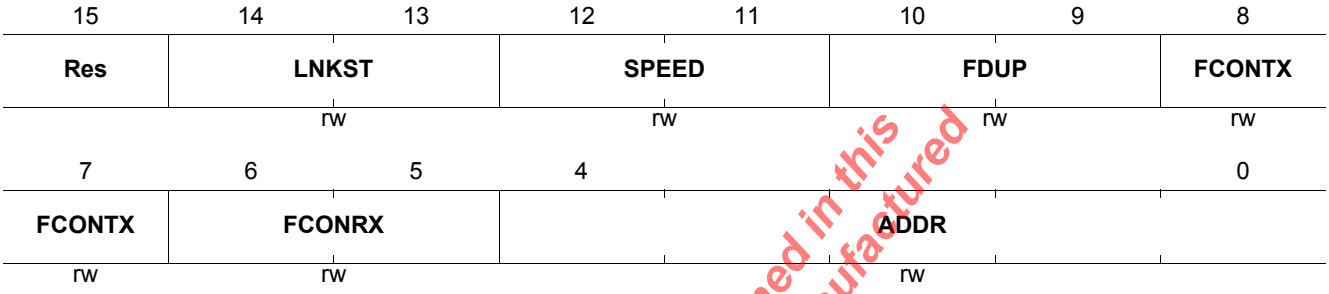
Field	Bits	Type	Description
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 9**.

PHY Address Register PORT 3

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values.

PHY_ADDR_3	Offset	Reset Value
PHY Address Register PORT 3	$F412_H$	1803_H



Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only

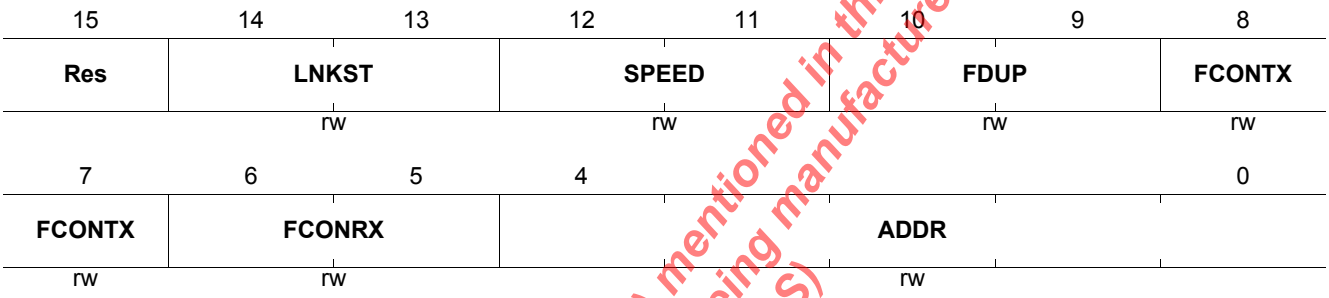
Field	Bits	Type	Description
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 9**.

PHY Address Register PORT 4

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values.

PHY_ADDR_4	Offset	Reset Value
PHY Address Register PORT 4	$F411_H$	1804_H



Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only

Field	Bits	Type	Description
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 9**.

PHY Address Register PORT 5

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values.

PHY_ADDR_5 **Offset** **Reset Value**

PHY Address Register PORT 5 **$F410_H$** **1805_H**

15	14	13	12	11	10	9	8
Res	LNKST		SPEED		FDUP		FCONTX
	rw		rw		rw		rw

7	6	5	4				0
FCONTX	FCONRX		ADDR				
rw	rw		rw				

Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode

Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on Table 9.

PHY Address Register PORT 6

This register is used to define the PHY address of the port.

If autopolling in MMDC_CFG_1 is disabled the modes defined here are used instead of the polling values.

PHY_ADDR_6 — **Offset** — **Reset Value**

PHY Address Register PORT 6 — **$F40F_H$** — **1806_H**

15	14	13	12	11	10	9	8
Res	LNKST		SPEED		FDUP		FCONTX
	rw		rw		rw		rw

7	6	5	4				0
FCONTX	FCONRX		ADDR				
rw	rw		rw				

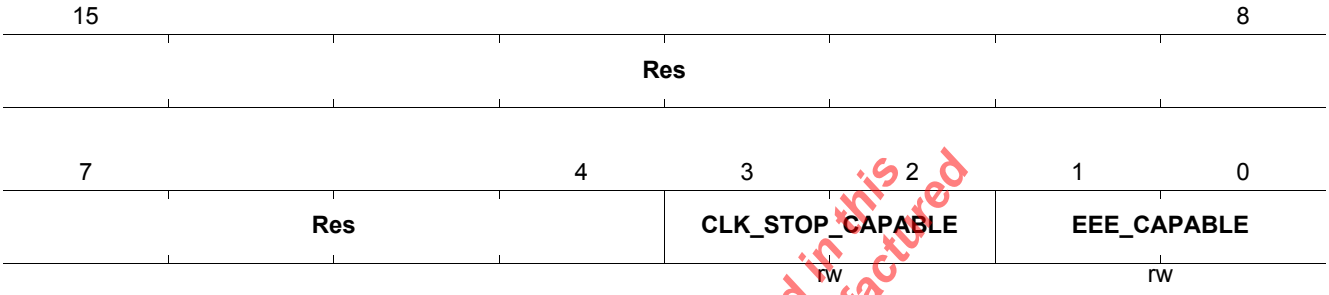
Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **UP** the link status is forced up 10_B **DOWN** the link status is forced down 11_B **RES** reserved, do not use
SPEED	12:11	rw	**Speed Control** **Constants** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** automatic mode detection by MDIO autopolling

Field	Bits	Type	Description
FDUP	10:9	rw	**Full Duplex Control** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** full duplex mode 10_B **RES** reserved 11_B **DIS** half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** **Constants** 00_B **AUTO** automatic mode detection by MDIO autopolling 01_B **EN** flow control in receive (ingress direction) only 10_B **RES** reserved 11_B **DIS** flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on Table 9.

EEE auto negotiation overrides

Override what is conveyed to the MAC from the auto negotiation with PHY.

ANEG_EEE_0	Offset	Reset Value
EEE auto negotiation overrides	$F41D_H$	0000_H



Field	Bits	Type	Description
CLK_STOP_CAPABLE	3:2	rw	**Clock Stop Capable** **Constants** 00_B **AUTO** automatic detection by autopolling 01_B **EN** force capable on 10_B **RES** reserved 11_B **DIS** force capable off
EEE_CAPABLE	1:0	rw	**EEE Capable** **Constants** 00_B **AUTO** automatic detection by auto polling 01_B **EN** force capable on 10_B **RES** reserved 11_B **DIS** force capable off

Similar Registers

The following registers are identical to the Register **ANEG_EEE_0** defined above.

Table 63 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
ANEG_EEE_1	EEE auto negotiation overrides	$F41E_H$	
ANEG_EEE_2	EEE auto negotiation overrides	$F41F_H$	
ANEG_EEE_3	EEE auto negotiation overrides	$F420_H$	
ANEG_EEE_4	EEE auto negotiation overrides	$F421_H$	
ANEG_EEE_5	EEE auto negotiation overrides	$F422_H$	
ANEG_EEE_6	EEE auto negotiation overrides	$F423_H$	

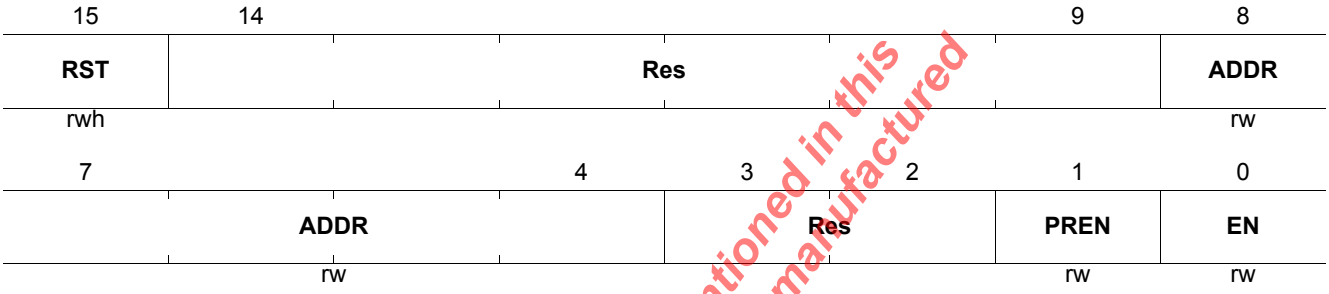
4.1.4 MDIO Slave Registers

This chapter provides the registers that are needed to control the MDIO slave interface.

MDIO Slave Configuration

This register is used to configure MDIO slave interface.

SMDIO_CFG	Offset	Reset Value
MDC Slave Configuration Register	$F480_H$	$01F1_H$

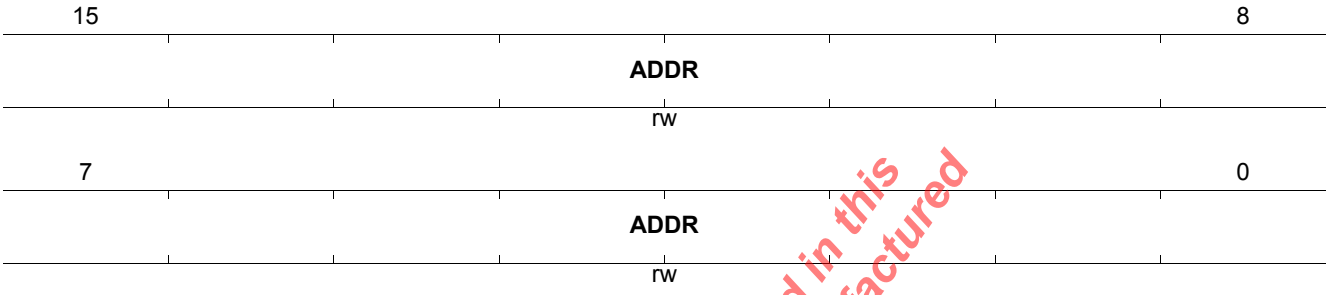


Field	Bits	Type	Description
RST	15	rwh	**MDIO Slave Hardware Reset** Reset all hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. **Constants** 0_B **OFF** reset is off 1_B **ON** reset is active
ADDR	8:4	rw	**SMDIO Address** This field defined SMDIO address. SMDIO responds to the access of this address.
PREN	1	rw	**SMDIO 32-bit Preamble Enable** **Constants** 0_B **DIS** Any preamble length can be accepted. 1_B **EN** Only 32-bit preamble length can be accepted.
EN	0	rw	**SMDIO Interface Enable** **Constants** 0_B **DIS** SMDIO Slave interface is disabled. 1_B **EN** SMDIO Slave interface is enabled.

MDIO Slave Target Base Address

This register is used to configure MDIO slave target base address.

SMDIO_BADR	Offset	Reset Value
MDC Slave Target Base Address Register	$F481_H$	0000_H



Field	Bits	Type	Description
ADDR	15:0	rw	**Target Base Address** It stores the target base address. For MDIO slave access, the address of target register is target base address + 5-bit offset address [in SMDIO REGADDR]. This register's SMDIO REGADDR is $1F_H$.

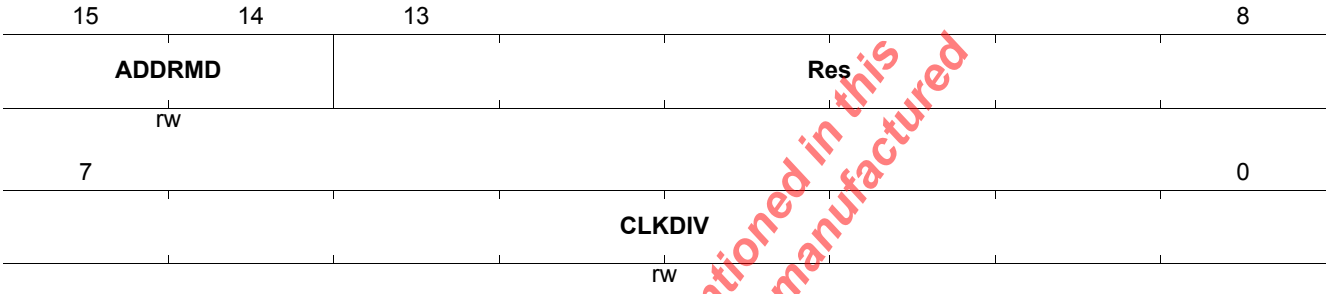
4.1.5 SPI Master Registers

This chapter provides the registers that are needed for SPI master interface.

SPI Master Interface Configuration

This register is used to configure SPI master interface mode.

MSPI_CFG	Offset	Reset Value
SPI Master Interface Configuration Register	$F510_H$	8019_H



Field	Bits	Type	Description
ADDRMD	15:14	rw	**SPI Master Addressing Mode** This bit specifies SPI master interface addressing mode. **Constants** 00_B **9-bit** SPI master interface is in 9-bit address mode. 01_B **16-bit** SPI master interface is in 16/17-bit address mode. 10_B **24-bit** SPI master interface is in 24-bit address mode. 11_B **24H-bit** SPI master interface is in 24-bit high speed access mode.
CLKDIV	7:0	rw	**SPI Clock Divider** This bit specifies SPI master interface clock divider. SPI clock is system core clock divided by this configuration. Frequency of SPI Clock = Sys_clock_freq/8/(CLKDIV+1)

SPI Master Operating Mode Configuration

This register is used to configure SPI master interface operating mode.

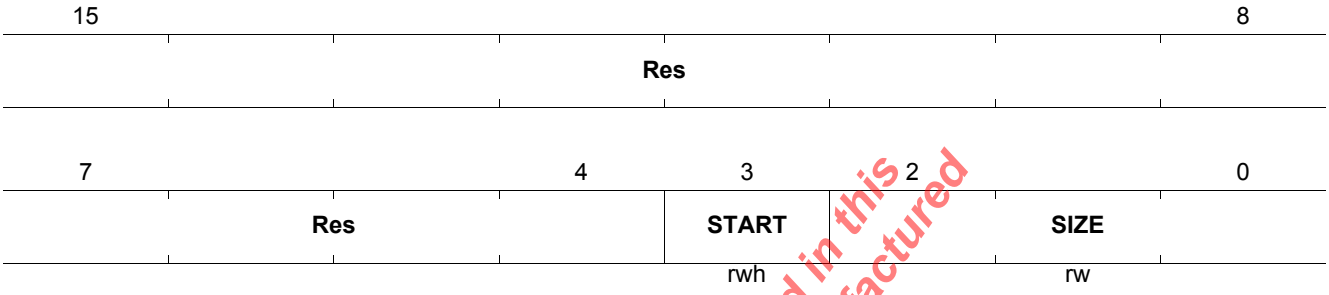
MSPI_OP	Offset	Reset Value
SPI Master Operating Mode Configuration Register	$F511_H$	0000_H

Field	Bits	Type	Description
BUSY	2	rh	**SPI Master Transaction Ongoing** This bit tells SPI master transaction status. **Constants** 0_B **IDLE** There is no ongoing SPI master transaction. 1_B **PEND** Pending request of manual mode is acknowledged.
MDSTA	1	rh	**SPI Master Operation Mode Status** This bit indicates SPI master operation mode status. **Constants** 0_B **AUTO** SPI master is in Auto operation mode. 1_B **MANU** SPI master is in manual operation mode.
MDSEL	0	rw	**SPI Master Operation Mode Selection** This bit specifies SPI manual or auto operation mode selection. The changing of this bit triggers the operation mode change request. Manual mode operation can be started when operation mode status is changed to manual mode. **Constants** 0_B **AUTO** Auto operation mode is selected. 1_B **MANU** Manual operation mode is selected.

SPI Master Manual Mode Control

This register is used to control SPI master manual mode transaction.

MSPI_MANCTRL	Offset	Reset Value
SPI Master Manual Mode Control Register	$F512_H$	0000_H

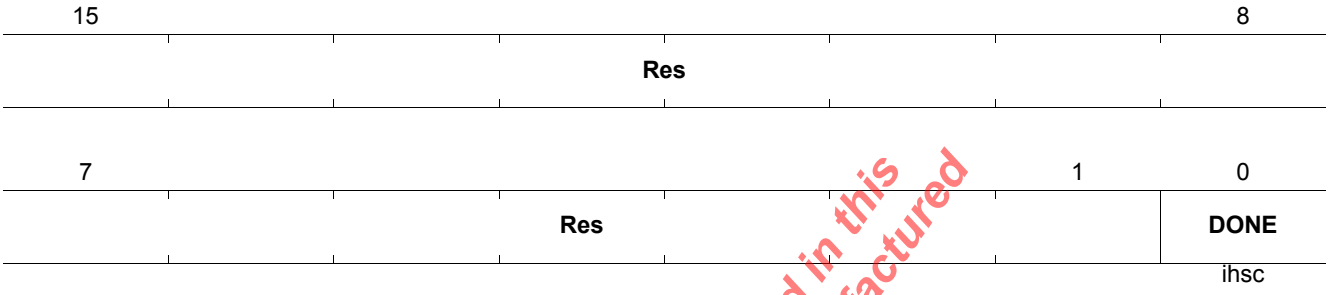


Field	Bits	Type	Description
START	3	rwh	**SPI Manual Mode Transaction Start Request** This bit triggers SPI manual mode transaction to start. Wring to '1' to triggers the manual mode transaction. When the transaction is done, this bit is clear by hardware automatically **Constants** 0_B **NIL** There is no ongoing manual mode transaction. 1_B **START** Manual mode transaction is started and ongoing.
SIZE	2:0	rw	**SPI Manual Mode Transaction Size** Size of SPI transaction in Bytes (actual size = t_size +1), i.e. 0: size = 1 Byte, 7: size = 8 Byte

SPI Master Interrupt Status Register

This register is used to hold SPI interrupt status.

MSPI_ISR	Offset	Reset Value
SPI Master Interrupt Status Register	$F513_H$	0000_H

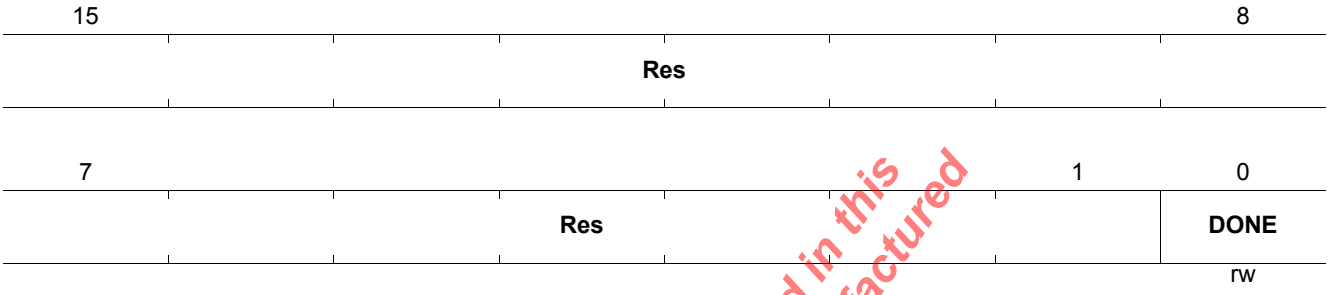


Field	Bits	Type	Description
DONE	0	lhsc	**SPI Manual Operation Transaction Done** This field holds SPI manual operation mode transaction done interrupt. **Constants** 0_B **NONE** Done interrupt is not triggered. 1_B **DONE** Done interrupt is triggered.

SPI Master Interrupt Enable Register

This register is used to specify SPI interrupt enable.

MSPI_IER	Offset	Reset Value
SPI Master Interrupt Enable Register	$F514_H$	0000_H

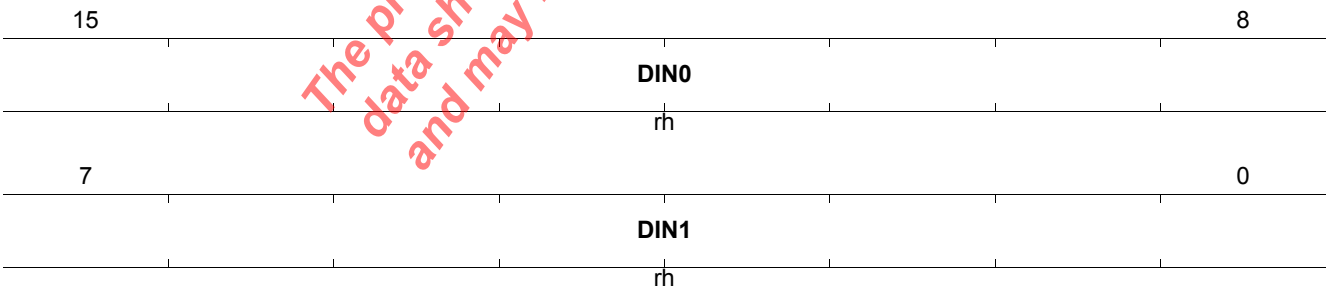


Field	Bits	Type	Description
DONE	0	rw	**SPI Access Done** This field specifies SPI access done interrupt enable **Constants** 0_B **DIS** Access Done interrupt is disabled. 1_B **EN** Access Done interrupt is enabled.

SPI Master Data In 0/1 Register

This register is used to store SPI data in byte 0 and 1.

MSPI_DIN01	Offset	Reset Value
SPI Master Data In 0/1 Register	$F518_H$	0000_H

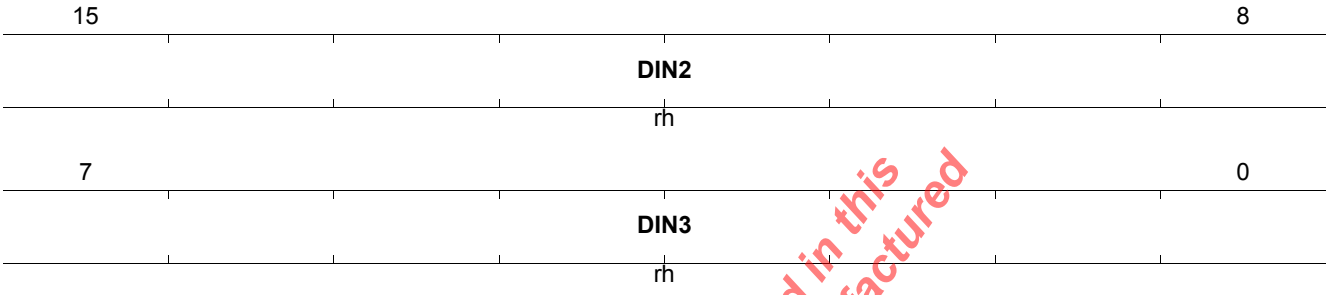


Field	Bits	Type	Description
DIN0	15:8	rh	**SPI Data In Byte 0** This field holds byte 0 (first byte) of the latest read transaction.
DIN1	7:0	rh	**SPI Data In Byte 1** This field holds byte 1 of the latest read transaction.

SPI Master Data In 2/3 Register

This register is used to store SPI data in byte 2 and 3.

MSPI_DIN23	Offset	Reset Value
SPI Master Data In 2/3 Register	$F519_H$	0000_H

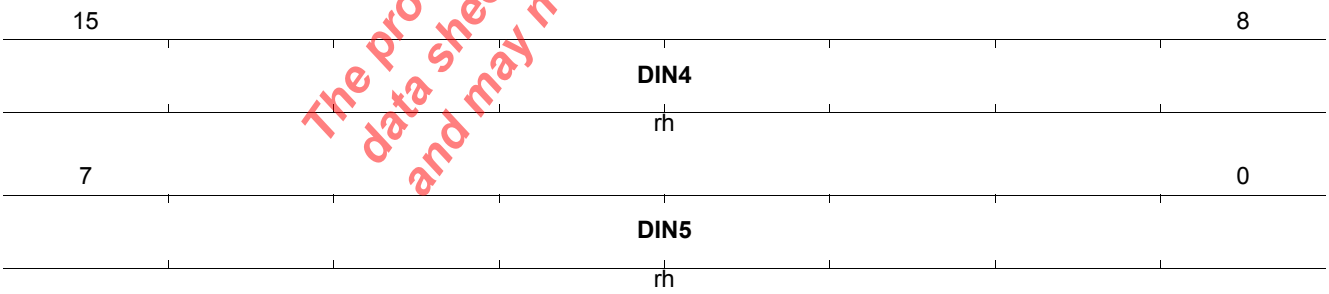


Field	Bits	Type	Description
DIN2	15:8	rh	**SPI Data In Byte 2** This field holds byte 2 of the latest read transaction.
DIN3	7:0	rh	**SPI Data In Byte 3** This field holds byte 3 of the latest read transaction.

SPI Master Data In 4/5 Register

This register is used to store SPI data in byte 4 and 5.

MSPI_DIN45	Offset	Reset Value
SPI Master Data In 4/5 Register	$F51A_H$	0000_H

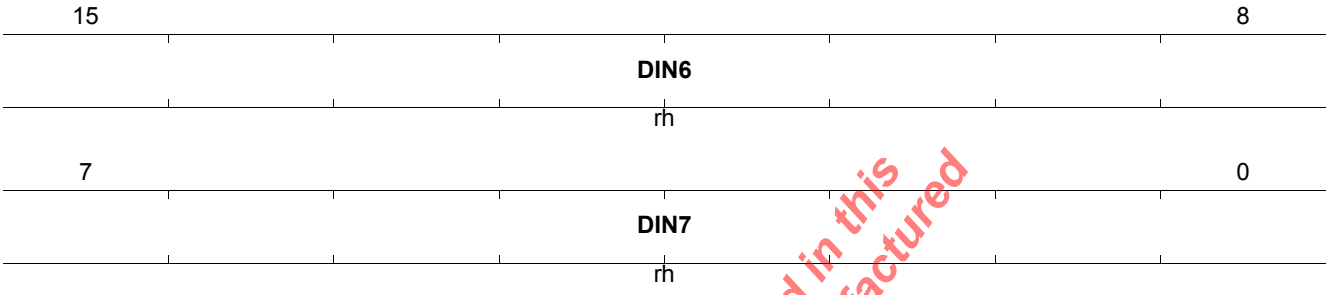


Field	Bits	Type	Description
DIN4	15:8	rh	**SPI Data In Byte 4** This field holds byte 4 of the latest read transaction.
DIN5	7:0	rh	**SPI Data In Byte 5** This field holds byte 5 of the latest read transaction.

SPI Master Data In 6/7 Register

This register is used to store SPI data in byte 6 and 7.

MSPI_DIN67	Offset	Reset Value
SPI Master Data In 6/7Register	$F51B_H$	0000_H

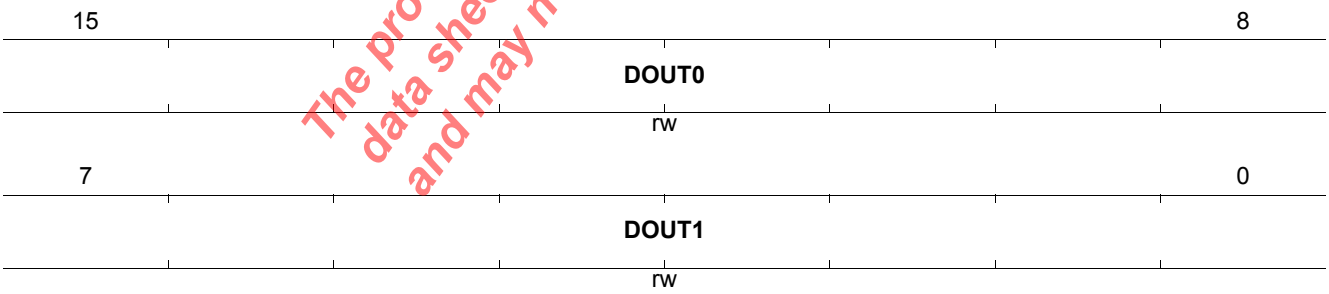


Field	Bits	Type	Description
DIN6	15:8	rh	**SPI Data In Byte 6** This field holds byte 6 of the latest read transaction.
DIN7	7:0	rh	**SPI Data In Byte 7** This field holds byte 7 of the latest read transaction.

SPI Master Data Out 0/1 Register

This register is used to store SPI data out byte 0 and 1.

MSPI_DOUT01	Offset	Reset Value
SPI Master Data Out 0/1 Register	$F51C_H$	0000_H

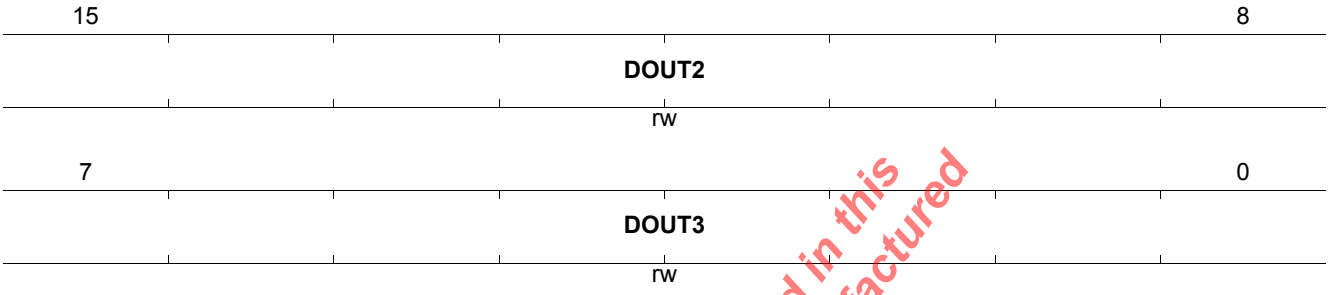


Field	Bits	Type	Description
DOUT0	15:8	rw	**SPI Data Out Byte 0** This field holds byte 0 (first byte) of the latest write transaction.
DOUT1	7:0	rw	**SPI Data Out Byte 1** This field holds byte 1 of the latest write transaction.

SPI Master Data Out 2/3 Register

This register is used to store SPI data out byte 2 and 3.

MSPI_DOUT23	Offset	Reset Value
SPI Master Data Out 2/3 Register	$F51D_H$	0000_H

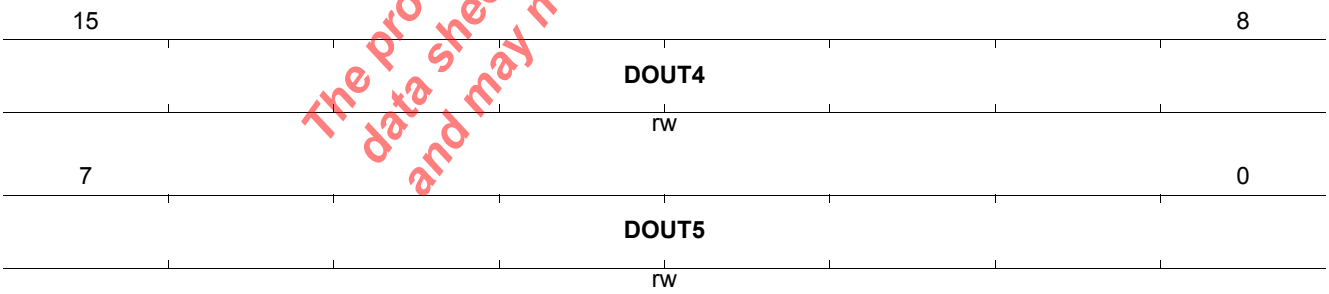


Field	Bits	Type	Description
DOUT2	15:8	rw	**SPI Data Out Byte 2** This field holds byte 2 of the latest write transaction.
DOUT3	7:0	rw	**SPI Data Out Byte 3** This field holds byte 3 of the latest write transaction.

SPI Master Data Out 4/5 Register

This register is used to store SPI data out byte 4 and 5.

MSPI_DOUT45	Offset	Reset Value
SPI Master Data Out 4/5 Register	$F51E_H$	0000_H

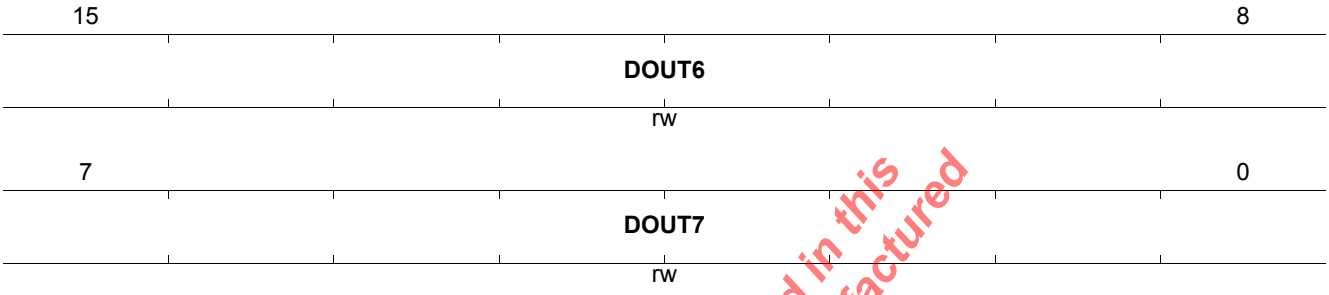


Field	Bits	Type	Description
DOUT4	15:8	rw	**SPI Data Out Byte 4** This field holds byte 4 of the latest write transaction.
DOUT5	7:0	rw	**SPI Data Out Byte 5** This field holds byte 5 of the latest write transaction.

SPI Master Data Out 6/7 Register

This register is used to store SPI data out byte 6 and 7.

MSPI_DOUT67	Offset	Reset Value
SPI Master Data Out 6/7 Register	$F51F_H$	0000_H



Field	Bits	Type	Description
DOUT6	15:8	rw	**SPI Data Out Byte 6** This field holds byte 6 of the latest write transaction.
DOUT7	7:0	rw	**SPI Data Out Byte 7** This field holds byte 7 of the latest write transaction.

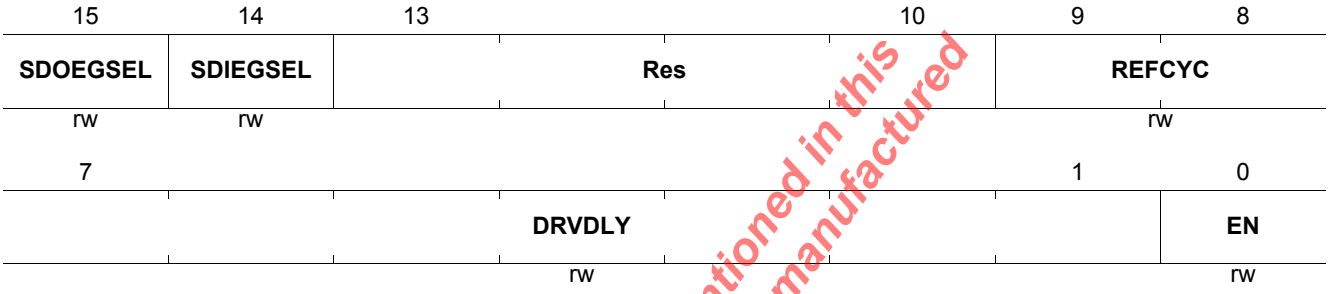
4.1.6 SPI Slave Registers

This chapter provides the registers that are needed for SPI slave interface.

SPI Slave Configuration Register

This register is used for SPI Slave Interface Configuration.

SSPI_CFG	Offset	Reset Value
SPI Slave Configuration Register	$F580_H$	0200_H



Field	Bits	Type	Description
SDOEGSEL	15	rw	**SDO Edge Select** This field selects the edge with which a SDO is driven out (e.g. if master expects with rising edge, driving should be at rising edge). **Constants** 0_B **FALL** SDO is driven at falling edge. 1_B **RISE** SDO is driven at rising edge.
SDIEGSEL	14	rw	**SDI Edge Select** This field selects the edge with which a SDI is sampled reliably (e.g. if master drives with rising edge, sampling should be set to falling, VERY IMPORTANT). **Constants** 0_B **FALL** SDI is sampled at falling edge. 1_B **RISE** SDI is sampled at rising edge.
REFCYC	9:8	rw	**SPI Slave Bus Reference Cycle** It specifies SDO output cycle adjustment, default value is 2, as to allow for adjustments up to 2 SCK clock cycles earlier.
DRVDLY	7:1	rw	**SPI Slave Bus Driver Delay** It specifies delay given in number of core clock cycles (please note that value 0 and 1 corresponds to about delay of 4 core clock cycles as seen from PAD).
EN	0	rw	**SPI Save Interface Enable** **Constants** 0_B **DIS** SPI Slave interface is disabled. 1_B **EN** SPI Slave interface is enabled.

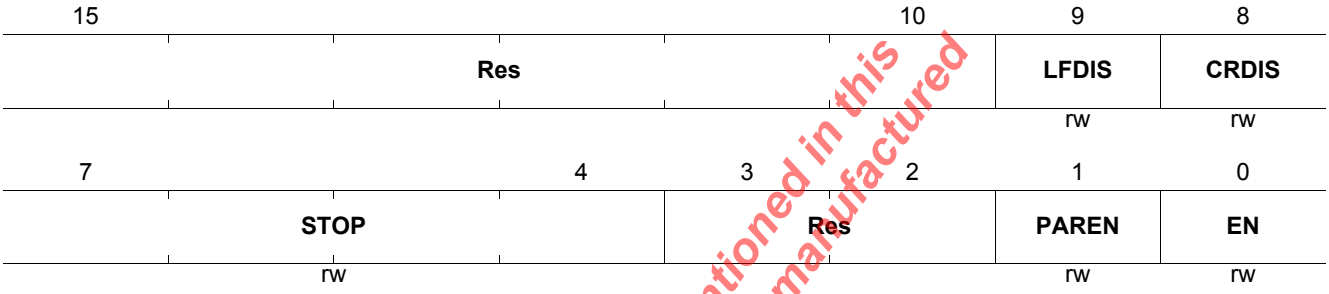
4.1.7 UART Registers

This chapter provides the registers that are needed for UART interface.

UART Configuration Register

This register is used for UART Configuration.

UART_CFG	Offset	Reset Value
UART Configuration Register	$F680_H$	0001_H

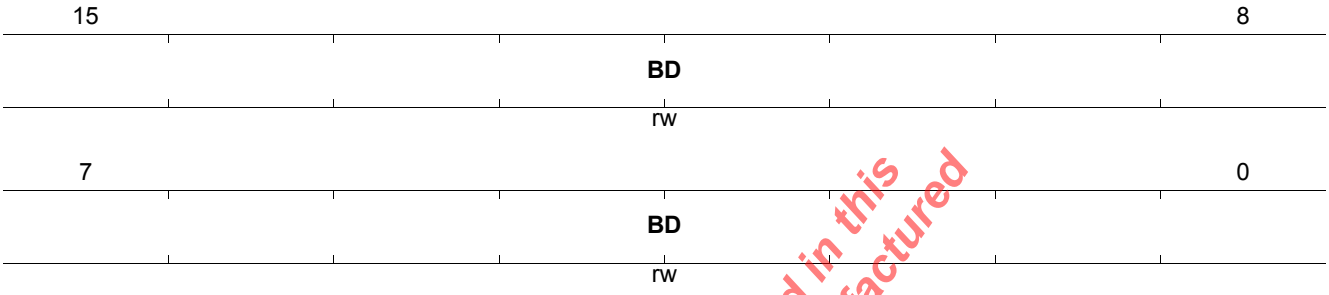


Field	Bits	Type	Description
LFDIS	9	rw	**LF As Enter Disable** **Constants** 0_B **EN** LF as “echoed enter” is enabled. 1_B **DIS** LF as “echoed enter” is disabled.
CRDIS	8	rw	**CR As Enter Disable** **Constants** 0_B **EN** CR as “echoed enter” is enabled. 1_B **DIS** CR as “echoed enter” is disabled.
STOP	7:4	rw	**Additional Stop Bits** The number of additional stop bits. The number of stop bits is 1 plus additional stop bits.
PAREN	1	rw	**UART Parity Enable** **Constants** 0_B **DIS** Parity is disabled. 1_B **EN** Parity is enabled.
EN	0	rw	**UART Interface Enable** **Constants** 0_B **DIS** UART interface is disabled. 1_B **EN** UART interface is enabled.

UART Baudrate Register

This register is used for UART Bautrate Configuration.

UART_BD	Offset	Reset Value
UART Baudrate Register	$F681_H$	$087A_H$

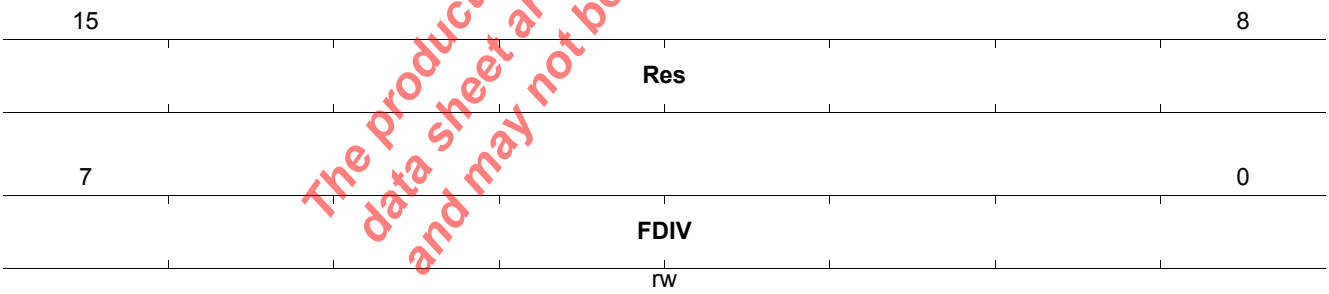


Field	Bits	Type	Description
BD	15:0	rw	**Baudrate Divider** This field shall be configured: round down 250M/baudrate to an integer.

UART Baudrate Fractional Divider Register

This register is used for UART Baudrate Fractional Divider Configuration.

UART_FDIV	Offset	Reset Value
UART Baudrate Fractional Divider Register	$F682_H$	0024_H

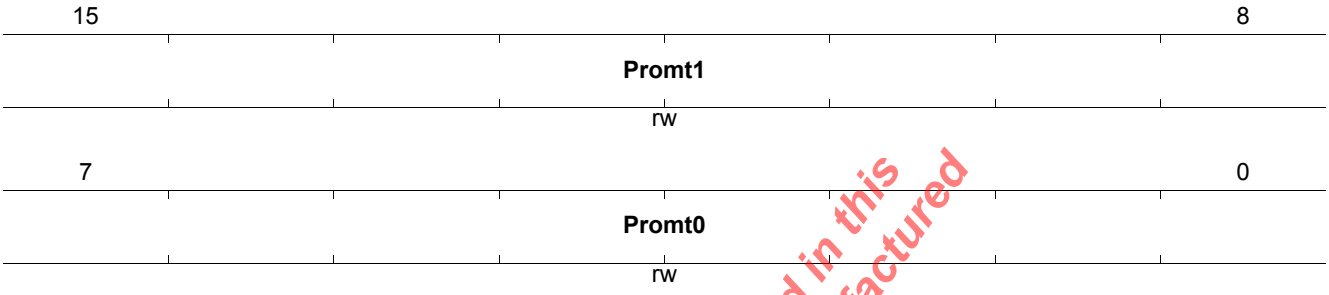


Field	Bits	Type	Description
FDIV	7:0	rw	**Baudrate Fractional Divider** The baudrate fractional divider is configured to: round up 256*(250M/baudrate - BD) to an integer

UART PROMPT Register

This register is used for UART Prompt.

UART_PROMPT	Offset	Reset Value
UART PROMPT Register	$F683_H$	$003E_H$

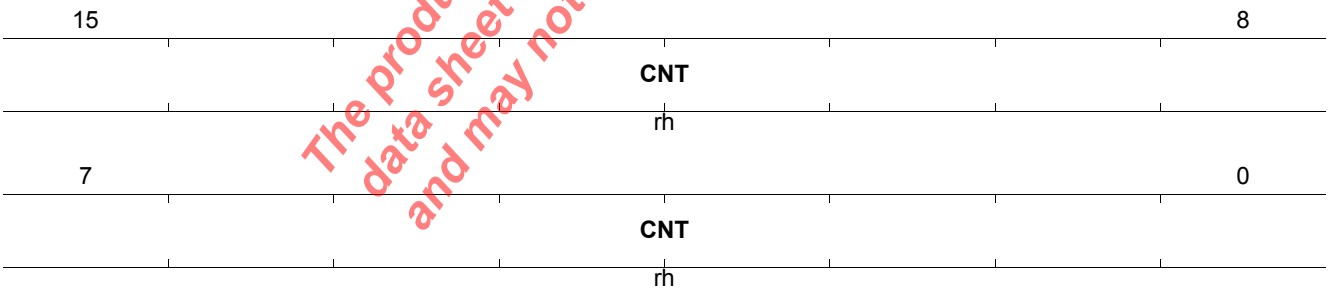


Field	Bits	Type	Description
Promt1	15:8	rw	**Second Prompt Character** If this field is 0, then second prompt character is disabled.
Promt0	7:0	rw	**First Prompt Character**

UART Error Counter Register

This register is used for UART Error Counter Register.

UART_ERRCNT	Offset	Reset Value
UART Error Counter Register	$F684_H$	0000_H



Field	Bits	Type	Description
CNT	15:0	rh	**Error Counter** Error Counter

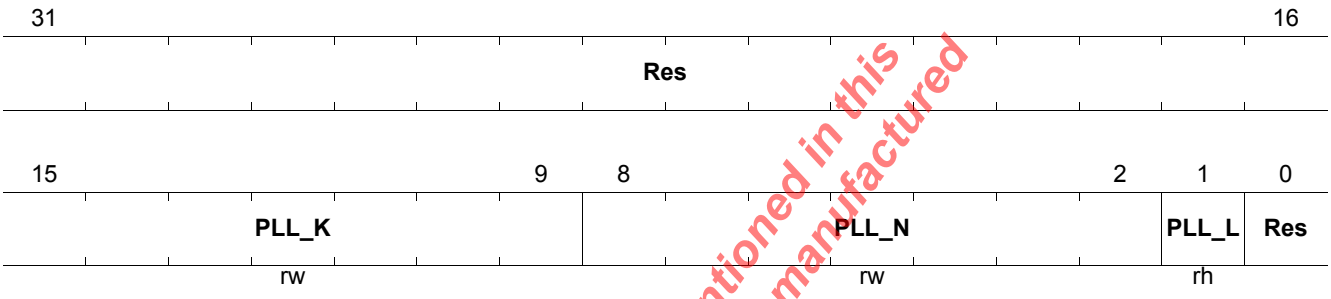
4.1.8 Clock Generation Unit Registers

This chapters describes all registers in CGU module.

SYS PLL Configuration 0 Register

It configures the SYS PLL. This register can not be reset by global software reset and module software reset.

SYSPLL_CFG0	Offset	Reset Value
SYS PLL Configuration 0 Register	$F980_H$	0140_H

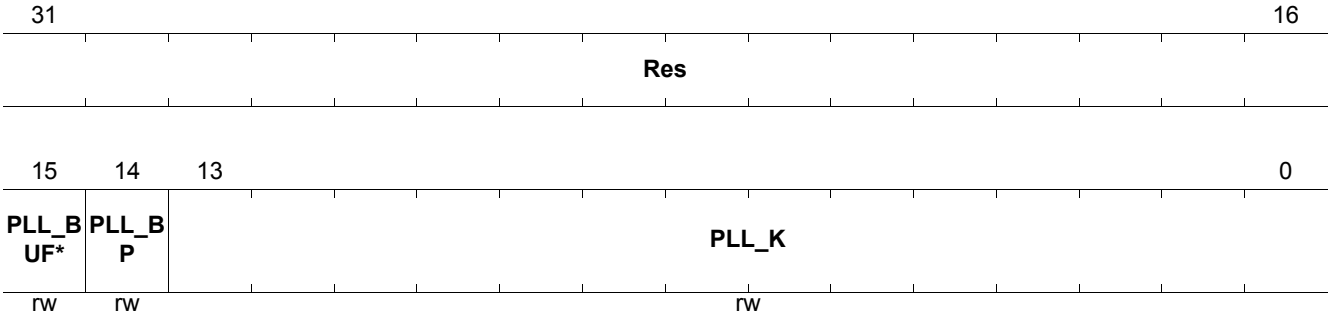


Field	Bits	Type	Description
PLL_K	15:9	rw	**PLL Fractional K Divider 6:0** PLL fractional K divider configuration.
PLL_N	8:2	rw	**PLL N Divider** PLL N divider configuration.
PLL_L	1	rh	**PLL Lock Status** PLL lock/unlock status information. 0_B **DISABLE** DisablePLL is not locked (default after reset). 1_B **ENABLE** EnablePLL is locked.

SYS PLL Configuration 1 Register

It configures the SYS PLL. This register can not be reset by global software reset and module software reset.

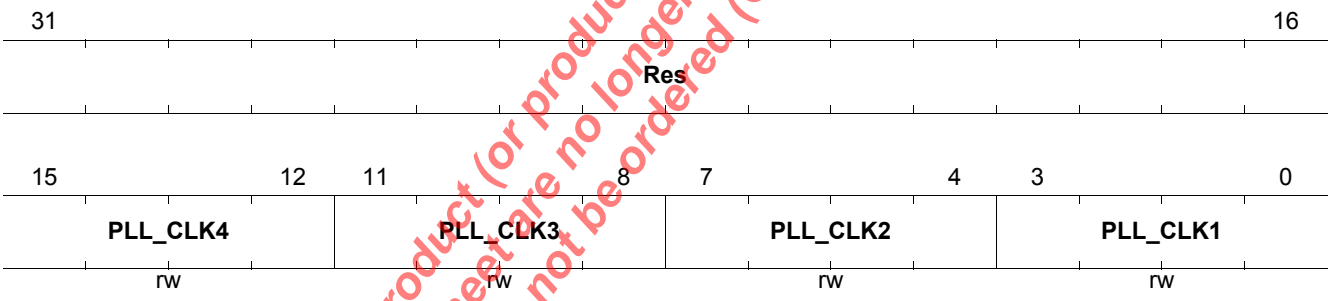
SYSPLL_CFG1	Offset	Reset Value
SYS PLL Configuration 1 Register	$F984_H$	0000_H



Field	Bits	Type	Description
PLL_BUFOUT	15	rw	**PLL CML input buffer** **PLL CML input buffered output enable. Disabled by default, this enable the CML clock buffer for CLKREF and supports buffered clock cascade on chip** 0_B **DSIABLE** DisableCML input buffered output disabled 1_B **ENABLE** EnableCML input buffered output enabled
PLL_BP	14	rw	**PLL Bypass** PLL bypass enable. 0_B **DISABLE** DisablePLL is enabled (default). 1_B **ENABLE** EnablePLL is bypassed.
PLL_K	13:0	rw	**PLL0 Fractional K Divider 20 to 7** PLL fractional K divider configuration. Default value is xx.

SYS PLL Configuration 2 Register

SYSPLL_CFG2	Offset	Reset Value
SYS PLL Configuration Register 2	$F988_H$	6666_H

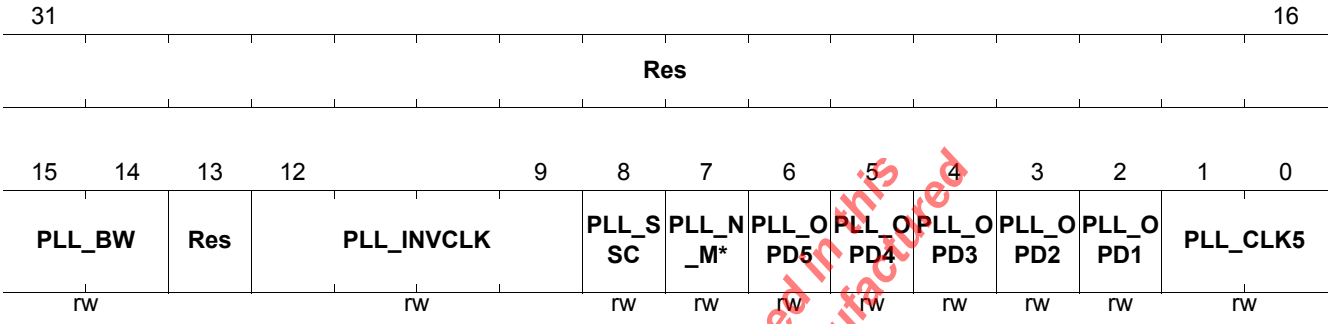


Field	Bits	Type	Description
PLL_CLK4	15:12	rw	**PLL Clock Output 4** PLL Clock output 4 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz
PLL_CLK3	11:8	rw	**PLL Clock Output 3** PLL Clock output 3 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz

Field	Bits	Type	Description (cont'd)
PLL_CLK2	7:4	rw	**PLL Clock Output 2** PLL Clock output 2 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz
PLL_CLK1	3:0	rw	**PLL Clock Output 1** PLL Clock output 1 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 1200 MHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 800 MHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 600 MHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 480 MHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 400 MHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 300 MHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 240 MHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 200 MHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 150 MHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 120 MHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 100 MHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 75 MHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 60 MHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 50 MHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz 37.5 MHz

SYS PLL Configuration 3 Register

SYSPLL_CFG3	Offset	Reset Value
SYS PLL Configuration Register 3	$F98C_H$	0140_H



Field	Bits	Type	Description
PLL_BW	15:14	rw	**PLL Bandwidth Select** PLL Bandwidth configuration.
PLL_INVCLK	12:9	rw	**PLL Invert Clock Enable** When '1' select the respective CLK1, CLK2, CLK3, CLK4 output buffer to be inverted as the output. 0_B **DIS** Inverter not enabled. 1_B **EN** Inverter enabled
PLL_SSC	8	rw	**PLL Spread Spectrum Mode** Configures the PLL N mode. 0_B **ENABLE** Enable Fractional input and SSC code is used. 1_B **DISABLE** Disable Ignores fractional and SS code
PLL_N_MODE	7	rw	**Integer N mode En** Integer-N Mode. When high, it ignores the fractional code and SSC code. **Constants** 0_B **FRAC** Fractional Mode with SSC 1_B **INT** Integer-N Mode only
PLL_OPD5	6	rw	**PLL CLK5 output buffer power down** Output Clock buffer power down for CLK5 **Constants** 0_B **NORMAL** buffer is active 1_B **PD** buffer is power down
PLL_OPD4	5	rw	**PLL CLK4 output buffer power down** Output Clock buffer power down for CLK4 **Constants** 0_B **NORMAL** buffer is active 1_B **PD** buffer is power down

Field	Bits	Type	Description (cont'd)
PLL_OPD3	4	rw	**PLL CLK3 output buffer power down** Output Clock buffer power down for CLK3 **Constants** 0_B **NORMAL** buffer is active 1_B **PD** buffer is power down
PLL_OPD2	3	rw	**PLL CLK2 output buffer power down** Output Clock buffer power down for CLK2 **Constants** 0_B **NORMAL** buffer is active 1_B **PD** buffer is power down
PLL_OPD1	2	rw	**PLL CLK1 output buffer power down** Output Clock buffer power down for CLK1 **Constants** 0_B **NORMAL** buffer is active 1_B **PD** buffer is power down
PLL_CLK5	1:0	rw	**PLL CML CLK5 output buffer frequency selection** PLL CLK5 CML output freq select **Constants** 00_B **DIV4** VCO Clock divide by 4 01_B **DIV6** VCO Clock divide by 6 10_B **DIV8** VCO Clock divide by 8 11_B **DIV12** VCO Clock divide by 12

SYSPLL Miscellaneous Control Register

SYSPLL_MISC **Offset** **Reset Value**

SYSPLL Miscellaneous Control Register **$F990_H$** **0022_H**

15	14	13	12	11	10	9	8
PSOVR	**UNLCK**	**FORCE**	**VEXT**	**EXTREF**	**LCKOVR**	**IPOK**	**IOPFSEL**
rw	ihsc	rwh	rw	rw	rw	rw	rw

7	6	5	4	3	2		0
INKSEL	**FPUP**	**CLKSEL**		**MODE**	**MPROG**		
rw	rw	rw		rw	rw		

Field	Bits	Type	Description
PSOVR	15	rw	**Pinstrap overwrite** When PSOVR='1' we can choose to overwrite the pin-strapped values (MODE, CLKSEL[1:0], INKSEL) with the content of this register.
UNLCK	14	ihsc	**Sticky bit for unlock status** This is a sticky bit status to detect if the PLL was ever unlock and then relock again. Write 1 to clear.

Field	Bits	Type	Description
FORCE	13	rwh	**Force Latching Of Shadow Registers** By default, all changes in the PDI registers shall not take effect until the next SRSTN. For debug purpose, this bit = '1' enable the user to force the latching without using the SRSTN. The changes can take immediate effect. This bit has a self-clearing behaviour to be implemented behind the rwh register type
VEXT	12	rw	**PLL output buffer power supply** PLL output buffer supply select signal - Selects between external 1.1 V supply, or internal Regulator supply to drive the output buffers. **Constants** 0_B **INT** Use Internally generated 1.1 V supply 1_B **EXT** Use Externally generated 1.1 V supply
EXTREF	11	rw	**Select External Reference Current** Select if we use external Reference Current or the internally generated one. **Constants** 0_B **INT** Use Internally generated REFERENCE BIASING current 1_B **EXT** Use Externally generated REFERENCE BIASING current
LCKOVR	10	rw	**PLL Lock Overwrite** When set to '1' force the ROPLL to assert lock state regardless of the lock detection status.
IPOK	9	rw	**Internal POK Override** Internal POK Override. This is for debug purpose and force the internal check of Power OK for 1V1 internal LDO power supply generation **Constants** 0_B **ENABLE** Internal check for Power OK state of the LDO 1_B **OVR** Internal Power OK module disabled
IOPFSEL	8	rw	**Selects if PLL internal digital allocates the default output frequencies.** Selects if PLL internal digital allocates the default output frequencies. When high, the ropll_op_freq_sel_clk1-4 pins are ignored. **Constants** 0_B **EXT** PDI selected output frequencies are used for CLK1-CLK4 1_B **INT** Internal LUT used for the CLK1-CLK4 frequency selection
INKSEL	7	rw	**Selects if PLL internal mapped N,K or based on PLL_CFG0/1 N,K** Selects the values of divider (int, frac) from the internal table lookup. When high, ignores the values of PLL_CFG1.K,PLL_CFG0.K, PLL_CFG1.N bits. Effective only when PSOVR=1. Otherwise according to pinstrap PS_XTAL.
FPUP	6	rw	**Force Power up of all Divider chains** Force Power up of all Divider chains. For debug purpose only **Constants** 0_B **NORMAL** Power up the divider chains according to mode select LUT 1_B **FORCE** All divider chain output are forced to power up

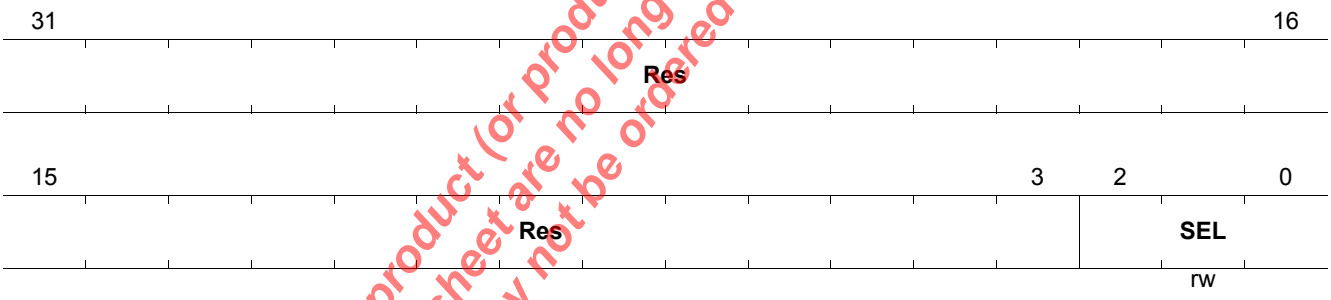
Field	Bits	Type	Description
CLKSEL	5:4	rw	**PLL input clock select** PLL input clock select - 25/40 MHz. Effective only when PSOVR=1. otherwise according to pinstrap PS_XTAL. **Constants** 01_B **XTAL40** RefCLK is 40 MHz 10_B **XTAL25** RefCLK is 25 MHz
MODE	3	rw	**Selects CML/CMOS input Clock** PLL input mode select - CML/CMOS. Effective only when PSOVR=1. otherwise always '0'. **Constants** 0_B **CML** CML differential input clock selected 1_B **CMOS** CMOS differential input clock selected
MPROG	2:0	rw	**PLL Mode Sel** PLL mode selection. Must be set to 2.

GPC0 Configuration Register

It configures general purpose clock 0.

GPC0_CONF — **Offset** — **Reset Value**

GPC0 Configuration Register — **$F948_H$** — **0000_H**



Field	Bits	Type	Description
SEL	2:0	rw	**GPC0 Output Clock Selection** This is to select output clock source. 101_B **CDB** clock output from CDB. 110_B **SYS2** The divided clock of the output clock 2 of SYS PLL. 111_B **SYS3** The divided clock of the output clock 3 of SYS PLL.

Similar Registers

The following registers are identical to the Register **GPC0_CONF** defined above.

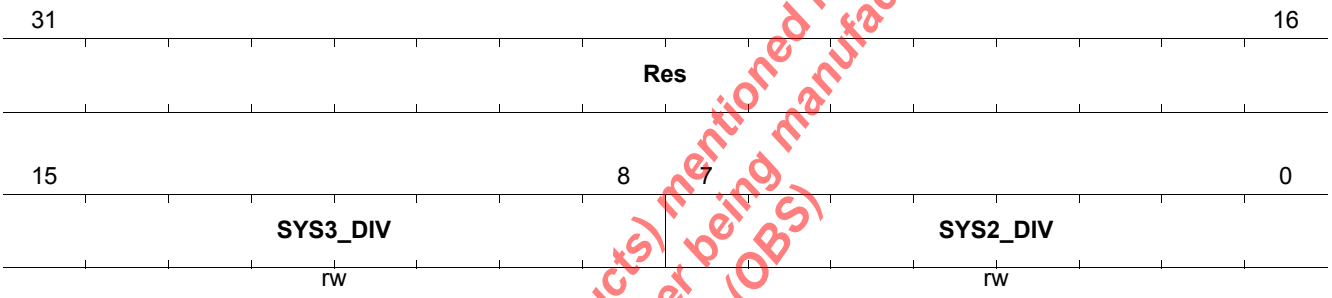
Table 64 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPC1_CONF	GPC1 Configuration Register	$F94C_H$	

SYSCLK Configuration Register

It configures sysclock divider.

SYSCLK_CONF	Offset	Reset Value
SYCCLK Configuration Register	$F950_H$	0000_H



Field	Bits	Type	Description
SYS3_DIV	15:8	rw	**SYS Clock 3 Divider Selection** If SYS is selected for GPC output, the output of SYS3 clock is divided before feeding to GPC. The divider is 2*(SYS3_DIV+1).
SYS2_DIV	7:0	rw	**SYS Clock 2 Divider Selection** If SYS is selected for GPC output, the output of SYS2 clock is divided before feeding to GPC. The divider is 2*(SYS2_DIV+1).

4.1.9 Reset Control Unit Registers

This chapters describes all registers in RCU module.

Reset Status Register

After a reset, the read-only reset status register RST_STAT indicates the type of reset that occurred and indicates which parts of the chip were affected by the reset.

RESET_STATUS	Offset	Reset Value
Reset Status Register	$FA00_H$	8000_H

15	14	13	12	11	10	9	8
HRST	RECORD						
rh	rw						

7	6	5	4	3	2	1	0
RECORD							INIT
rw							rw

Field	Bits	Type	Description
HRST	15	rh	**Hardware Reset Cause Flag** 0_B **SRST** The last reset is software reset. 1_B **HRST** The last reset is hardware reset.
RECORD	14:1	rw	**Last Reset Record** The value is not cleared by software reset.
INIT	0	rw	**Initialization Done Flag** **The value is not cleared by software reset.** 0_B **NO** Initialization is not done. 1_B **DONE** Initialization is done.

Reset Request Register

The Reset Request Register RST_REQ is used to generate a software reset. Unlike the other reset types, the software reset can exclude functions from reset. A software reset is invoked by writing ‘1’ to register RST_REQ.

RST_REQ	Offset	Reset Value
Reset Request Register	$FA01_H$	$002F_H$

15	14	13	12	11	10	9	8
SRST	RD14	Res	G0RST	Res	RD10	RD9	Res
rwh	rw		rwh		rw	rw	

7	6	5	4	3	2	1	0
RD7	RD6	Res	RD3	RD3	RD2	RD1	RD0
rw	rw		rw	rw	rw	rw	rw

Field	Bits	Type	Description
SRST	15	rwh	**Enable Global Software Reset** Configures the global software reset. Reset is automatically deactivated after some cycles. 0_B **Nil** Global software reset is not issued. 1_B **REQ** Global software reset is triggered.
RD14	14	rw	**Reset Request for Reset Domain RD14** Configures the reset domain 14. Software to decide the required duration. Software reset MGE module. MGE reset type 2 resets all logics excluding register file in MGE module. 0_B **Disabled** MGE software reset type 2 is disabled. 1_B **Enabled** MGE software reset type 2 is enabled.
G0RST	12	rwh	**Enable GPHY0 Reset** Configures the GPHY0 reset. Reset is automatically deactivated after some cycles. 0_B **Nil** GPHY0 reset is not issued. 1_B **REQ** GPHY0 reset is triggered.
RD10	10	rw	**Reset Request for Reset Domain RD10** Configures the reset domain 10. Software to decide the required duration. Software reset GPIO module. 0_B **Disabled** GPIO software reset is disabled. 1_B **Enabled** GPIO software reset is enabled.
RD9	9	rw	**Reset Request for Reset Domain RD9** Configures the reset domain 9. Software to decide the required duration. Software reset MGE module. 0_B **Disabled** MGE software reset is disabled. 1_B **Enabled** MGE software reset is enabled.
RD7	7	rw	**Reset Request for Reset Domain RD7** Configures the reset domain 0. Software to decide the required duration. Software reset CDB. 0_B **Disabled** CDB software reset is disabled. 1_B **Enabled** CDB software reset is enabled.
RD6	6	rw	**Reset Request for Reset Domain RD6** Configures the reset domain 6. Software to decide the required duration. Software reset GPHY Shell. 0_B **Disabled** GPHY Shell software reset is disabled. 1_B **Enabled** GPHY Shell software reset is enabled.
RD3	4	rw	**Reset Request for Reset Domain RD4** Configures the reset domain 4. Software to decide the required duration. Software reset GPHY4 Macro. 0_B **Disabled** GPHY4 Macro software reset is disabled. 1_B **Enabled** GPHY4 Macro software reset is enabled.
RD3	3	rw	**Reset Request for Reset Domain RD3** Configures the reset domain 3. Software to decide the required duration. Software reset GPHY3 Macro. 0_B **Disabled** GPHY3 Macro software reset is disabled. 1_B **Enabled** GPHY3 Macro software reset is enabled.

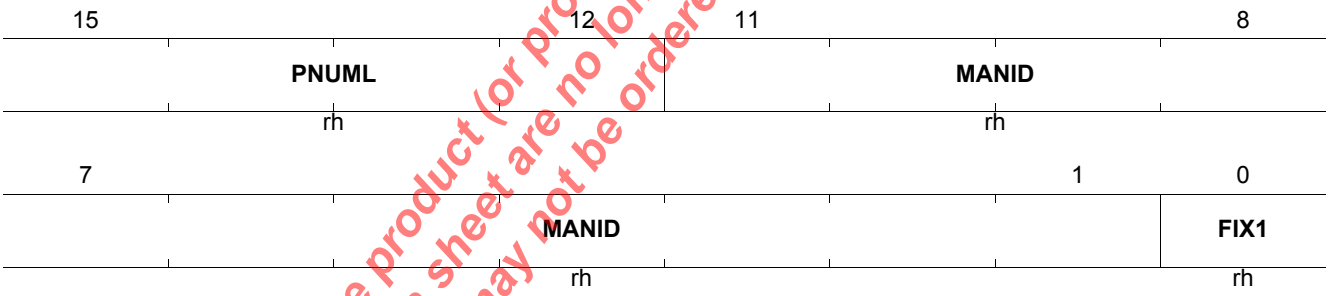
Field	Bits	Type	Description
RD2	2	rw	**Reset Request for Reset Domain RD2** Configures the reset domain 2. Software to decide the required duration. Software reset GPHY2 Macro. 0_B **Disabled** GPHY2 Macro software reset is disabled. 1_B **Enabled** GPHY2 Macro software reset is enabled.
RD1	1	rw	**Reset Request for Reset Domain RD1** Configures the reset domain 1. Software to decide the required duration. Software reset GPHY1 Macro. 0_B **Disabled** GPHY1 Macro software reset is disabled. 1_B **Enabled** GPHY1 Macro software reset is enabled.
RD0	0	rw	**Reset Request for Reset Domain RD0** Configures the reset domain 0. Software to decide the required duration. Software reset GPHY0 Macro. 0_B **Disabled** GPHY0 Macro software reset is disabled. 1_B **Enabled** GPHY0 Macro software reset is enabled.

MANU ID Register

This shows Manufacturer ID and part number.

MANU_ID **Offset** **Reset Value**

MANU ID Register **$FA10_H$** **0713_H**

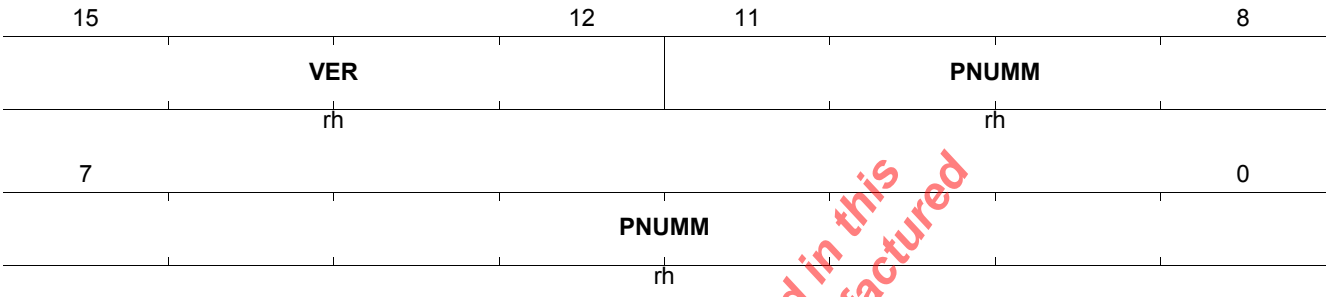


Field	Bits	Type	Description
PNUML	15:12	rh	**Part Number LSB** Part Number LSB
MANID	11:1	rh	**Manufacturer ID** Manufacturer ID, it shall be 389_H
FIX1	0	rh	**Fixed to 1** Fixed to 1.

Part Number Register

This shows part number and chip version.

PNUM_ID	Offset	Reset Value
PNUM ID Register	$FA11_H$	$x003_H$

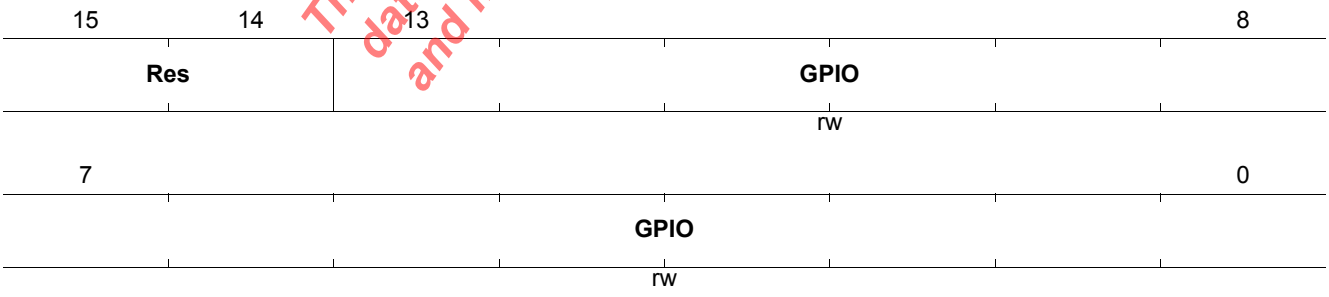


Field	Bits	Type	Description
VER	15:12	rh	**Chip Version** Chip Version ID **Constants** 0001_B **V1.1** Chip version ID register value is '1' for V1.1. 0010_B **V1.2** Chip version ID register value is '2' for V1.2.
PNUMM	11:0	rh	**Part Number MSB** Part Number, Fixed to 003_H

GPIO PAD Driver Strength Control 0 Register

This configures PAD driver strength control.

GPIO_DRIVE0_CFG	Offset	Reset Value
GPIO PAD Driver Strength 0 Control Register	$FA70_H$	$3FFF_H$

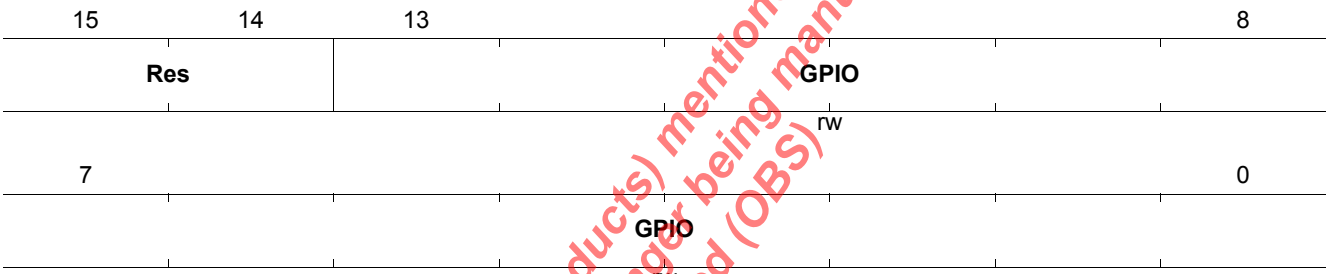


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO PAD Drive Strength Bit 0** PAD driver strength. 00_B **2 mA** PAD drive strength is 2 mA. 01_B **4 mA** PAD drive strength is 4 mA. 10_B **8 mA** PAD drive strength is 8 mA. 11_B **12 mA** PAD drive strength is 12 mA.

GPIO PAD Driver Strength Control 1 Register

This configures PAD driver strength control.

GPIO_DRIVE1_CFG	Offset	Reset Value
GPIO PAD Driver Strength 1 Control Register	$FA71_H$	0000_H

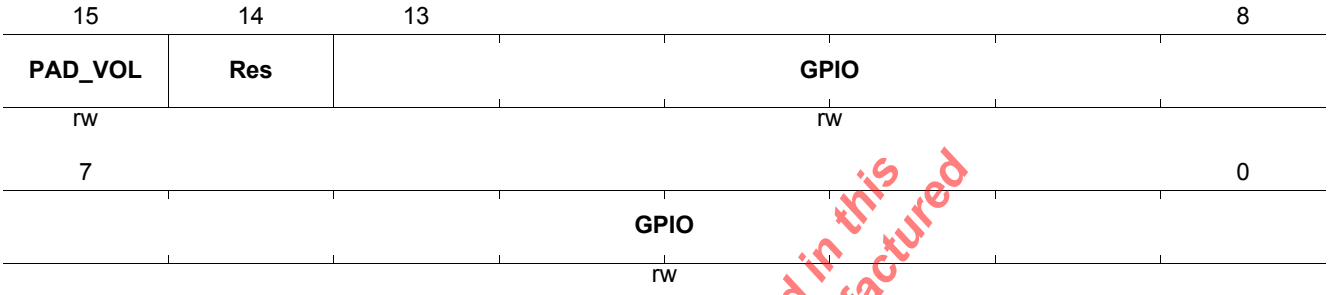


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO PAD Drive Strength Bit 1** PAD driver strength. 00_B **2 mA** PAD drive strength is 2 mA. 01_B **4 mA** PAD drive strength is 4 mA. 10_B **8 mA** PAD drive strength is 8 mA. 11_B **12 mA** PAD drive strength is 12 mA.

GPIO PAD Slew Control Register

This configures GPIO PAD Slew control.

GPIO_SLEW_CFG	Offset	Reset Value
GPIO PAD Slew Control Register	$FA72_H$	0000_H

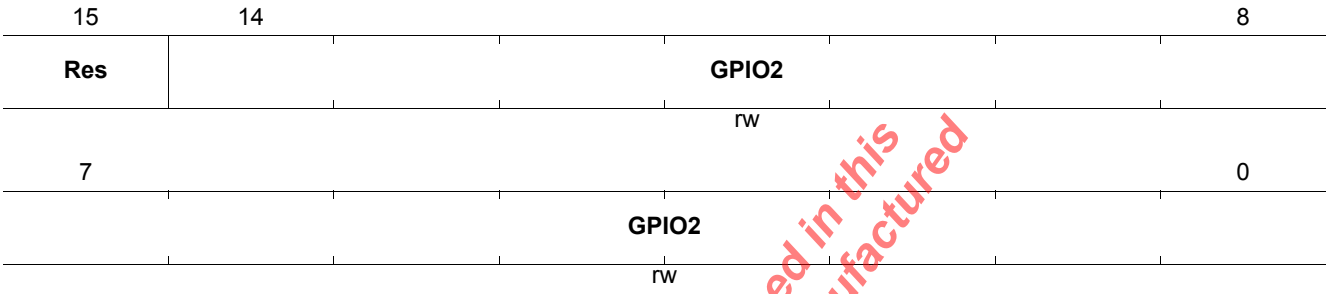


Field	Bits	Type	Description
PAD_VOL	15	rw	**GPIO1 PAD Voltage Supply Level** PAD Slew rate. 0_B **HIGH** GPIO group 1and Reset PAD Voltage supply level is 3.3 V or 2.5 V. 1_B **LOW** GPIO group 1 and Reset PAD Voltage supply level is 1.8 V.
GPIO	13:0	rw	**GPIO PAD Slew Control** PAD slew control. 0_B **Slow** Slow slew. 1_B **Fast** Fast slew.

GPIO2 PAD Driver Strength Control 0 Register

This configures PAD driver strength control.

GPIO2_DRIVE0_CFG	Offset	Reset Value
GPIO2 PAD Driver Strength 0 Control Register	$FA74_H$	$7FFF_H$

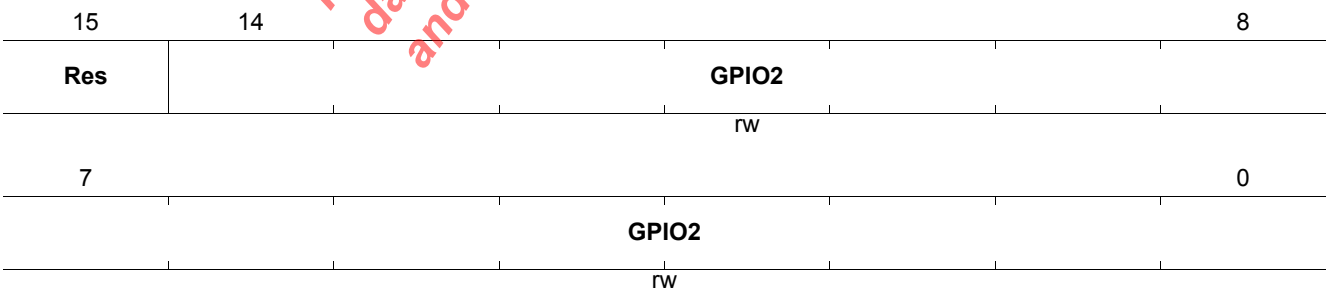


Field	Bits	Type	Description
GPIO2	14:0	rw	**GPIO2 PAD Drive Strength Bit 0** PAD driver strength. 00_B **2 mA** PAD drive strength is 2 mA. 01_B **4 mA** PAD drive strength is 4 mA. 10_B **8 mA** PAD drive strength is 8 mA. 11_B **12 mA** PAD drive strength is 12 mA.

GPIO2 PAD Driver Strength Control 1 Register

This configures PAD driver strength control.

GPIO2_DRIVE1_CFG	Offset	Reset Value
GPIO2 PAD Driver Strength 1 Control Register	$FA75_H$	0000_H



Field	Bits	Type	Description
GPIO2	14:0	rw	**GPIO2 PAD Drive Strength Bit 1** PAD driver strength. 00_B **2 mA** PAD drive strength is 2 mA. 01_B **4 mA** PAD drive strength is 4 mA. 10_B **8 mA** PAD drive strength is 8 mA. 11_B **12 mA** PAD drive strength is 12 mA.

GPIO2 PAD Slew Control Register

This configures GPIO2 PAD Slew control.

GPIO2_SLEW_CFG	Offset	Reset Value
GPIO2 Slew Control Register	$FA76_H$	0000_H

15	14	8
PAD_VOL	GPIO2	
rw	rw	

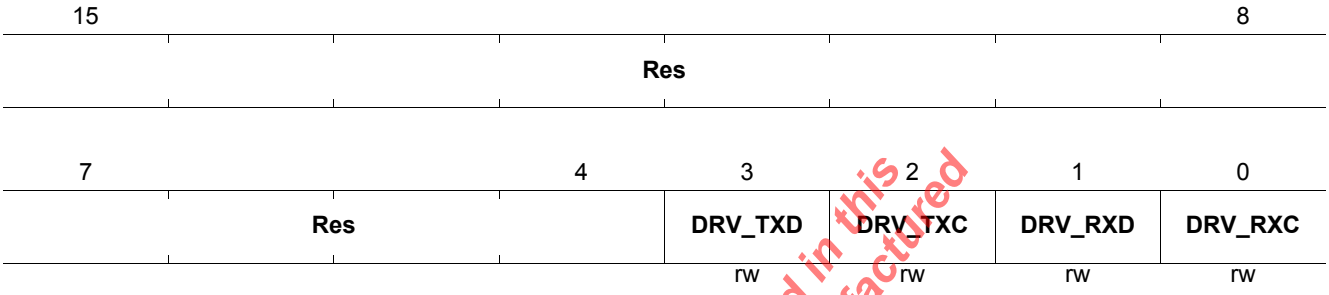
7	0
GPIO2	
rw	

Field	Bits	Type	Description
PAD_VOL	15	rw	**GPIO2 PAD Voltage Supply Level** PAD Slew rate. 0_B **HIGH** GPIO group 2 PAD Voltage supply level is 3.3 V or 2.5 V. 1_B **LOW** GPIO group 2 PAD Voltage supply level is 1.8 V.
GPIO2	14:0	rw	**GPIO PAD Slew Control** PAD slew control. 0_B **Slow** Slow Slew. 1_B **Fast** Fast Slew.

RGMII PAD Slew Control Register

This configures PAD driver strength control.

RGMII_SLEW_CFG	Offset	Reset Value
RGMII PAD Slew Control Register	$FA78_H$	0000_H

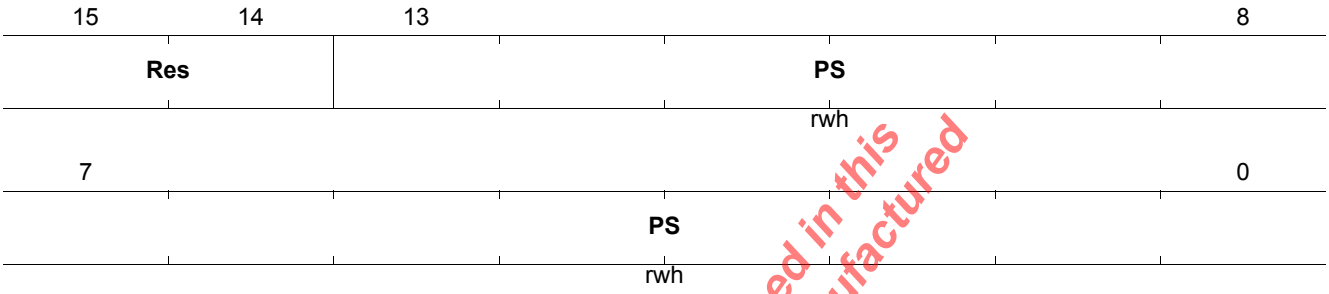


Field	Bits	Type	Description
DRV_TXD	3	rw	**RGMII TX Non-Clock PAD Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_TXC	2	rw	**RGMII TX Clock Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_RXD	1	rw	**RGMII RX Non-Clock PAD Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_RXC	0	rw	**RGMII RX Clock Slew Rate** PAD driver strength. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.

Pin Strapping Register 0

The configuration input pin(s) are sampled and latched at the rising edge of Hardware Reset input. This register can not be reset by global software reset and module software reset.

PS0	Offset	Reset Value
Pin Strapping Register	$FA80_H$	$XXXX_H$

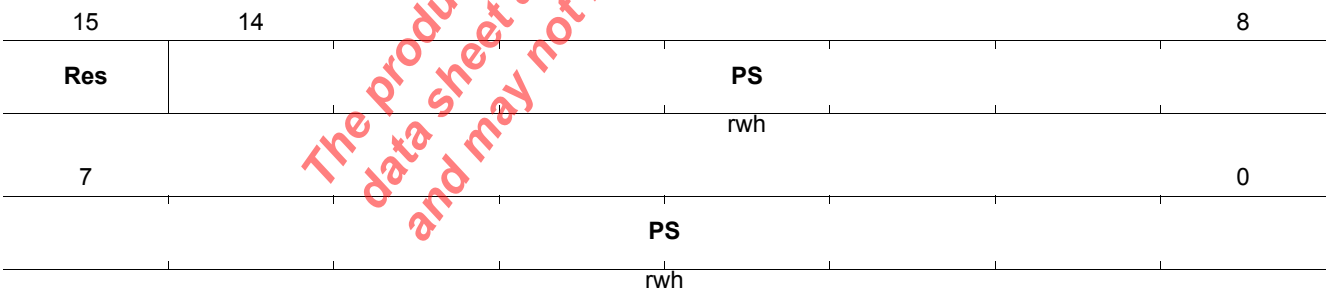


Field	Bits	Type	Description
PS	13:0	rwh	**Pin Strapping of GPIO0 to GPIO13**

Pin Strapping Register 1

The configuration input pin(s) are sampled and latched at the rising edge of Hardware Reset input. This register can not be reset by global software reset and module software reset.

PS1	Offset	Reset Value
Pin Strapping Register 1	$FA81_H$	$XXXX_H$



Field	Bits	Type	Description
PS	14:0	rwh	**Pin Strapping of GPIO16 to GPIO30**

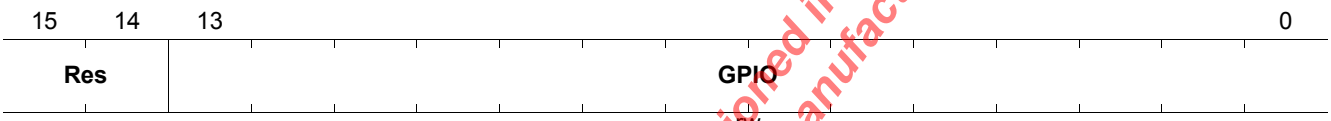
4.1.10 GPIO Registers

The individual control and data bits of each digital parallel port are implemented in a number of registers. Bits with the same meaning and function are assembled together in the same register. Each parallel port consists of a set of registers. The registers are used to configure and use the port as general purpose I/O or alternate function input/output.

GPIO Data Output Register

If a pin is used as general purpose output (GPIO), output data is written into register GPIO_OUT.

GPIO_OUT	Offset	Reset Value
GPIO Data Output Register	$F380_H$	0000_H

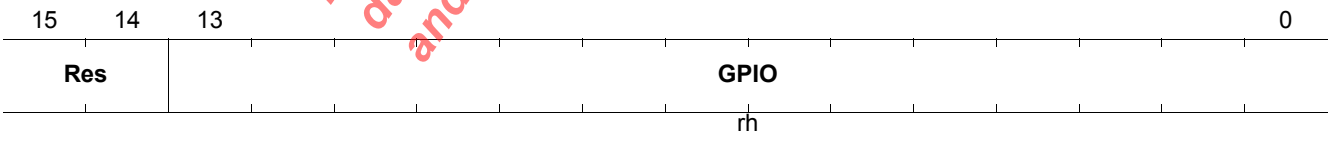


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Output Value** 0_B **LOW** Output value = 0 *Note: Default value after reset* 1_B **HIGH** Output value = 1

GPIO Data Input Register

The value at a pin can be read through the read-only register GPIO_IN. The data input register GPIO_IN always contains a latched value of the assigned pin.

GPIO_IN	Offset	Reset Value
GPIO Data Input Register	$F381_H$	0000_H



Field	Bits	Type	Description
GPIO	13:0	rh	**GPIO Input Value** 0_B **LOW** Input value = 0 1_B **HIGH** Output value = 1

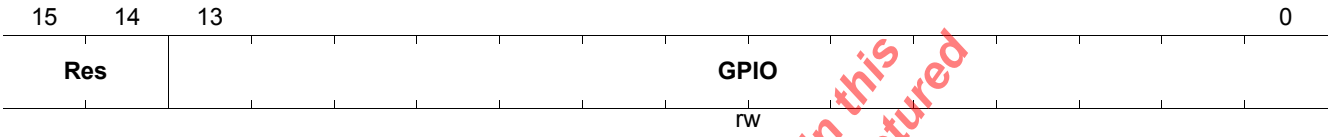
GPIO Direction Register

The direction of port pins can be controlled in the following ways:

- Controlled by Px_DIR register if used for GPIO and controlled by the peripheral if used for alternate function
- Controlled by Px_DIR register if used as GPIO and fixed direction if used for alternate function

If the port direction is controlled by the respective direction register Px_DIR, the following encoding is defined.

GPIO_DIR	Offset	Reset Value
GPIO Direction Register	$F382_H$	0000_H



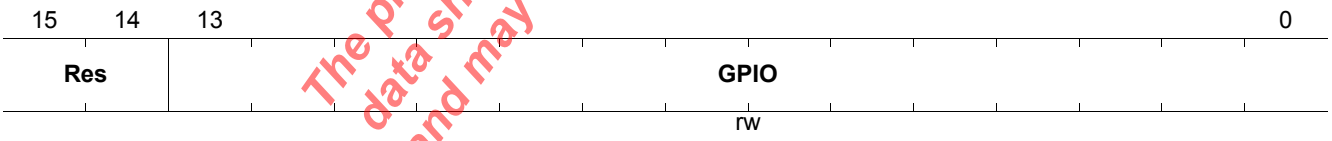
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Direction Control** 0_B **Input** GPIO is in input mode *Note: Default value after reset* 1_B **Output** GPIO is in output mode

GPIO Alternate Function Select Register 0

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO_ALTSEL0** and 1.

GPIO_ALTSEL0	Offset	Reset Value
Port 0 Alternate Function Select Register 0	$F383_H$	0000_H



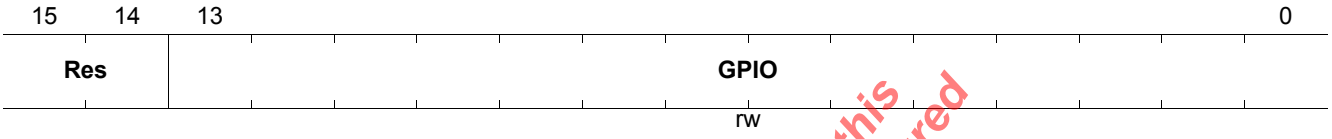
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Alternate Function Selection LSB** GPIO Alternate Function Selection LSB

GPIO Alternate Function Select Register 1

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO_ALTSEL0** and 1.

GPIO_ALTSEL1	Offset	Reset Value
Port 0 Alternate Function Select Register 1	$F384_H$	$003C_H$

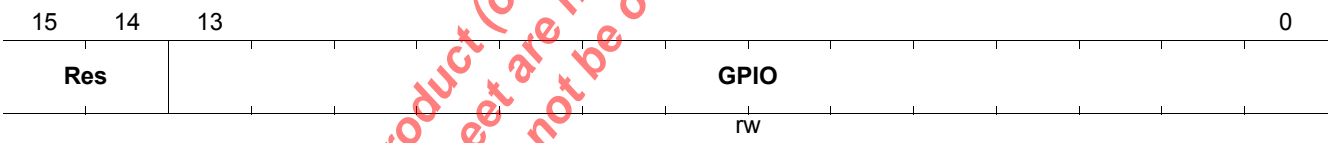


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Alternate Function Selection MSB** GPIO Alternate Function Selection MSB

GPIO Open Drain Control Register

Each pin in output mode can be switched to Open Drain Mode. If driven with 1, no driver will be activated; if driven with 0, the pull-down transistor will be activated.

GPIO_OD	Offset	Reset Value
GPIO Open Drain Control Register	$F385_H$	$3FFF_H$



Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Open Drain Mode** 0_B **OD** Open Drain Mode, output is actively driven only for 0 state. 1_B **PP** Normal Mode, output is actively driven for 0 and 1 state.

Port 0 Pull-Up/Pull-Down Select Register

Internal pull-up/pull-down devices can be optionally applied to pin. This offers the possibility to configure the following input characteristics:

- Tristate
- High-impedance with a weak pull-up device
- High-impedance with a weak pull-down device

And the following output characteristics:

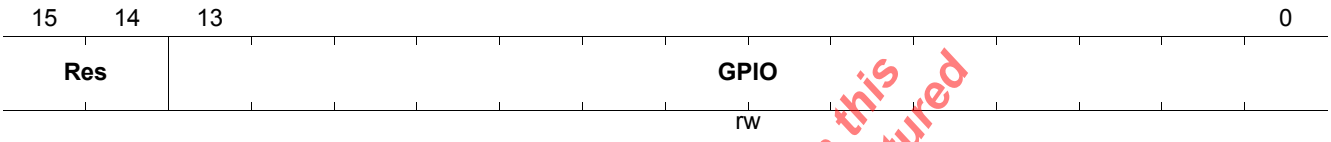
- Push/pull (optional pull-up/pull-down)
- Open drain with internal pull-up
- Open drain with external pull-up

The pull-up/pull-down device can be fixed or controlled via the registers **GPIO_PUDEN**. Register **GPIO_PUDSEL** selects the type of pull-up/pull-down device, while register **GPIO_PUDEN** enables or disables it. The pull-up/pull-down device can be selected pin-wise. Note that the pull-up/pull-down devices are predefined for some pins after reset.

Note: The selected pull-up/pull-down device is enabled by setting the respective bit in the Px_PUDEN register.

GPIO_PUDSEL **Offset** **Reset Value**

GPIO Pull-Up/Pull-Down Select Register **$F386_H$** **$3FFF_H$**



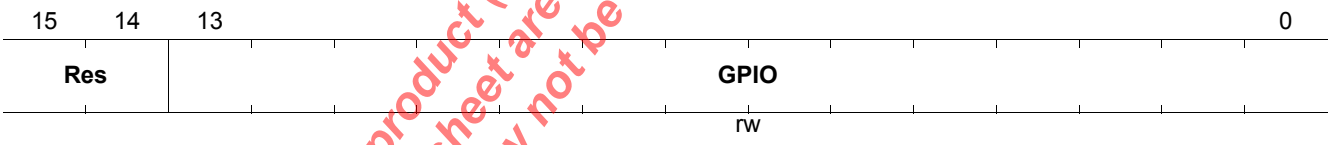
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Pull Up/Down Mode** 0_B **PD** Internal weak pull down is enabled. 1_B **PU** Internal weak pull up is enabled.

GPIO Pull-Up/Pull-Down Enable Register

Description, see above.

GPIO_PUDEN **Offset** **Reset Value**

GPIO Pull-Up/Pull-Down Enable Register **$F387_H$** **$3FFF_H$**

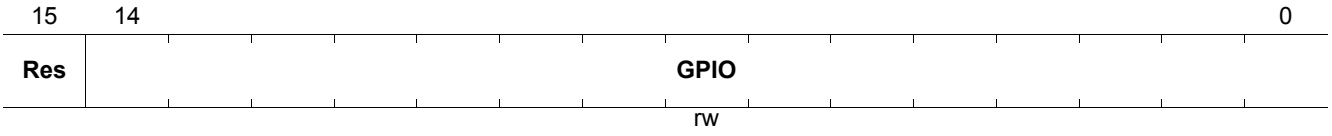


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Pull Up/Down Enable** 0_B **Disable** Internal weak pull up/down is disabled. 1_B **Enable** Internal weak pull up/down is enabled.

GPIO2 Data Output Register

If a pin is used as general purpose output (GPIO), output data is written into register GPIO_OUT.

GPIO2_OUT	Offset	Reset Value
GPIO2 Data Output Register	$F390_H$	0000_H

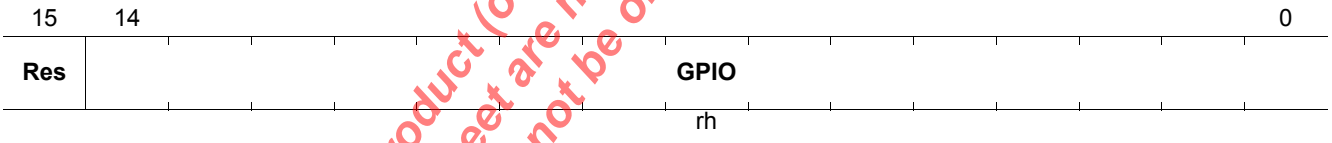


Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Output Value** 0_B **LOW** Output value = 0 *Note: Default value after reset* 1_B **HIGH** Output value = 1

GPIO2 Data Input Register

The value at a pin can be read through the read-only register GPIO_IN. The data input register GPIO_IN always contains a latched value of the assigned pin.

GPIO2_IN	Offset	Reset Value
GPIO2 Data Input Register	$F391_H$	0000_H



Field	Bits	Type	Description
GPIO	14:0	rh	**GPIO Input Value** 0_B **LOW** Input value = 0 1_B **HIGH** Output value = 1

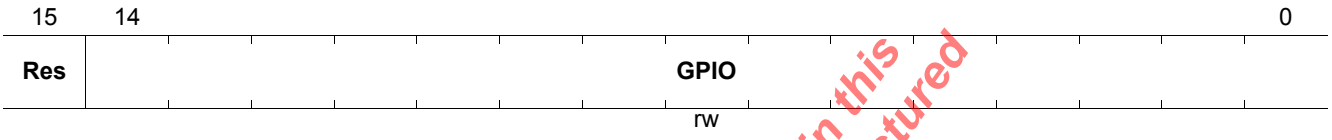
GPIO2 Direction Register

The direction of port pins can be controlled in the following ways:

- Controlled by Px_DIR register if used for GPIO and controlled by the peripheral if used for alternate function
- Controlled by Px_DIR register if used as GPIO and fixed direction if used for alternate function

If the port direction is controlled by the respective direction register Px_DIR, the following encoding is defined.

GPIO2_DIR	Offset	Reset Value
GPIO2 Direction Register	$F392_H$	0000_H



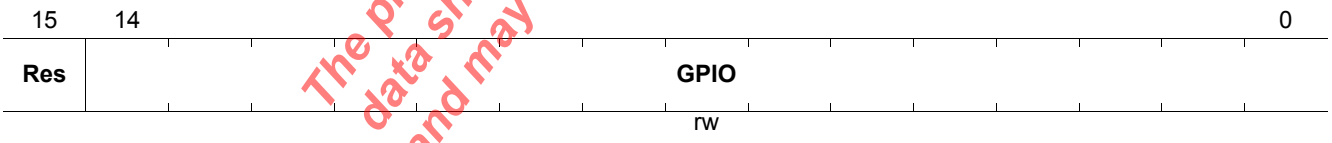
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Direction Control** 0_B **Input** GPIO is in input mode *Note: Default value after reset* 1_B **Output** GPIO is in output mode

GPIO2 Alternate Function Select Register 0

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO2_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO2_ALTSEL0** and 1.

GPIO2_ALTSEL0	Offset	Reset Value
Port 2 Alternate Function Select Register 0	$F393_H$	0000_H



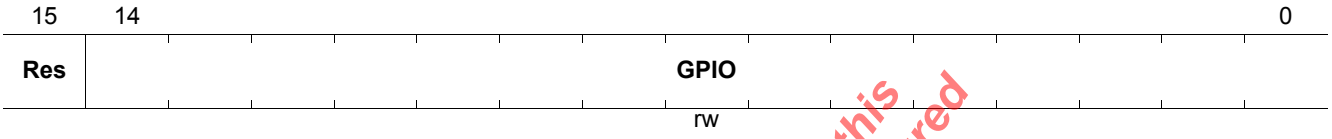
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Alternate Function Selection LSB** GPIO Alternate Function Selection LSB

GPIO2 Alternate Function Select Register 1

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO2_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO2_ALTSEL0** and 1.

GPIO2_ALTSEL1	Offset	Reset Value
Port 2 Alternate Function Select Register 1	**$F394_H$**	**0000_H**

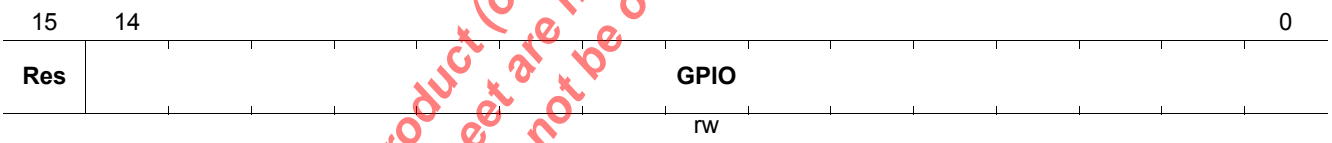


Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Alternate Function Selection MSB** GPIO Alternate Function Selection MSB

GPIO2 Open Drain Control Register

Each pin in output mode can be switched to Open Drain Mode. If driven with 1, no driver will be activated; if driven with 0, the pull-down transistor will be activated.

GPIO2_OD	Offset	Reset Value
GPIO2 Open Drain Control Register	**$F395_H$**	**$7FFF_H$**



Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Open Drain Mode** 0_B **OD** Open Drain Mode, output is actively driven only for 0 state. 1_B **PP** Normal Mode, output is actively driven for 0 and 1 state.

Port 2 Pull-Up/Pull-Down Select Register

Internal pull-up/pull-down devices can be optionally applied to pin. This offers the possibility to configure the following input characteristics:

- Tristate
- High-impedance with a weak pull-up device
- High-impedance with a weak pull-down device

And the following output characteristics:

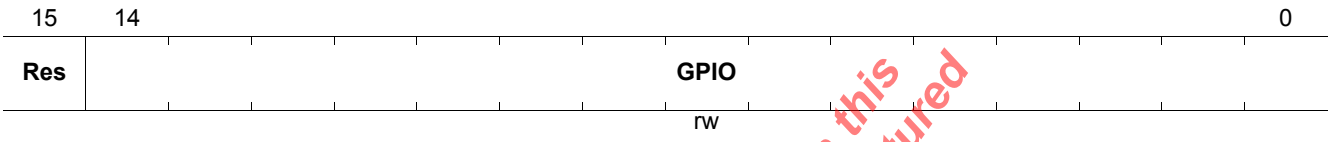
- Push/pull (optional pull-up/pull-down)
- Open drain with internal pull-up
- Open drain with external pull-up

The pull-up/pull-down device can be fixed or controlled via the registers **GPIO2_PUDEN**. Register **GPIO2_PUDSEL** selects the type of pull-up/pull-down device, while register **GPIO2_PUDEN** enables or disables it. The pull-up/pull-down device can be selected pin-wise. Note that the pull-up/pull-down devices are predefined for some pins after reset.

Note: The selected pull-up/pull-down device is enabled by setting the respective bit in the Px_PUDEN register.

GPIO2_PUDSEL **Offset** **Reset Value**

GPIO2 Pull-Up/Pull-Down Select Register **$F396_H$** **$7FFF_H$**



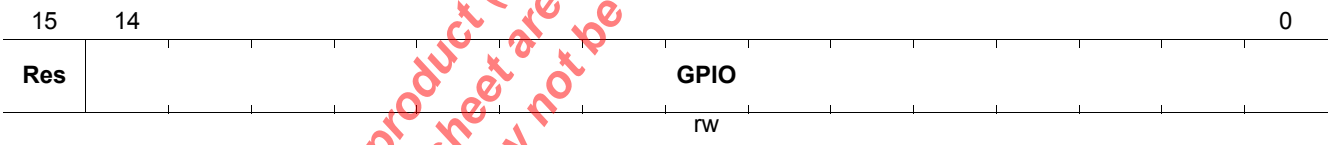
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Pull Up/Down Mode** 0_B **PD** Internal weak pull down is enabled. 1_B **PU** Internal weak pull up is enabled.

GPIO2 Pull-Up/Pull-Down Enable Register

Description, see above.

GPIO2_PUDEN **Offset** **Reset Value**

GPIO2 Pull-Up/Pull-Down Enable Register **$F397_H$** **$7FFF_H$**



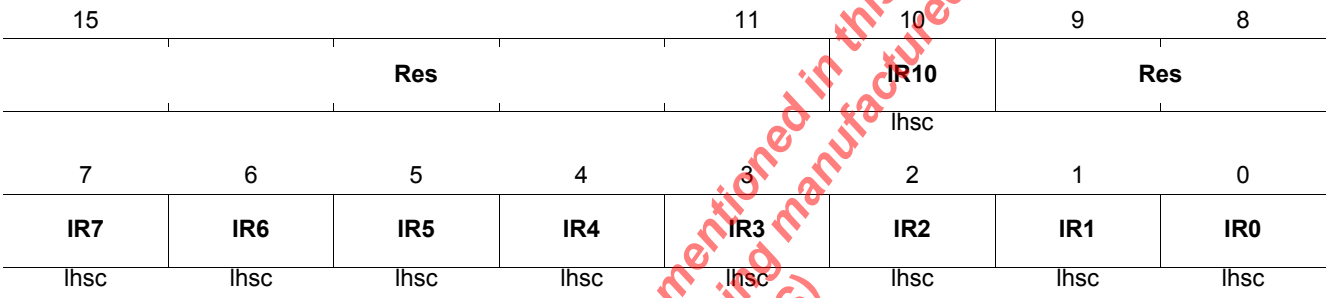
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Pull Up/Down Enable** 0_B **Disable** Internal weak pull up/down is disabled. 1_B **Enable** Internal weak pull up/down is enabled.

4.1.11 ICU Registers

IM0 Interrupt Status Register

Writing a 1 to a bit in the interrupt status register causes this bit to be cleared. Writing 0 to a bit does not change the value of the interrupt request flag. A read action to this register delivers the unmasked captured status of the interrupt request lines.

IM0_ISR	Offset	Reset Value
IM0 Interrupt Status Register	$F3C0_H$	0000_H



Field	Bits	Type	Description
IR10	10	lhsc	**Status of Interrupt Request Packet Extraction** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR7	7	lhsc	**Status of Interrupt Request MGE** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR6	6	lhsc	**Status of Interrupt Request xMII** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR5	5	lhsc	**Status of Interrupt Request GSWIP** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR4	4	lhsc	**Status of Interrupt Request PHY4** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR3	3	lhsc	**Status of Interrupt Request PHY3** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR2	2	lhsc	**Status of Interrupt Request PHY2** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR1	1	lhsc	**Status of Interrupt Request PHY1** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.

Field	Bits	Type	Description
IR0	0	lhsc	**Status of Interrupt Request PHY0** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.

IM0 EINT0 Interrupt Enable Register

Writing 1 to a bit enables the interrupt request line, while writing 0 to a bit disables the associated interrupt request line.

IM0_EINT0_IER — **IM0 EINT0 Interrupt Enable Register**

Offset $F3C2_H$

Reset Value 0000_H

15	14	13	12	11	10	9	8
Res					IR10	Res	
					rw		

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IR10	10	rw	**Interrupt Enable Packet Extraction** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR7	7	rw	**Interrupt Enable MGE** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR6	6	rw	**Interrupt Enable xMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR5	5	rw	**Interrupt Enable GSWIP** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR4	4	rw	**Interrupt Enable PHY4** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR3	3	rw	**Interrupt Enable PHY3** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR2	2	rw	**Interrupt Enable PHY2** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR1	1	rw	**Interrupt Enable PHY1** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

Field	Bits	Type	Description
IR0	0	rw	**Interrupt Enable PHY0** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

IM0 EINT1 Interrupt Enable Register

Writing 1 to a bit enables the interrupt request line, while writing 0 to a bit disables the associated interrupt request line.

IM0_EINT1_IER	Offset	Reset Value
IM0 EINT1 Interrupt Enable Register	$F3C3_H$	0000_H

15				11	10	9	8
Res					IR10	Res	
					rw		

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
rw	rw	rw	rw	rw	rw	rw	rw

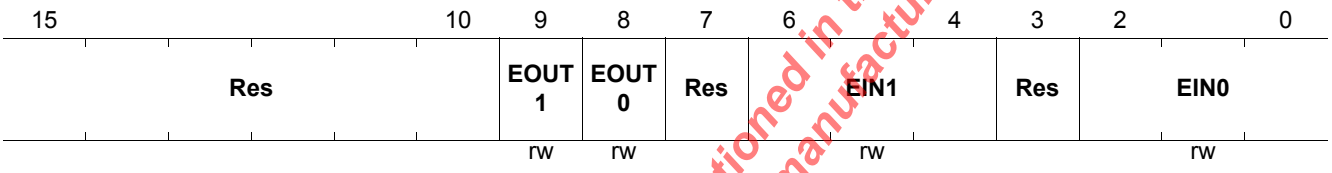
Field	Bits	Type	Description
IR10	10	rw	**Interrupt Enable Packet Extraction** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR7	7	rw	**Interrupt Enable MGE** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR6	6	rw	**Interrupt Enable xMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR5	5	rw	**Interrupt Enable GSWIP** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR4	4	rw	**Interrupt Enable PHY4** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR3	3	rw	**Interrupt Enable PHY3** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR2	2	rw	**Interrupt Enable PHY2** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR1	1	rw	**Interrupt Enable PHY1** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

Field	Bits	Type	Description
IR0	0	rw	**Interrupt Enable PHY0** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

External Interrupt Control Register

The edge and level detection mechanism of all external interrupt inputs are controlled by register. The polarity of external interrupt outputs are also controlled by register

EIU_EXIN_CONF	Offset	Reset Value
EIU External Interrupt Controller Register	$F3C4_H$	0000_H



Field	Bits	Type	Description
EOUT1	9	rw	**External Interrupt Output EINT1** Configures the external interrupt pin 1 output characteristics. 0_B **High Level** Active High 1_B **Low Level** Active Low
EOUT0	8	rw	**External Interrupt Output EINT0** Configures the external interrupt pin 0 output characteristics. 0_B **High Level** Active High 1_B **Low Level** Active Low
EIN1	6:4	rw	**External Interrupt Input EINT1** Configures the external interrupt pin 1 input characteristics. 000_B **Edge/Level** Edge and level detection as well as interrupt request generation is disabled 001_B **Rising Edge** Interrupt on rising (positive) edges 010_B **Falling Edge** Interrupt on falling (negative) edges 011_B **Rising/Falling Edge** Both edges, rising and falling edges 100_B **Edge/Level disable** Edge and level detection as well as interrupt request generation is disabled 101_B **High Level** Level detection of high levels 110_B **Low Level** Level detection of low-levels 111_B **Res** reserved

Field	Bits	Type	Description
EIN0	2:0	rw	**External Interrupt Input EINT0** Configures the external interrupt pin 0 input characteristics. 000_B **Edge/Level** Edge and level detection as well as interrupt request generation is disabled 001_B **Rising Edge** Interrupt on rising (positive) edges 010_B **Falling Edge** Interrupt on falling (negative) edges 011_B **Rising/Falling Edge** Both edges, rising and falling edges 100_B **Edge/Level disable** Edge and level detection as well as interrupt request generation is disabled 101_B **High Level** Level detection of high levels 110_B **Low Level** Level detection of low-levels 111_B **Res** reserved

4.1.12 LED Registers

This chapters describes all registers in LED module.

LED Single Color Mode Register

This register configures the LED ground mode or power mode.

LED_MD_CFG	Offset	Reset Value
LED Single Color LED Mode Register	$F3E0_H$	0000_H

15	14	13	12	11	10	9	8
Res	LED14	LED13	LED12	LED11	LED10	LED9	LED8
	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
rw	rw	rw	rw	rw	rw	rw	rw

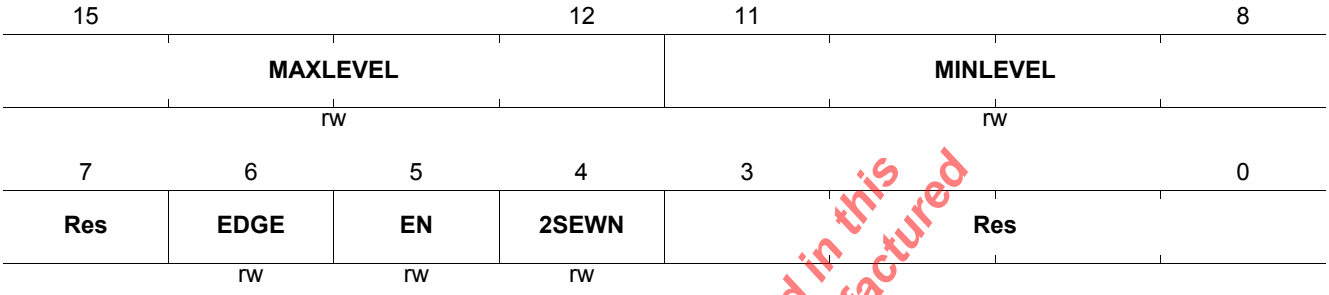
Field	Bits	Type	Description
LED14	14	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED13	13	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED12	12	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED11	11	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED10	10	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED9	9	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED8	8	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED7	7	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode

Field	Bits	Type	Description
LED6	6	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED5	5	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED4	4	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED3	3	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED2	2	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED1	1	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED0	0	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode

LED Brightness Control Register

This register configures the LED brightness control.

LED_BRT_CTRL	Offset	Reset Value
LED Brightness Control Register	$F3E1_H$	$F430_H$

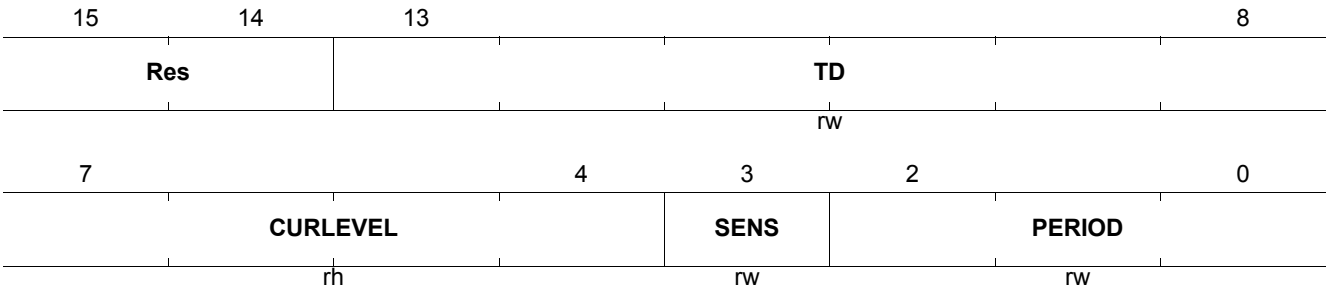


Field	Bits	Type	Description
MAXLEVEL	15:12	rw	**Maximum LED Brightness Value**
MINLEVEL	11:8	rw	**Minimum LED Brightness Value**
EDGE	6	rw	**LED Brightness Switch Edge Detection** 0_B **Falling** Falling Edge 1_B **Rising** Rising Edge
EN	5	rw	**LED Brightness Control Enable** 0_B **Disable** LED brightness control is disabled 1_B **Enable** LED brightness control is enabled
2SEWN	4	rw	**LED Brightness 2 Level Switch Enable** 0_B **Disable** LED brightness control via an external switch is disabled 1_B **Enable** LED brightness control via an external switch is enabled

LED Light Sensing Control Register

This register configures the LED light sensing.

LED_LSENS_CTRL	Offset	Reset Value
LED Light Sensing Control Register	$F3E2_H$	$0D09_H$



Field	Bits	Type	Description
TD	13:8	rw	**The Number of Slots for Discharge**
CURLEVEL	7:4	rh	**Current Brightness Level**
SENS	3	rw	**LED Sensing Enable** 0_B **Disable** LED sensing is disabled 1_B **Enable** LED sensing is enabled
PERIOD	2:0	rw	**LED Sensing Period** 000_B **1000** 1000 ms 001_B **500** 500 ms 010_B **333** 333 ms 011_B **250** 250 ms 100_B **200** 200 ms 101_B **167** 167 ms 110_B **142** 142 ms 111_B **125** 125 ms

4.2 PHY MDIO Registers

This Chapter defines all the registers needed to operate the module "REGISTERS".[1)]

Table 65 Registers Address Space

Module	Base Address	End Address	Note
REGISTERS	00_H	60_H	

Table 66 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
PHY MDIO Registers, STD: Standard Management Registers			
CTRL	Control	00_H	9040_H
STAT	Status Registers	01_H	7949_H
PHYID1	PHY Identifier 1	02_H	$D565_H$
PHYID2	PHY Identifier 2	03_H	$A401_H$
AN_ADV	Auto-Negotiation Advertisement	04_H	$01E1_H$
AN_LPA	Auto-Negotiation Link-Partner Ability	05_H	0000_H
AN_EXP	Auto-Negotiation Expansion	06_H	0004_H
AN_NPTX	Auto-Negotiation Next-Page Transmit Register	07_H	2001_H
AN_NPRX	Auto-Negotiation Link-Partner Received Next-Page Register	08_H	2001_H
GCTRL	Gigabit Control Register	09_H	0300_H
GSTAT	Gigabit Status Register	$0A_H$	0000_H
RES11	Reserved	$0B_H$	0000_H
RES12	Reserved	$0C_H$	0000_H
MMDCTRL	MMD Access Control Register	$0D_H$	0000_H
MMDDATA	MMD Access Data Register	$0E_H$	0000_H
XSTAT	Extended Status Register	$0F_H$	3000_H
PHY MDIO Registers, PHY: PHY-Specific Management Registers			
PHYPERF	Physical Layer Performance Status	10_H	$80FF_H$
PHYSTAT1	Physical Layer Status 1	11_H	0000_H
PHYSTAT2	Physical Layer Status 2	12_H	0000_H
PHYCTL1	Physical Layer Control 1	13_H	0003_H
PHYCTL2	Physical Layer Control 2	14_H	8006_H
ERRCNT	Error Counter	15_H	0000_H
MIISTAT	Media-Independent Interface Status	18_H	0000_H
IMASK	Interrupt Mask Register	19_H	0000_H
ISTAT	Interrupt Status Register	$1A_H$	0000_H
LED	LED Control Register	$1B_H$	$0F00_H$
TPGCTRL	Test-Packet Generator Control	$1C_H$	0000_H

1) Generated by REFIGE v1.4 - Beta Release XIV

Table 66 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
TPGDATA	Test-Packet Generator Data	$1D_H$	$00AA_H$
FWV	Firmware Version Register	$1E_H$	8304_H
RES1F	Reserved	$1F_H$	0000_H

The register is addressed wordwise.

Table 67 Register Access Types

Mode	Symbol	Internal Hardware Configuration		
		Type	Behavior	Arbitration
Status Register, Latch-High	ROLH	RWRE	AUTO_PDI	CLROR
Status Register, Latch-Low	ROLL	WOR	AUTO_HW	CLROR
Status Register, Self-Clearing	ROSC	WOR	AUTO_PDI	CLROR
Read-Write Register	RW	RWR	AUTO_PDI	-
Read-Write Register, Self-Clearing	RWSC	RWR	AUTO_PDI	CLROR
Status Register	RO	WOR	AUTO_PDI	-

4.2.1 STD: Standard Management Registers

This section describes the IEEE 802.3 standard management registers.

Control

This register controls the main functions of the PHY. See IEEE 802.3 22.2.4.1.

CTRL	Offset	Reset Value
Control	00_H	9040_H

15	14	13	12	11	10	9	8
RST	LB	SSL	ANEN	PD	ISOL	ANRS	DPLX
rwsc	rw	rw	rw	rw	rw	rwsc	rw
7	6	5					0
COL	SSM			RES			
rw	rw			ro			

Field	Bits	Type	Description
RST	15	RWSC	**Reset** Resets the PHY to its default state. Active links are terminated. Note that this is a self-clearing bit which is set to zero by the hardware after reset has been done. See IEEE 802.3 22.2.4.1.1. **Constants** 0_B **NORMAL** Normal operational mode 1_B **RESET** Resets the device
LB	14	RW	**Loop-Back** This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the medium via MDI. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test. See IEEE 802.8-2008 22.2.4.1.2. **Constants** 0_B **NORMAL** Normal operational mode 1_B **ENABLE** Closes the loop-back from TX to RX at xMII
SSL	13	RW	**Forced Speed-Selection LSB** Note that this bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This is the LSB (CTRL.SSL) of the forced speed-selection register SS. In conjunction with the MSB (CTRL.SSM), the following encodings are valid: SS=0: 10 Mbit/s SS=1: 100 Mbit/s SS=2: 1000 Mbit/s SS=3: Reserved

Field	Bits	Type	Description
ANEN	12	RW	**Auto-Negotiation Enable** Allows enabling and disabling of the auto-negotiation process capability of the PHY. If enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation. See IEEE 802.3 22.2.4.1.4. **Constants** 0_B **DISABLE** Disable the auto-negotiation protocol 1_B **ENABLE** Enable the auto-negotiation protocol
PD	11	RW	**Power Down** Forces the device into a power-down state where power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power-down functionality, the PHY terminates active data links. None of the xMII interface work in power-down mode. See IEEE 802.3 22.2.4.1.5. **Constants** 0_B **NORMAL** Normal operational mode 1_B **POWERDOWN** Forces the device into power-down mode
ISOL	10	RW	**Isolate** The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance). See IEEE 802.3 22.2.4.1.6. **Constants** 0_B **NORMAL** Normal operational mode 1_B **ISOLATE** Isolates the PHY from the MAC
ANRS	9	RWSC	**Restart Auto-Negotiation** Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (CTRL.ANEN). Note that this bit is self-clearing after the auto-negotiation process is initiated. See IEEE 802.3 22.2.4.1.7. **Constants** 0_B **NORMAL** Stay in current mode 1_B **RESTART** Restart auto-negotiation
DPLX	8	RW	**Forced Duplex Mode** Note that this bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This bit controls the forced duplex mode. It allows forcing of the PHY into full or half-duplex mode. Note that this bit does not take effect in loop-back mode, that is, when bit CTRL.LB is set to one. See IEEE 802.3 22.2.4.1.8. **Constants** 0_B **HD** Half duplex 1_B **FD** Full duplex

Field	Bits	Type	Description
COL	7	RW	**Collision Test** Allows$WORKAREA/units/mdio/source testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency time. See IEEE 802.3 22.2.4.1.9. **Constants** 0_B **DISABLE** Normal operational mode 1_B **ENABLE** Activates the collision test
SSM	6	RW	**Forced Speed-Selection MSB** See the description of SSL. See also IEEE 802.3-2008 22.2.4.1.3.
RES	5:0	RO	**Reserved** Write as zero, ignore on read.

Status Registers

This register contains status and capability information about the device. Note that all bits are read-only. A write access by the MAC does not have any effect. See IEEE 802.3 22.2.4.2.

STAT **Offset** **Reset Value**

Status Registers **01_H** **7949_H**

15	14	13	12	11	10	9	8
CBT4	**CBTXF**	**CBTXH**	**XBTF**	**XBTH**	**CBT2F**	**CBT2H**	**EXT**
ro	ro	ro	ro	ro	ro	ro	ro
7	6	5	4	3	2	1	0
RES	**MFPS**	**ANOK**	**RF**	**ANAB**	**LS**	**JD**	**XCAP**
ro	ro	ro	rolh	ro	roll	rolh	ro

Field	Bits	Type	Description
CBT4	15	RO	**IEEE 100BASE-T4** Specifies the 100BASE-T4 ability. See IEEE 802.3 22.2.4.2.1. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXF	14	RO	**IEEE 100BASE-TX Full-Duplex** Specifies the 100BASE-TX full-duplex ability. See IEEE 802.3 22.2.4.2.2. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode

Field	Bits	Type	Description
CBTXH	13	RO	**IEEE 100BASE-TX Half-Duplex** Specifies the 100BASE-TX half-duplex ability. See IEEE 802.3 22.2.4.2.3. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTF	12	RO	**IEEE 10BASE-T Full-Duplex** Specifies the 10 BASE-T full-duplex ability. See IEEE 802.3 22.2.4.2.4. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTH	11	RO	**IEEE 10BASE-T Half-Duplex** Specifies the 10BASE-T half-duplex ability. See IEEE 802.3 22.2.4.2.5. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2F	10	RO	**IEEE 100BASE-T2 Full-Duplex** Specifies the 100BASE-T2 full-duplex ability. See IEEE 802.3 22.2.4.2.6. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2H	9	RO	**IEEE 100BASE-T2 Half-Duplex** Specifies the 100BASE-T2 half-duplex ability. See IEEE 802.3 22.2.4.2.7. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
EXT	8	RO	**Extended Status** The extended status registers are used to specify 1000 Mbit/s speed capabilities in the register XSTAT. See IEEE 802.3 22.2.4.2.16. **Constants** 0_B **DISABLED** No extended status information available in register 15 1_B **ENABLED** Extended status information available in register 15
RES	7	RO	**Reserved** Ignore when read.
MFPS	6	RO	**Management Preamble Suppression** Specifies the MF preamble suppression ability. See IEEE 802.3 22.2.4.2.9. **Constants** 0_B **DISABLED** PHY requires management frames with preamble 1_B **ENABLED** PHY accepts management frames without preamble
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or in progress. See IEEE 802.3 22.2.4.2.10. **Constants** 0_B **RUNNING** Auto-negotiation process is in progress 1_B **COMPLETED** Auto-negotiation process is completed

Field	Bits	Type	Description
RF	4	ROLH	**Remote Fault** Indicates the detection of a remote fault event. See IEEE 802.3 22.2.4.2.11. **Constants** 0_B **INACTIVE** No remote fault condition detected 1_B **ACTIVE** Remote fault condition detected
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. See IEEE 802.3 22.2.4.2.12. **Constants** 0_B **DISABLED** PHY is not able to perform auto-negotiation 1_B **ENABLED** PHY is able to perform auto-negotiation
LS	2	ROLL	**Link Status** Indicates the link status of the PHY to the link partner. See IEEE 802.3 22.2.4.2.13. **Constants** 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
JD	1	ROLH	**Jabber Detect** Indicates that a jabber event has been detected. See IEEE 802.3 22.2.4.2.14. **Constants** 0_B **NONE** No jabber condition detected 1_B **DETECTED** Jabber condition detected
XCAP	0	RO	**Extended Capability** Indicates the availability and support of extended capability registers. See IEEE 802.3 22.2.4.2.15. **Constants** 0_B **DISABLED** Only base registers are supported 1_B **ENABLED** Extended capability registers are supported

PHY Identifier 1

This is the first of two PHY identification registers containing the MSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.

PHYID1	Offset	Reset Value
PHY Identifier 1	02_H	$D565_H$

15	8
OUI	
ro	

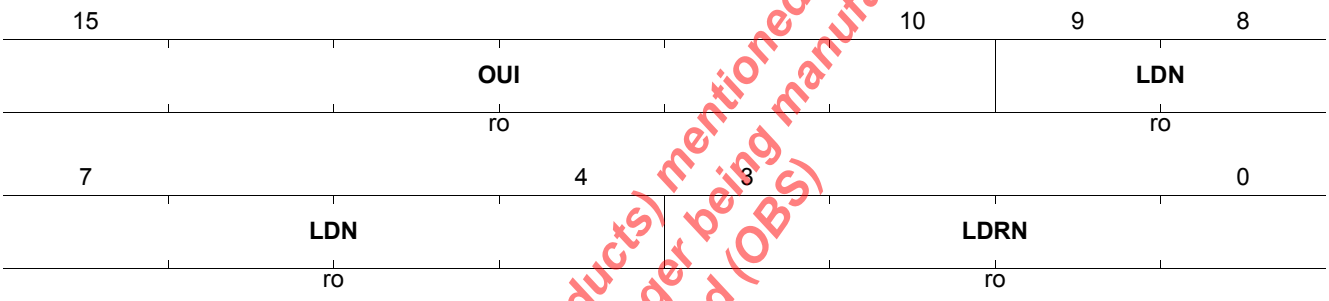
7	0
OUI	
ro	

Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18** This register holds the bits 3:18 of the OUI code for Lantiq Deutschland GmbH (an Intel Company) , which is specified to be OUI=AC-9A-96. See IEEE 802.3 22.2.4.3.1.

PHY Identifier 2

This is the second of 2 PHY identification registers containing the LSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number. See IEEE 802.3 22.2.4.3.1.

PHYID2	Offset	Reset Value
PHY Identifier 2	03_H	$A401_H$

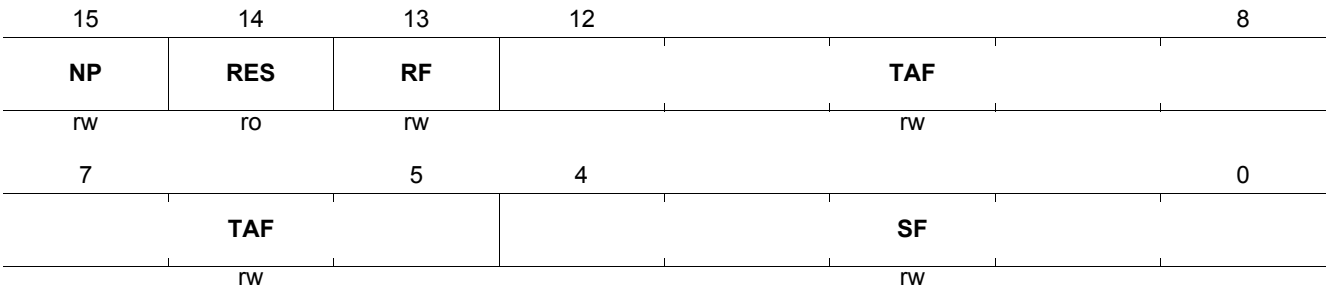


Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24** This register holds the bits 19:24 of the OUI code for Lantiq Deutschland GmbH (an Intel Company), which is specified to be OUI=AC-9A-96.
LDN	9:4	RO	**Lantiq Device Number** Specifies the device number, in order to distinguish between several Lantiq products.
LDRN	3:0	RO	**Lantiq Device Revision Number** Specifies the device revision number, in order to distinguish between several versions of this device.

Auto-Negotiation Advertisement

This register contains the advertised abilities of the PHY during auto-negotiation. See also IEEE 802.3 28.2.4.1.3, as well as IEEE 802.3 Table 28-2.

AN_ADV	Offset	Reset Value
Auto-Negotiation Advertisement	04_H	$01E1_H$



Field	Bits	Type	Description
NP	15	RW	**Next Page** Next-page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP if a 1000BASE-T mode is advertised during auto-negotiation. See IEEE 802.3 28.2.1.2.6. **Constants** 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. See IEEE 802.3 28.2.1.2.4. **Constants** 0_B **NONE** No remote fault is indicated 1_B **FAULT** A remote fault is indicated
TAF	12:5	RW	**Technology Ability Field** The technology ability field is an eight-bit wide field containing information indicating supported technologies as defined by the following constants specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. In converter mode, the field is always forced to value 0x60. The TAF encoding for the IEEE 802.3 selector (AN_ADV.SF=0x1) is described in IEEE 802.3 Annex 28B.2 and in Annex 28D. See also IEEE 802.3 28.2.1.2.2. **Constants** 00000001_B**XBT_HDX** Advertise 10BASE-T half duplex 00000010_B**XBT_FDX** Advertise 10BASE-T full duplex 00000100_B**DBT_HDX** Advertise 100BASE-TX half duplex 00001000_B**DBT_FDX** Advertise 100BASE-TX full duplex 00010000_B**DBT4** Advertise 100BASE-T4 00100000_B**PS_SYM** Advertise symmetric pause 01000000_B**PS_ASYM** Advertise asymmetric pause 10000000_B**RES** Reserved for future technologies

Field	Bits	Type	Description
SF	4:0	RW	**Selector Field** The selector field is a five-bit wide field for encoding 32 possible messages. Selector field encoding definitions are shown in IEEE 802.3 Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. See also IEEE 802.3 28.2.1.2.1. **Constants** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Link-Partner Ability

All of the bits in the auto-negotiation link-partner ability register are read-only. A write to the auto-negotiation link-partner ability register has no effect. This register contains the advertised ability of the link partner (see IEEE 802.3 Tables 28-3 and 28-4). The bit definitions are a direct representation of the received link-code word (see IEEE 802.3 Figure 28-7). See IEEE 802.3 22.2.4.3.3.

AN_LPA — **Offset** — **Reset Value**

Auto-Negotiation Link-Partner Ability — **05_H** — **0000_H**

15	14	13	12	11	10	9	8
NP	**ACK**	**RF**	**TAF**				
ro	ro	ro	ro				

7	6	5	4	3	2	1	0
TAF			**SF**				
ro			ro				

Field	Bits	Type	Description
NP	15	RO	**Next Page** Next-page request indication from the link partner. See IEEE 802.3 28.2.1.2.6. **Constants** 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next pages will follow
ACK	14	RO	**Acknowledge** Acknowledgement indication from the link partner's link-code word. See IEEE 802.3 28.2.1.2.5. **Constants** 0_B **INACTIVE** The device did not successfully receive its link partner's link code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word

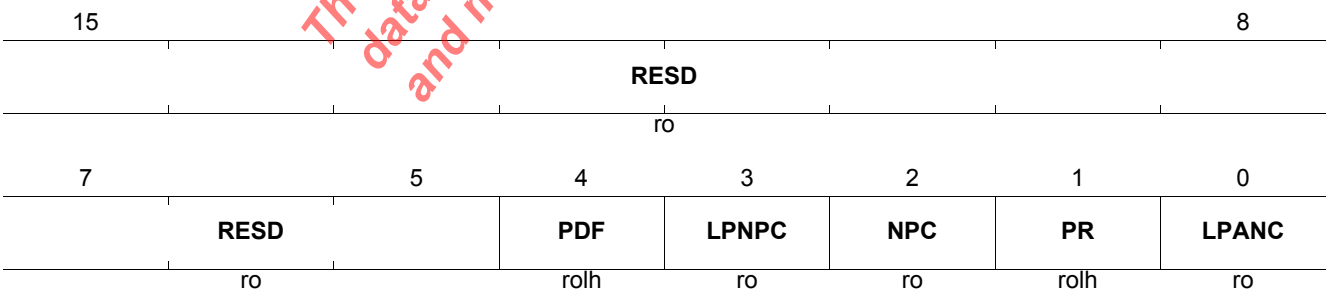
Field	Bits	Type	Description
RF	13	RO	**Remote Fault** Remote fault indication from the link partner. See IEEE 802.3 28.2.1.2.4. **Constants** 0_B **NONE** Remote fault is not indicated by the link partner 1_B **FAULT** Remote fault is indicated by the link partner
TAF	12:5	RO	**Technology Ability Field** Indicates the link-partner capabilities as received from the link partner's link-code word. See IEEE 802.3 28.2.1.2.2. **Constants** 00000001_B**XBT_HDX** Link partner advertised 10BASE-T half duplex 00000010_B**XBT_FDX** Link partner advertised 10BASE-T full duplex. 00000100_B**DBT_HDX** Link partner advertised 100BASE-TX half duplex 00001000_B**DBT_FDX** Link partner advertised 100BASE-TX full duplex 00010000_B**DBT4** Link partner advertised 100BASE-T4 00100000_B**PS_SYM** Link partner advertised symmetric pause 01000000_B**PS_ASYM** Link partner advertised asymmetric pause 10000000_B**RES** Reserved for future technologies; should be zero
SF	4:0	RO	**Selector Field** The selector field represents one of the 32 possible messages. Note that it must fit to the advertised selector field in AN_ADV.SF. Selector field encoding definitions are shown in IEEE 802.3 Annex 28A. **Constants** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Expansion

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. See IEEE 802.3 28.2.4.1.5.

AN_EXP — **Offset** — **Reset Value**

Auto-Negotiation Expansion — **06_H** — **0004_H**



Field	Bits	Type	Description
RESD	15:5	RO	**Reserved** Write as zero, ignore on read.

Field	Bits	Type	Description
PDF	4	ROLH	**Parallel Detection Fault** Note that this bit latches high. It is set to zero upon read of AN_EXP. See IEEE 802.3 28.2.4.1.5. **Constants** 0_B **NONE** A fault has not been detected via the parallel detection function 1_B **FAULT** A fault has been detected via the parallel detection function
LPNPC	3	RO	**Link Partner Next-Page Capable** See IEEE 802.3 28.2.4.1.5. **Constants** 0_B **UNABLE** Link partner is unable to exchange next pages 1_B **CAPABLE** Link partner is capable of exchanging next pages
NPC	2	RO	**Next-Page Capable** See IEEE 802.3 28.2.4.1.5. **Constants** 0_B **UNABLE** Local Device is unable to exchange next pages 1_B **CAPABLE** Local device is capable of exchanging next pages
PR	1	ROLH	**Page Received** Note that this bit latches high. It is set to zero upon read of AN_EXP. See IEEE 802.3 28.2.4.1.5. **Constants** 0_B **NONE** A new page has not been received 1_B **RECEIVED** A new page has been received
LPANC	0	RO	**Link Partner Auto-Negotiation Capable** See IEEE 802.3 28.2.4.1.5. **Constants** 0_B **UNABLE** Link partner is unable to auto-negotiate 1_B **CAPABLE** Link partner is auto-negotiation capable

Auto-Negotiation Next-Page Transmit Register

The auto-negotiation next-page transmit register contains the next-page link-code word to be transmitted when next-page ability is supported. On power-up, this register contains the default value of 0x2001, which represents a message page with the message code set to the null message. See also IEEE 802.3 28.2.4.1.6.

AN_NPTX	Offset	Reset Value
Auto-Negotiation Next-Page Transmit Register	07_H	2001_H

15	14	13	12	11	10	9	8
NP	RES	MP	ACK2	TOGG	MCF		
rw	ro	rw	rw	ro	rw		

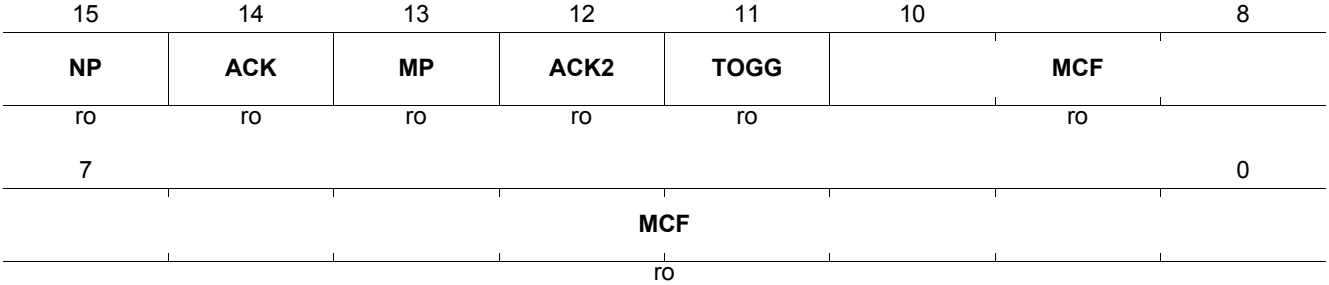
7	6	5	4	3	2	1	0
MCF							
rw							

Field	Bits	Type	Description
NP	15	RW	**Next Page** See IEEE 802.3 28.2.3.4. **Constants** 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zeros, ignore on read.
MP	13	RW	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. See IEEE 802.3 28.2.3.4. **Constants** 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RW	**Acknowledge 2** See IEEE 802.3 28.2.3.4. **Constants** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** See IEEE 802.3 28.2.3.4. **Constants** 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RW	**Message or Unformatted Code Field** See IEEE 802.3 28.2.3.4.

Auto-Negotiation Link-Partner Received Next-Page Register

The auto-negotiation link-partner received next-page register contains the next-page link-code word received from the link partner. See IEEE 802.3 28.2.4.1.7.

AN_NPRX	Offset	Reset Value
Auto-Negotiation Link-Partner Received Next-Page Register	**08_H**	**2001_H**

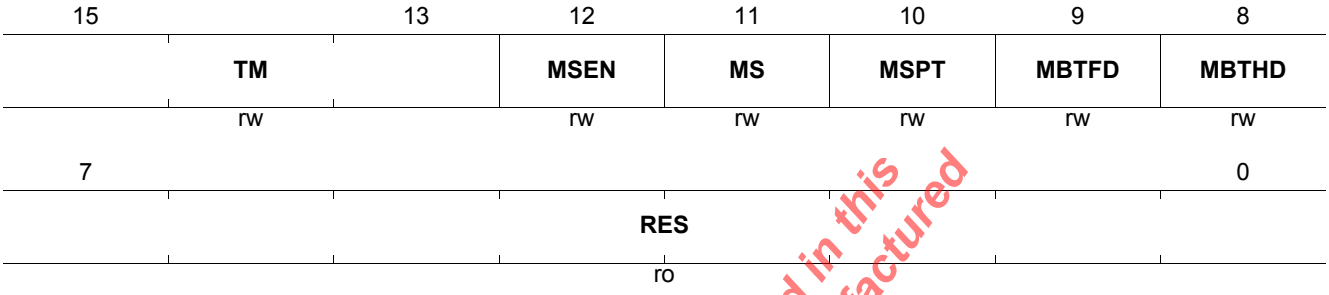


Field	Bits	Type	Description
NP	15	RO	**Next Page** See IEEE 802.3 28.2.3.4. **Constants** 0_B **INACTIVE** No next pages to follow 1_B **ACTIVE** Additional next page(s) will follow
ACK	14	RO	**Acknowledge** See IEEE 802.3 28.2.3.4. **Constants** 0_B **INACTIVE** The device did not successfully receive its link partner's link-code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word
MP	13	RO	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. See IEEE 802.3 28.2.3.4. **Constants** 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RO	**Acknowledge 2** See IEEE 802.3 28.2.3.4. **Constants** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** See IEEE 802.3 28.2.3.4. **Constants** 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RO	**Message or Unformatted Code Field** See IEEE 802.3 28.2.3.4.

Gigabit Control Register

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. See IEEE 802.3 40.5.1.1.

GCTRL	Offset	Reset Value
Gigabit Control Register	09_H	0300_H



Field	Bits	Type	Description
TM	15:13	RW	**Transmitter Test Mode** This register field allows enabling of the standard transmitter test modes. See also IEEE 802.3-2008 Table 40-7. **Constants** 000_B **NOR** Normal operation 001_B **WAV** Test mode 1 transmit waveform test 010_B **JITM** Test mode 2 transmit jitter test in MASTER mode 011_B **JITS** Test mode 3 transmit jitter test in SLAVE mode 100_B **DIST** Test mode 4 transmitter distortion test 101_B **RESD0** Reserved, operations not identified. 110_B **CDIAG** Cable diagnostics. 111_B **ABIST** Analog build in self-test
MSEN	12	RW	**Master/Slave Manual Configuration Enable** See also IEEE 802.3-2008 40.5.1.1. **Constants** 0_B **DISABLED** Disable master/slave manual configuration value 1_B **ENABLED** Enable master/slave manual configuration value
MS	11	RW	**Master/Slave Config Value** Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to logical one. See also IEEE 802.3-2008 40.5.1.1. **Constants** 0_B **SLAVE** Configure PHY as SLAVE during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one 1_B **MASTER** Configure PHY as MASTER during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one

Field	Bits	Type	Description
MSPT	10	RW	**Master/Slave Port Type** Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. See also IEEE 802.3-2008 40.5.1.1. **Constants** 0_B **SPD** Single-port device 1_B **MPD** Multi-port device
MBTFD	9	RW	**1000BASE-T Full-Duplex** Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode. See also IEEE 802.3 40.5.1.1. **Constants** 0_B **DISABLED** Advertise PHY as not 1000BASE-T full-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T full-duplex capable
MBTHD	8	RW	**1000BASE-T Half-Duplex** Advertises the 1000BASE-T half-duplex capability; always forced to 1 in converter mode. See IEEE 802.3 40.5.1.1. **Constants** 0_B **DISABLED** Advertise PHY as not 1000BASE-T half-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T half-duplex capable
RES	7:0	RO	**Reserved** Write as zero, ignore on read.

Gigabit Status Register

This is the status register used to reflect the Gigabit Ethernet status of the PHY. See also IEEE 802.3-2008 40.5.1.1.

GSTAT **Offset** **Reset Value**

Gigabit Status Register **$0A_H$** **0000_H**

15	14	13	12	11	10	9	8
MSFAULT	**MSRES**	**LRXSTAT**	**RRXSTAT**	**MBTFD**	**MBTHD**	**RES**	
rolh	ro	ro	ro	ro	ro	ro	
7							0
IEC							
rosc							

Field	Bits	Type	Description
MSFAULT	15	ROLH	**Master/Slave Manual Configuration Fault** This is a latching high bit. It is cleared upon each read of GSTAT. This bit will self clear on auto-negotiation enable or auto-negotiation complete. This bit will be set to active high if the number of failed master/slave resolutions reaches 7. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **OK** Master/slave manual configuration resolved successfully 1_B **NOK** Master/slave manual configuration resolved with a fault
MSRES	14	RO	**Master/Slave Configuration Resolution** See IEEE 802.3 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **SLAVE** Local PHY configuration resolved to SLAVE 1_B **MASTER** Local PHY configuration resolved to MASTER
LRXSTAT	13	RO	**Local Receiver Status** Indicates the status of the local receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **NOK** Local receiver not OK 1_B **OK** Local receiver OK
RRXSTAT	12	RO	**Remote Receiver Status** Indicates the status of the remote receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **NOK** Remote receiver not OK 1_B **OK** Remote receiver OK
MBTFD	11	RO	**Link-Partner Capable of Operating 1000BASE-T Full-Duplex** See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex
MBTHD	10	RO	**Link-Partner Capable of Operating 1000BASE-T Half-Duplex** See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex
RES	9:8	RO	**Reserved** Write as zero, ignore on read.

Field	Bits	Type	Description
IEC	7:0	ROSC	**Idle Error Count** Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the GSTAT register is read by the management function or upon execution of the PCS reset function, and are to be held at all ones in case of overflow.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment(PSE) control functions (see IEEE 802.3-2008 33.6.1.1), which is not supported by this PHY.

RES11 **Offset** **Reset Value**

Reserved **$0B_H$** **0000_H**

15							8
RES							
ro							
7							0
RES							
ro							

Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment(PSE) status functions (see IEEE 802.3-2008 33.6.1.2), which is not supported by this PHY.

RES12 **Offset** **Reset Value**

Reserved **$0C_H$** **0000_H**

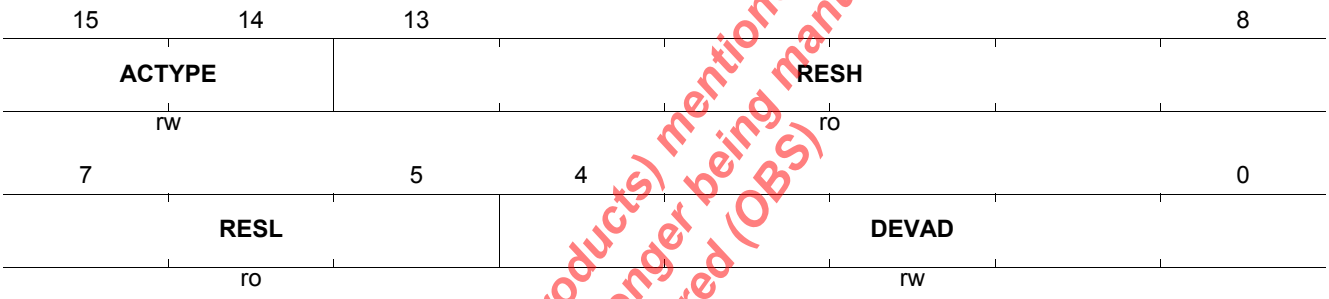
15							8
RES							
ro							
7							0
RES							
ro							

Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

MMD Access Control Register

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. Each MMD maintains its own individual address register, as described in IEEE 802.3-2008 clause 45.2.8. The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2. For additional insight into the operation and use of the MMD registers, see IEEE 802.3-2008 clause 22.2.4.3.11, Annex 22D and clause 45.2.

MMDCTRL — **MMD Access Control Register** — **Offset** $0D_H$ — **Reset Value** 0000_H



Field	Bits	Type	Description
ACTYPE	15:14	RW	**Access Type Function** If the access of register MMDDATA is an address access (ACTYPE=0) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD. The function field can be set to any of the constants defined (ADDRESS, DATA, DATA_PI, DATA_PIWR). **Constants** 00_B **ADDRESS** Accesses to register MMDDATA access the MMD individual address register 01_B **DATA** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register 10_B **DATA_PI** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register. After this access is complete, for both read and write accesses, the value in the MMD address field is incremented. 11_B **DATA_PIWR** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register. After this access is complete, for write accesses only, the value in the MMDs address field is incremented. For read accesses, the value in the MMDs address field is not modified.

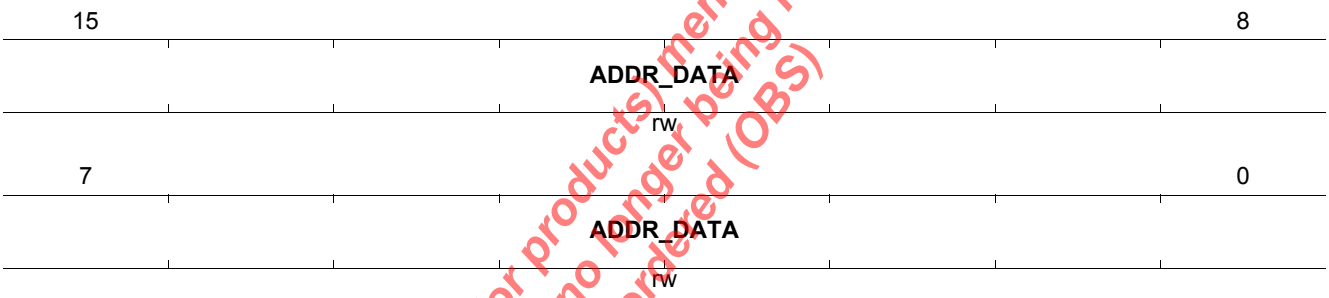
Field	Bits	Type	Description
RESH	13:8	RO	**Reserved** Write as zero, ignored on read.
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.
DEVAD	4:0	RW	**Device Address** The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2.

MMD Access Data Register

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 clause 22.2.4.3.12, clause 45.2 and Annex 22D.

MMDDATA — **Offset** — **Reset Value**

MMD Access Data Register — **$0E_H$** — **0000_H**

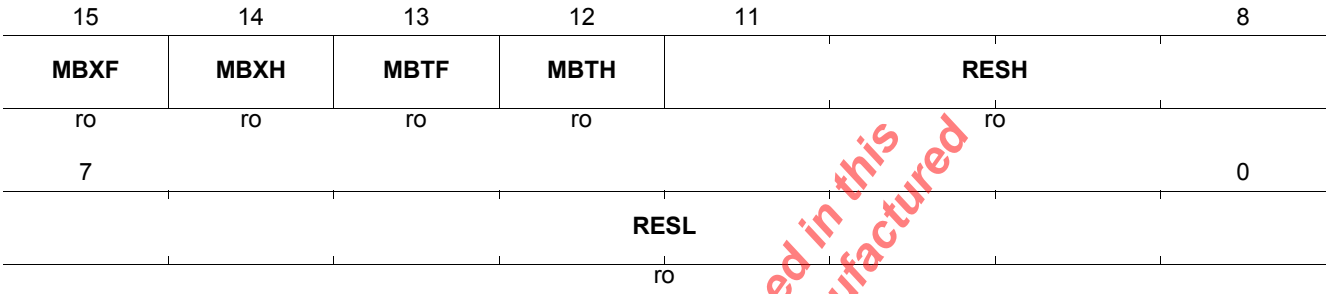


Field	Bits	Type	Description
ADDR_DATA	15:0	RW	**Address or Data Register** This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register.

Extended Status Register

This register contains extended status and capability information about the PHY. Note that all bits are read-only. A write access does not have any effect.

XSTAT	Offset	Reset Value
Extended Status Register	$0F_H$	3000_H



Field	Bits	Type	Description
MBXF	15	RO	**1000BASE-X Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBXH	14	RO	**1000BASE-X Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X half-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTF	13	RO	**1000BASE-T Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTH	12	RO	**1000BASE-T Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
RESH	11:8	RO	**Reserved** Ignore when read.
RESL	7:0	RO	**Reserved** Ignore when read.

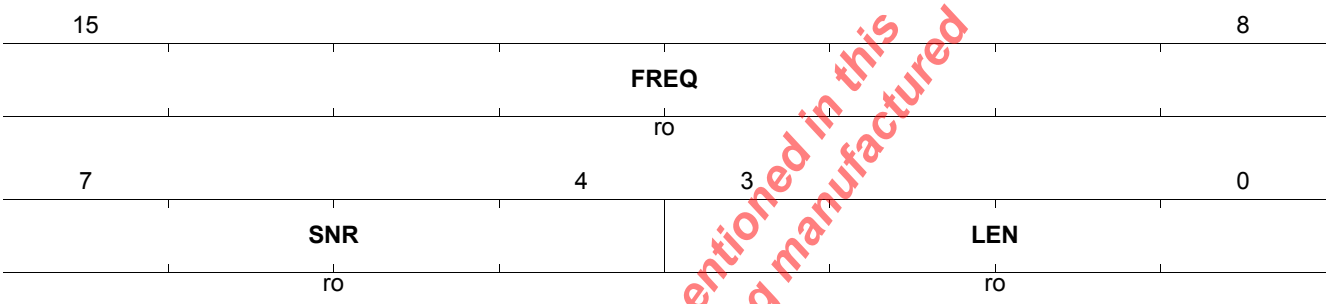
4.2.2 PHY: PHY-Specific Management Registers

This chapter describes the PHY-specific management registers.

Physical Layer Performance Status

This register reports the PHY performance in the current mode of operation. The content of this register is only valid when the link is up.

PHYPERF	Offset	Reset Value
Physical Layer Performance Status	10_H	$80FF_H$

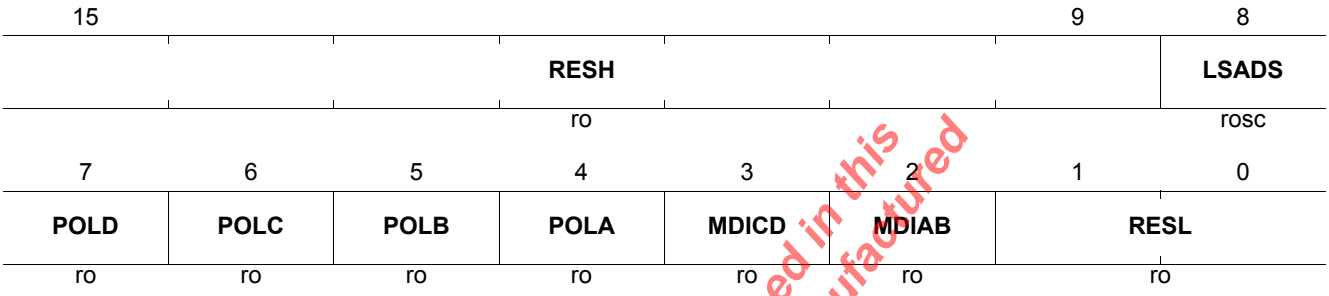


Field	Bits	Type	Description
FREQ	15:8	RO	**Frequency Offset of Link-Partner [ppm]** This register fields reports the measured frequency offset of the receiver in ppm as a signed 2's complement number. Note that a value of -128 (0x80) indicates an invalid number.
SNR	7:4	RO	**Receive SNR Margin [dB]** This register field reports the measured SNR margin of the receiver in dB. The value saturates at a 14-dB SNR margin for very short links and 0 dB for very long links. A value of 15 indicates an invalid number. **Constants** 1111_B**INVALID** Invalid value
LEN	3:0	RO	**Estimated Loop Length (Valid During Link-Up)** This register field reports the estimated loop length compared to a virtually ideal CAT5e straight cable. The unit is LEN x 10m. A value of 15 indicates an invalid number.

Physical Layer Status 1

This register reports PHY lock information, for example link-up, polarity reversals and port mapping. The content of this register is only valid when the link is up.

PHYSTAT1	Offset	Reset Value
Physical Layer Status 1	11_H	0000_H



Field	Bits	Type	Description
RESH	15:9	RO	**Reserved** Write as zero, ignored on read.
LSADS	8	ROSC	**Link-Speed Auto-Downspeed Status** Monitors the status of the link speed auto-downspeed controlled in PHYCTL1.LDADS. **Constants** 0_B **NORMAL** Did not perform any link speed auto-downspeed 1_B **DETECTED** Detected an auto-downspeed
POLD	7	RO	**Receive Polarity Inversion Status on Port D** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLC	6	RO	**Receive Polarity Inversion Status on Port C** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLB	5	RO	**Receive Polarity Inversion Status on Port B** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLA	4	RO	**Receive Polarity Inversion Status on Port A** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
MDICD	3	RO	**Mapping of MDI ports C and D** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode

Field	Bits	Type	Description
MDIAB	2	RO	**Mapping of MDI ports A and B** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
RESL	1:0	RO	**Reserved** Write as zero, ignored on read.

Physical Layer Status 2

This register reports PHY lock information, for example, pair skews in the GbE mode. The content of this register is only valid when the link is up.

PHYSTAT2 **Offset** **Reset Value**

Physical Layer Status 2 **12_H** **0000_H**

15	14	12	11	10	8
RESD	**SKEWD**		**RESC**	**SKEWC**	
ro	ro		ro	ro	

7	6	4	3	2	0
RESB	**SKEWB**		**RESA**	**SKEWA**	
ro	ro		ro	ro	

Field	Bits	Type	Description
RESD	15	RO	**Reserved** Write as zero, ignored on read.
SKEWD	14:12	RO	**Receive Skew on Port D** The skew is reported as an unsigned number of symbol periods.
RESC	11	RO	**Reserved** Write as zero, ignored on read.
SKEWC	10:8	RO	**Receive Skew on Port C** The skew is reported as an unsigned number of symbol periods.
RESB	7	RO	**Reserved** Write as zero, ignored on read.
SKEWB	6:4	RO	**Receive Skew on Port B** The skew is reported as an unsigned number of symbol periods.
RESA	3	RO	**Reserved** Write as zero, ignored on read.
SKEWA	2:0	RO	**Receive Skew on Port A** The skew is reported as an unsigned number of symbol periods.

Physical Layer Control 1

This register controls the PHY functions.

PHYCTL1	Offset	Reset Value
Physical Layer Control 1	13_H	0003_H

15	14	13	12	11	10	9	8
TLOOP			TXOFF	TXADJ			
rw			rw	rw			

7	6	5	4	3	2	1	0
POLD	POLC	POLB	POLA	MDICD	MDIAB	TXEEE10	AMDIX
rw	rw	rw	rw	rw	rw	ro	rw

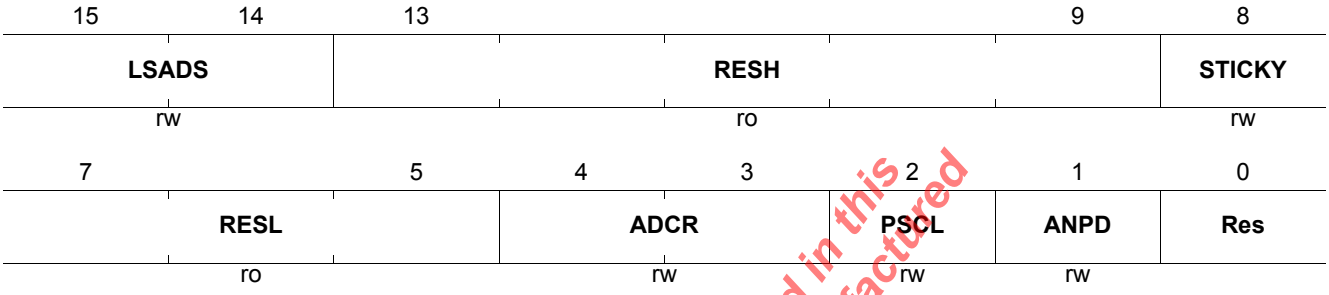
Field	Bits	Type	Description
TLOOP	15:13	RW	**Test Loop** Configures predefined test loops. **Constants** 000_B **OFF** Test loops are switched off - normal operation. 001_B **NETL** Near-end test loop 010_B **FETL** Far-end test loop 011_B **ECHO** Echo test loop 100_B **RJTL** RL45 connector test loop 101_B **FETLS** Standalone Far-end test loop. No dependency on TX_CLK and RX_CLK on the (G)MII interface
TXOFF	12	RW	**Transmitter Off** This register bit allows turning off of the transmitter. This feature might be useful for return loss measurements. **Constants** 0_B **ON** Transmitter is on 1_B **OFF** Transmitter is off
TXADJ	11:8	RW	**Transmit Level Adjustment** Transmit-level adjustment can be used to fine tune the transmit amplitude of the PHY. The amplitude adjustment is valid for all supported speed modes. The adjustment is performed in digits. One digit represents 3.125 percent of the nominal amplitude. The scaling factor is gain = 1 + signed(TXADJ)*2^-7.
POLD	7	RW	**Transmit Polarity Inversion Status on Port D** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLC	6	RW	**Transmit Polarity Inversion Status on Port C** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion

Field	Bits	Type	Description
POLB	5	RW	**Transmit Polarity Inversion Control on Port B** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLA	4	RW	**Transmit Polarity Inversion Control on Port A** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
MDICD	3	RW	**Mapping of MDI Ports C and D** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RW	**Mapping of MDI Ports A and B** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
TXEEE10	1	RO	**Transmit Energy-Efficient Ethernet 10BASE-Te Amplitude** This register bit allows enabling of the 10BASE-Te energy-efficient mode transmitting only with a 1.75 V nominal amplitude. **Constants** 0_B **DISABLED** Transmit the 10Base-T amplitude, that is, 2.3 V 1_B **ENABLED** Transmit the 10BASE-Te amplitude, that is, 1.75 V
AMDIX	0	RW	**PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X** **Constants** 0_B **MANUAL** PHY uses manual MDI/MDI-X 1_B **AUTO** PHY performs Auto-MDI/MDI-X

Physical Layer Control 2

This register controls the PHY functions.

PHYCTL2	Offset	Reset Value
Physical Layer Control 2	14_H	8006_H



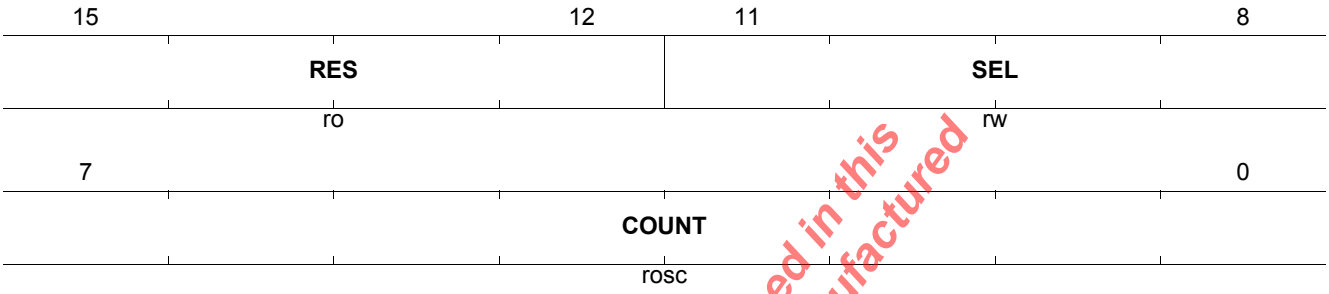
Field	Bits	Type	Description
LSADS	15:14	RW	**Link Speed Auto-Downspeed Control Register** Link speed auto-downspeed is a functionality which allows an Ethernet link to be established even in non-standard harsh cable environments. **Constants applicable for V1.1** 00_B **Reserved** 01_B **ADS2** Perform auto-downspeed of link speed after 1 consecutive failed link-ups 10_B **ADS3** Perform auto-downspeed of link speed after 2 consecutive failed link-ups 11_B **ADS4** Perform auto-downspeed of link speed after 3 consecutive failed link-ups **Constants applicable for V1.2** 00_B **Reserved** 01_B **ADS2** Perform auto-downspeed of link speed after 4 consecutive failed link-ups 10_B **ADS3** Perform auto-downspeed of link speed after 6 consecutive failed link-ups 11_B **ADS4** Perform auto-downspeed of link speed after 8 consecutive failed link-ups
RESH	13:9	RO	**Reserved** Write as zero, ignored on read.
STICKY	8	RW	**Sticky-Bit Handling** Allows enabling/disabling of the sticky-bit handling for all PHY-specific MDIO register bits of type RW, except for the TPGCTRL register. This means that the current content of these registers is left untouched during a software reset if sticky-bit handling is enabled. **Constants** 0_B **OFF** Sticky-bit handling is disabled 1_B **ON** Sticky-bit handling is enabled

Field	Bits	Type	Description
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.
ADCR	4:3	RW	**ADC Resolution Boost.** Allows for the ADC resolution to be increased. **Constants** 00_B **DEFAULT** Default ADC resolution. 01_B **BOOST** ADC resolution boost.
PSCL	2	RW	**Power-Consumption Scaling Depending on Link Quality** Allows enabling/disabling of the power-consumption scaling dependent on the link quality. **Constants** 0_B **OFF** PSCL is disabled 1_B **ON** PSCL is enabled
ANPD	1	RW	**Auto-Negotiation Power Down** Allows enabling/disabling of the power-down Modes during auto-negotiation looking for a link partner. **Constants** 0_B **OFF** ANPD is disabled 1_B **ON** ANPD is enabled

Error Counter

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

ERRCNT	Offset	Reset Value
Error Counter	15_H	0000_H

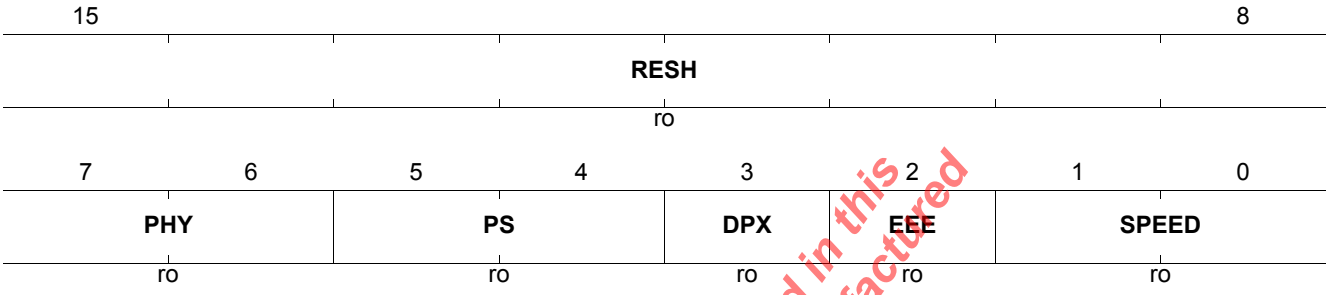


Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Write as zero, ignored on read.
SEL	11:8	RW	**Select Error Event** Configures the error/event to which the error counter is sensitive. **Constants** 0000_B **RXERR** Receive errors are counted 0001_B **RXACT** Receive frames are counted 0010_B **ESDERR** ESD errors are counted 0011_B **SSDERR** SSD errors are counted 0100_B **TXERR** Transmit errors are counted 0101_B **TXACT** Transmit frames events get counted 0110_B **COL** Collision events get counted 1000_B **NLD** Number of Link Down get counted 1001_B **NDS** Number of auto-downspeed get counted
COUNT	7:0	ROSC	**Counter State** This counter state is updated each time the selected error event has been detected. The counter state is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value 0xFF.

Media-Independent Interface Status

This register contains status information of the MII interface.

MIISTAT	Offset	Reset Value
Media-Independent Interface Status	18_H	0000_H



Field	Bits	Type	Description
RESH	15:8	RO	**Reserved** Write as zero, ignored on read.
PHY	7:6	RO	**Active PHY Interface.** **Constants** 00_B **TP** The twisted-pair interface is the active PHY interface 01_B **FIBER** The fiber interface is the active PHY interface 10_B **MII2** The second MII interface is the active PHY interface 11_B **SGMII** The SGMII interface is the active PHY interface
PS	5:4	RO	**Resolved Pause Status for Flow Control** **Constants** 00_B **NONE** No PAUSE 01_B **TX** Transmit PAUSE 10_B **RX** Receive PAUSE 11_B **TXRX** Both transmit and receive PAUSE
DPX	3	RO	**Duplex mode at which the MII currently operates.** **Constants** 0_B **HDX** Half duplex 1_B **FDX** Full duplex
EEE	2	RO	**Resolved Energy-Efficient Ethernet Mode** **Constants** 0_B **OFF** EEE is disabled after auto-negotiation resolution 1_B **ON** EEE is enabled after auto-negotiation resolution
SPEED	1:0	RO	**PHY Speed at which the MII Currently Operates.** **Constants** 00_B **TEN** 10 Mbit/s 01_B **FAST** 100 Mbit/s 10_B **GIGA** 1000 Mbit/s 11_B **FRE** FRE mode

Interrupt Mask Register

This register defines the mask for the Interrupt Status Register (ISTAT). Each masked interrupt is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTAT register. A read operation on the ISTAT register simultaneously clears the interrupts, deactivating MDINT.

IMASK	Offset	Reset Value
Interrupt Mask Register	19_H	0000_H

15	14	13	12	11	10	9	8
WOL	MSRE	NPRX	NPTX	ANE	ANC	AMBF	LOR
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
RESL		ADSC	MDIPC	MDIXC	DXMC	LSPC	LSTC
ro		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WOL	15	RW	**Wake-On-LAN Event Mask** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MSRE	14	RW	**Master/Slave Resolution Error Mask** When active, MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	RW	**Next Page Received Mask** When active, MDINT is activated upon reception of a next page in STD.AN_NPRX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	RW	**Next Page Transmitted Mask** When active, MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
ANE	11	RW	**Auto-Negotiation Error Mask** When active, MDINT is activated upon detection of an auto-negotiation error. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANC	10	RW	**Auto-Negotiation Complete Mask** When active, MDINT is activated upon completion of the auto-negotiation process. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
AMBF	9	RW	**MDIO Handling Fault** When active, MDINT is activated upon detection that the MDIO handling FIFO has overflowed and as such flushed and init by FW. This shall indicate that one or more of the MDIO transactions before this event may be lost. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LOR	8	RW	**SyncE Lost Of Reference** When active, MDINT is activated upon detection that the SyncE reference clock is lost. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESL	7:6	RO	**Reserved** Write as zeroes, ignore on read.
ADSC	5	RW	**Link-Speed Auto-Downspeed Detect Mask** When active, MDINT is activated upon detection of a link speed auto-downspeed event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	RW	**MDI Polarity Change Detect Mask** When active, MDINT is activated upon detection of an MDI polarity change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	RW	**MDIX Change Detect Mask** When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
DXMC	2	RW	**Duplex Mode Change Mask** When active, MDINT is activated upon detection of full- or half-duplex change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	RW	**Link Speed Change Mask** When active, MDINT is activated upon detection of link speed change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSTC	0	RW	**Link State Change Mask** When active, MDINT is activated upon detection of link status change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Interrupt Status Register

This register defines the Interrupt Status Register (ISTAT). Each masked interrupt (IMASK) is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTA register. A read operation on the ISTAT register simultaneously clears the interrupts and this deactivates MDINT.

ISTAT **Offset** **Reset Value**

Interrupt Status Register **$1A_H$** **0000_H**

15	14	13	12	11	10	9	8
WOL	**MSRE**	**NPRX**	**NPTX**	**ANE**	**ANC**	**AMBF**	**LOR**
rolh	rolh	rolh	rolh	rolh	rolh	rw	rolh
7	6	5	4	3	2	1	0
RESL		**ADSC**	**MDIPC**	**MDIXC**	**DXMC**	**LSPC**	**LSTC**
rolh		rolh	rolh	rolh	rolh	rolh	rolh

Field	Bits	Type	Description
WOL	15	ROLH	**Wake-On-LAN Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
MSRE	14	ROLH	**Master/Slave Resolution Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	ROLH	**Next Page Received Interrupt Status** When active and masked in IMASK, the MDINT is activated upon reception of a next page in STD.AN_NPRX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	ROLH	**Next Page Transmitted Interrupt Status** When active and masked in IMASK, the MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANE	11	ROLH	**Auto-Negotiation Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an auto-negotiation error. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANC	10	ROLH	**Auto-Negotiation Complete Interrupt Status** When active and masked in IMASK, the MDINT is activated upon completion of the auto-negotiation process. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
AMBF	9	RW	**MDIO Handling Fault** When active and masked in IMASK, MDINT is activated upon detection that the MDIO handling FIFO has overflowed and as such flushed and init by FW. This shall indicate that one or more of the MDIO transactions before this event may be lost. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LOR	8	ROLH	**SyncE Lost Of Reference** When active and masked in IMASK, MDINT is activated upon detection that the SyncE reference clock is lost. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESL	7:6	ROLH	**Reserved** Write as zeros, ignore on read.

Field	Bits	Type	Description
ADSC	5	ROLH	**Link Speed Auto-Downspeed Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a link speed auto-downspeed event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	ROLH	**MDI Polarity Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI polarity change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	ROLH	**MDIX Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI/MDIX cross-over change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
DXMC	2	ROLH	**Duplex Mode Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a full or half-duplex change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	ROLH	**Link Speed Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link speed change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSTC	0	ROLH	**Link State Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link status change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

LED Control Register

This register contains control bits to allow for direct access to the LEDs. A directly controlled LED must disable the integrated LED function as specified by the more sophisticated LED control registers in page LED.

LED	Offset	Reset Value
LED Control Register	$1B_H$	$0F00_H$

15	14	13	12	11	10	9	8
RESH				LED3EN	LED2EN	LED1EN	LED0EN
ro				rw	rw	rw	rw

7	6	5	4	3	2	1	0
RESL				LED3DA	LED2DA	LED1DA	LED0DA
ro				rw	rw	rw	rw

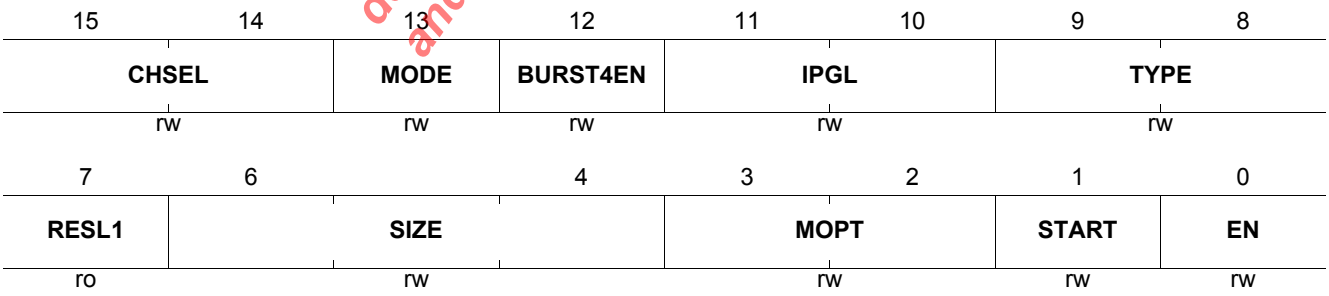
Field	Bits	Type	Description
RESH	15:12	RO	**Reserved** Write as zero, ignored on read.
LED3EN	11	RW	**Enable the integrated function of LED3** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED3DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED2EN	10	RW	**Enable the integrated function of LED2** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED1EN	9	RW	**Enable the Integrated Function of LED1** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED0EN	8	RW	**Enable the Integrated Function of LED0** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
RESL	7:4	RO	**Reserved** Write as zero, ignored on read.

Field	Bits	Type	Description
LED3DA	3	RW	**Direct Access to LED3** Write a logic 1 to this bit to illuminate the LED. Note that LED3EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED2DA	2	RW	**Direct Access to LED2** Write a logic 1 to this bit to illuminate the LED. Note that LED2EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED1DA	1	RW	**Direct Access to LED1** Write a logic 1 to this bit to illuminate the LED. Note that LED1EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED0DA	0	RW	**Direct Access to LED0** Write a logic 1 to this bit to illuminate the LED. Note that LED0EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED

Test-Packet Generator Control

This register controls the operation of the integrated Test-Packet Generator (TPG). Note that this module is only used for testing purposes.

TPGCTRL	Offset	Reset Value
Test-Packet Generator Control	$1C_H$	0000_H



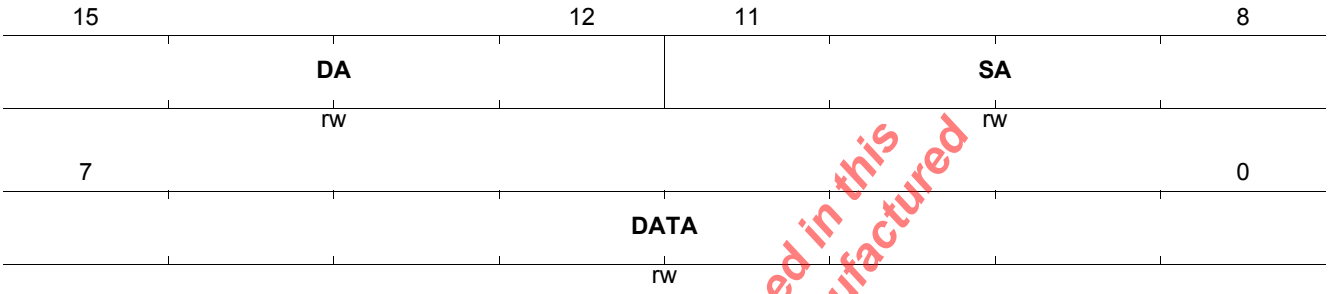
Field	Bits	Type	Description
CHSEL	15:14	RW	**Channel Selection** There are 4 channels in the IP which can be selected for debug data dumping. Note that this field is not used in case BURST4EN=1 && MOPT=1 (auto-channel burst). **Constants** 00_B **CHA** Channel A is selected 01_B **CHB** Channel B is selected 10_B **CHC** Channel C is selected 11_B **CHD** Channel D is selected
MODE	13	RW	**Mode of the TPG** Configures the packet generation mode **Constants** 0_B **CONTINUOUS** Send packets continuously 1_B **SINGLE** Send a single packet. Also used to send a single burst of 4 packets in debug dumping when selected.
BURST4EN	12	RW	**Burst Of 4 packets Enable** When Enabled, this indicates to the packet generator to auto-select based on MOPT the debug data configuration per packet in the burst of 4. when MOPT=0, then the packets will be generated capturing for the selected ASP channel, the polyphases 0,1,2,3 respectively. When MOPT=1 then the packets will be generated capturing for the selected DVC option, the channels A,B,C,D respectively. Note that this will lead to a burst of 4 packets if MODE=SINGLE. In case MODE=1(continuous), then we will get packets where every group of 4 packets are generated according to the MOPT selection. **Constants** 0_B **DISABLE** Disable 1_B **ENABLE** Enable Burst of 4 packet generation
IPGL	11:10	RW	**Inter-Packet Gap Length** Configures the length of the inter-packet gap in bit times. **Constants** 00_B **BT48** Length is 48 bit times 01_B **BT96** Length is 96 bit times 10_B **BT960** Length is 960 bit times 11_B **BT9600** Length is 9600 bit times
TYPE	9:8	RW	**Packet Data Type** Configures the packet data type to be either predefined, byte increment or random. If pre-defined, the content of the register TPGDATA is used repetitively. **Constants** 00_B **RANDOM** Use random data as the packet content 01_B **BYTEINC** Use byte increment as the packet content 10_B **PREDEF** Use pre-defined content of the register TPGDATA 11_B **DBGDATA** Use Dbg data as packet content. Additional Configuration will be taken from TPGDATA
RESL1	7	RO	**Reserved.** Write as zero, ignore on read.

Field	Bits	Type	Description
SIZE	6:4	RW	**Packet Size** Configures the size of the generated Ethernet packets in bytes. The size includes DA, SA, length/type, payload and FCS. **Constants** 000_B **L64** Packet length is 64 bytes. 001_B **L2048** Packet length is 2048 bytes (jumbo frames). 010_B **L256** Packet length is 256 bytes. 011_B **L4096** Packet length is 4096 bytes (jumbo frames). 100_B **L1024** Packet length is 1024 bytes. 101_B **L1518** Packet length is 1518 bytes. 110_B **L9000** Packet length is 9000 bytes (jumbo frames). 111_B **RANDOM** Packet length is randomized between upper sizes without jumbo frames.
MOPT	3:2	RW	**Mux Option** Additional Mux Selection Options depending on the value of DVC in TPGDATA[3:0] **Constants** 00_B **MOPT0** BURST4EN=1: auto-polyphase selected, BURST4EN=0 && DVC=0b1001: DBG SYNC Data Gen, otherwise sub-DVC-mode selection 01_B **MOPT1** BURST4EN=1: auto-channel selected, BURST4EN=0 && DVC=0b1001: DBG Trace Data, otherwise sub-DVC-mode selection 10_B **MOPT2** sub-DVC-mode selection 11_B **MOPT3** sub-DVC-mode selection
START	1	RW	**Start or Stop TPG Data Generation.** Starts the TPG data generation. Depending on the MODE, the TPG sends only 1 single packet or chunks of 10,000 packets until stopped. **Constants** 0_B **STOP** Stops the TPG data generation 1_B **START** Starts the TPG data generation
EN	0	RW	**Enable the TPG** Enables the TPG for data generation. **Constants** 0_B **DISABLE** Disables the TPG 1_B **ENABLE** Enables the TPG

Test-Packet Generator Data

Specifies the payload data to be used when sending a non-random data packet. All payload data bytes are sent with this value.

TPGDATA	Offset	Reset Value
Test-Packet Generator Data	$1D_H$	$00AA_H$



Field	Bits	Type	Description
DA	15:12	RW	**Destination Address** Configures the destination address nibble. The Source Address builds up to 00-03-19-FF-FF-F[DA].
SA	11:8	RW	**Source Address** Configures the source address nibble. The source address builds up to 00-03-19-FF-FF-F[SA].
DATA	7:0	RW	**Data Byte to be Transmitted** This is the content of the payload bytes in the frame in case it is selected to send constant data. In case it is selected to send debug data, this byte has additional configuration as seen in the constants below. The bit masks are shown here. For detail configuration please refer to the respective chapter. **Constants** 00001111_B**DVC** Select the debug data to be dump 00010000_B**RESERVED** Reserved 01100000_B**PREC2** For reduce precision, select the options with bits [6:5] 10000000_B**PREC** select whether to take full precision('1') of reduce precision '0' at bit 7

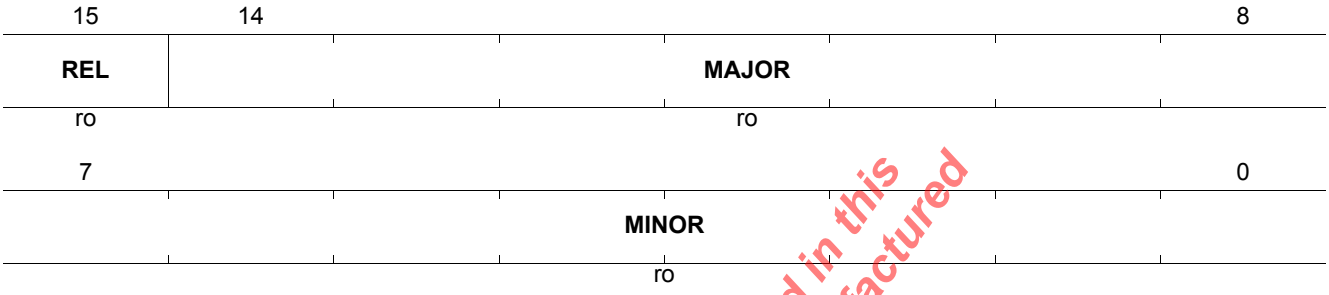
Firmware Version Register

This register contains the version of the PHY firmware.

FWV — **Firmware Version Register**

Offset $1E_H$

Reset Value 8304_H



Field	Bits	Type	Description
REL	15	RO	**Release Indication** This parameter indicates either a test or a release version. **Constants** 0_B **TEST** Indicates a test version 1_B **RELEASE** Indicates a released version
MAJOR	14:8	RO	**Major Version Number** Specifies the main version release number of the firmware.
MINOR	7:0	RO	**Minor Version Number** Specifies the sub-version release number of the firmware.

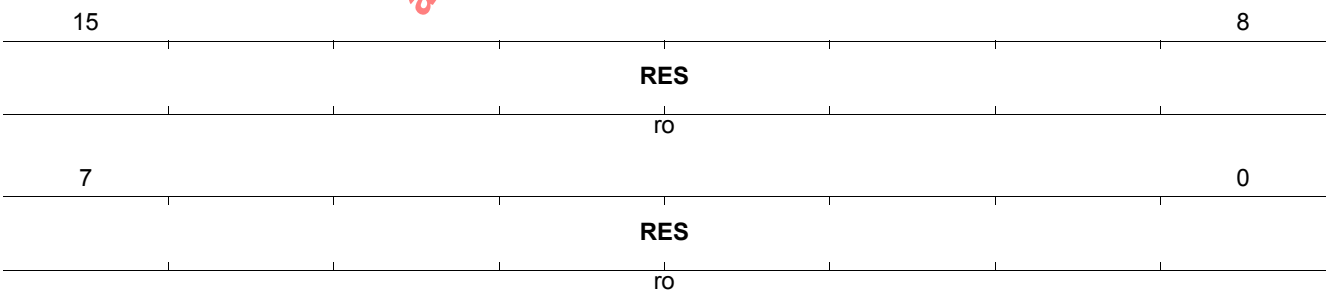
Reserved

Reserved.

RES1F — **Reserved**

Offset $1F_H$

Reset Value 0000_H



Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

4.3 PHY MMD Registers

This Chapter defines all the registers needed to operate the module "MMD_REGISTERS".[1)]

Table 68 Registers Address Space

Module	Base Address	End Address	Note
MMD_REGISTERS	000000_H	$1FFFFF_H$	

Table 69 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
PHY MMD Registers, PMAPMD: Standard PMAPMD Registers for MMD=0x01			
TIMESYNC_CAP	PMAPMD TimeSync Capability Indication	01.1800_H	0000_H
PHY MMD Registers, EEE: Standard EEE Registers for MMD=0x03			
EEE_CTRL1	EEE Control Register 1	03.0000_H	0000_H
EEE_STAT1	EEE Status Register 1	03.0001_H	0000_H
EEE_CAP	EEE Capability Register	03.0014_H	0006_H
EEE_WAKERR	EEE Status Register 1	03.0016_H	0000_H
PHY MMD Registers, ANEG: Standard Auto-Negotiation Registers for MMD=0x07			
EEE_AN_ADV	EEE Auto-Negotiation Advertisement Register	$07.003C_H$	0000_H
EEE_AN_LPADV	EEE Auto-Negotiation Link-Partner Advertisement Register	$07.003D_H$	0000_H
PHY MMD Registers, INTERNAL: Internal Address Space (MMD=0x1F)			
LEDCH	LED Configuration	$1F.01E0_H$	$00C5_H$
LEDCL	LED Configuration	$1F.01E1_H$	0067_H
LED0H	Configuration for LED Pin 0	$1F.01E2_H$	0070_H
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	0020_H
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	0040_H
LED3H	Configuration for LED Pin 3	$1F.01E8_H$	0040_H
LED0L	Configuration for LED Pin 0	$1F.01E3_H$	0003_H
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	0000_H
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	0000_H
LED3L	Configuration for LED Pin 3	$1F.01E9_H$	0020_H
EEE_RXERR_LINK_FAIL_H	High Byte of the EEE Link-Fail Counter	$1F.01EA_H$	0000_H
EEE_RXERR_LINK_FAIL_L	Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	0000_H
WOLCTRL	Wake-On-LAN Control Register	$1F.0781_H$	0000_H
WOLAD0	Wake-On-LAN Address Byte 0	$1F.0783_H$	0000_H
WOLAD1	Wake-On-LAN Address Byte 1	$1F.0784_H$	0000_H
WOLAD2	Wake-On-LAN Address Byte 2	$1F.0785_H$	0000_H

1) Generated by REFIGE v1.4 - Beta Release XIV

Table 69 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLAD3	Wake-On-LAN Address Byte 3	$1F.0786_H$	0000_H
WOLAD4	Wake-On-LAN Address Byte 4	$1F.0787_H$	0000_H
WOLAD5	Wake-On-LAN Address Byte 5	$1F.0788_H$	0000_H
WOLPW0	Wake-On-LAN SecureON Password Byte 0	$1F.0789_H$	0000_H
WOLPW1	Wake-On-LAN SecureON Password Byte 1	$1F.078A_H$	0000_H
WOLPW2	Wake-On-LAN SecureON Password Byte 2	$1F.078B_H$	0000_H
WOLPW3	Wake-On-LAN SecureON Password Byte 3	$1F.078C_H$	0000_H
WOLPW4	Wake-On-LAN SecureON Password Byte 4	$1F.078D_H$	0000_H
WOLPW5	Wake-On-LAN SecureON Password Byte 5	$1F.078E_H$	0000_H
PD_CTL	Configuration for Synchronous Ethernet	$1F.07FE_H$	0000_H

The register is addressed wordwise.

Table 70 Register Access Types

Mode	Symbol	Internal Hardware Configuration		
		Type	Behavior	Arbitration
Status Register, Latch-High	ROLH	WOR	AUTO_PDI	CLROR
Status Register, Latch-Low	ROLL	WOR	AUTO_PDI	CLROR
Status Register, Self-Clearing	ROSC	WOR	AUTO_PDI	CLROR
Read-Write Register	RW	RWR	AUTO_PDI	-
Read-Write Register, Self-Clearing	RWSC	RWR	AUTO_PDI	CLROR
Status Register	RO	WOR	AUTO_PDI	-

4.3.1 PMAPMD: Standard PMAPMD Registers for MMD=0x01

This section describe the registers for support of IEEE 802.3BF indication for TimeSync (a.k.a SyncT interface in this IP).

PMAPMD TimeSync Capability Indication

PMAPMD TimeSync Capability indication Register. Note that this IP does not support providing data path delay information. It is provided to enhance compatibility

TIMESYNC_CAP	Offset	Reset Value
PMAPMD TimeSync Capability Indication	01.1800_H	0000_H

Field	Bits	Type	Description
TXDEL	1	RO	**Transmit Data Path Delay Information** PHY indicates whether it is capable of providing the minimum and maximum data path delay information. **Constants** 0_B **NONE** PHY do not have this capability 1_B **CAPABLE** min and max TX data path delay available
RXDEL	0	RO	**Receive Data Path Delay Information** PHY indicates whether it is capable of providing the minimum and maximum data path delay information. **Constants** 0_B **NONE** PHY do not have this capability 1_B **CAPABLE** min and max RX data path delay available

4.3.2 EEE: Standard EEE Registers for MMD=0x03

This section describes the EEE registers for MMD device 0x03.

EEE Control Register 1

EEE Control Register 1.

EEE_CTRL1	Offset	Reset Value
EEE Control Register 1	**03.0000_H**	**0000_H**

15	11	10	9	8
Res		RXCKST	Res	
		rw		

7	0
Res	

Field	Bits	Type	Description
RXCKST	10	RW	**Receive Clock Stoppable** The MAC can set this bit to active to allow the PHY to stop the clocking during the LPI_MODE. **Constants** 0_B **DISABLE** The PHY must not stop the xMII clock during LPI_MODE 1_B **ENABLE** The PHY can stop the xMII clock during LPI_MODE

EEE Status Register 1

EEE Status Register 1.

EEE_STAT1	Offset	Reset Value
EEE Status Register 1	**03.0001_H**	**0000_H**

15	12	11	10	9	8
Res		TXLPI_RCVD	RXLPI_RCVD	TXLPI_IND	RXLPI_IND
		rolh	rolh	ro	ro

7	6	5	0
Res	TXCKST	Res	
	ro		

Field	Bits	Type	Description
TXLPI_RCVD	11	ROLH	**TXLPI Has Been Received** **Constants** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received
RXLPI_RCVD	10	ROLH	**RXLPI Has Been Received** **Constants** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received
TXLPI_IND	9	RO	**TXLPI Indication** **Constants** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
RXLPI_IND	8	RO	**RXLPI Indication** **Constants** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
TXCKST	6	RO	**Transmit Clock Stoppable** Indicate whether PHY is able to accept a stopped transmit clock during LPI_MODE. MAC may choose to stop the clocking during LPI_MODE if this bit is set to active. **Constants** 0_B **DISABLE** The PHY is not able to accept stopped transmit clocks(default) 1_B **ENABLE** The PHY is able to accept a stopped transmit clock during LPI_MODE

EEE Capability Register

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

EEE_CAP	Offset	Reset Value
EEE Capability Register	03.0014_H	0006_H

15							8
Res							

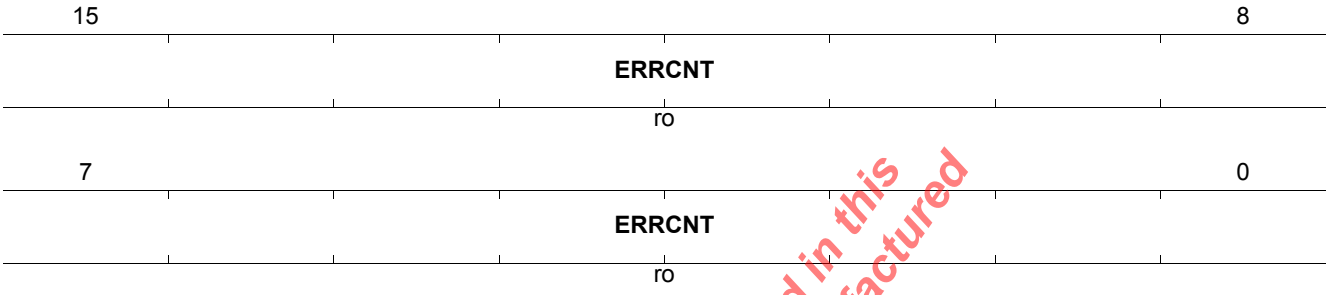
7	6	5	4	3	2	1	0
Res	EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	Res
	ro	ro	ro	ro	ro	ro	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Status Register 1

Not Specified

EEE_WAKERR	Offset	Reset Value
EEE Status Register 1	03.0016_H	0000_H



Field	Bits	Type	Description
ERRCNT	15:0	RO	**EEE Wake Error Counter** This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wake-up as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PCS reset. It is held at all ones in case of overflow.

4.3.3 ANEG: Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07 (only supporting EEE specifics).

EEE Auto-Negotiation Advertisement Register

This register defines the EEE advertisement that is sent in the unformatted next page following an EEE technology message code as defined in 28C.12. The 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to the bits in the unformatted next page. For PHYs that negotiate extended next-page support, the 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to bits U10 to U0 respectively of the extended next-page unformatted code field.

EEE_AN_ADV	Offset	Reset Value
EEE Auto-Negotiation Advertisement Register	$07.003C_H$	0000_H

15	14	13	12	11	10	9	8
Res							

7	6	5	4	3	2	1	0
Res	EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	Res
	ro	ro	ro	ro	rw	rw	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RW	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

Field	Bits	Type	Description
EEE_100BTX	1	RW	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Auto-Negotiation Link-Partner Advertisement Register

All of the bits in the EEE LP advertisement register are read only. A write operation to the EEE LP advertisement register has no effect. After the AN process has been completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement register.

EEE_AN_LPADV	Offset	Reset Value
EEE Auto-Negotiation Link-Partner Advertisement Register	**$07.003D_H$**	**0000_H**

15							8
Res							

7	6	5	4	3	2	1	0
Res	EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	Res
	ro	ro	ro	ro	ro	ro	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

Field	Bits	Type	Description
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

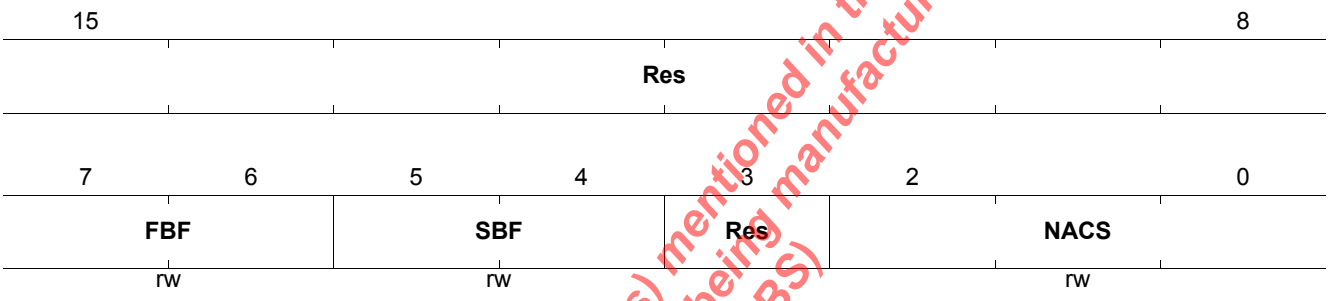
4.3.4 INTERNAL: Internal Address Space (MMD=0x1F)

This register file contains the PHY internal address space (MMD=0x1F).

LED Configuration

This register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state which is defined to activate complex LED functions, all LEDs are controlled according to the type of the complex function.

LEDCH	Offset	Reset Value
LED Configuration	$1F.01E0_H$	$00C5_H$



Field	Bits	Type	Description
FBF	7:6	RW	**Fast Blink Frequency** This register must be used to configure the fast-blinking frequency. Note that this setting implicitly defines the pulse-stretching width. **Constants** 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency
SBF	5:4	RW	**Slow Blink Frequency** This register must be used to configure the slow-blinking frequency. **Constants** 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency

Field	Bits	Type	Description
NACS	2:0	RW	**Inverse of SCAN Function** This configuration defines in which state the "complex SCAN" should be activated. The complex SCAN performs running off which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

LED Configuration

The register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state which is defined to activate complex LED functions all LEDs are controlled according to the type of the complex function.

LEDCL **Offset** **Reset Value**

LED Configuration **$1F.01E1_H$** **0067_H**

15	8
Res	

7	6	4	3	2	0
Res	SCAN		Res	CBLINK	
	rw			rw	

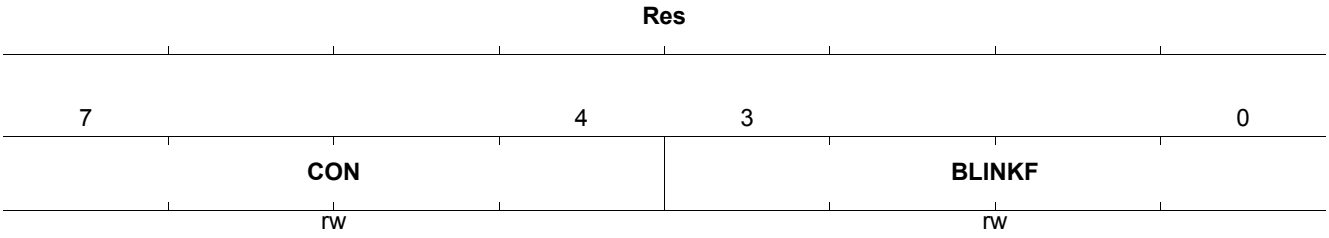
Field	Bits	Type	Description
SCAN	6:4	RW	**Complex SCAN Configuration** This configuration defines in which state the "complex SCAN" should be activated. The complex SCAN performs running on which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running
CBLINK	2:0	RW	**Complex Blinking Configuration** This configuration defines in which state the "complex blinking" should be activated. The complex blinking performs a blinking at the fast-blinking frequency on all LEDs simultaneously. This function can be used to indicate a special mode of the PHY such as cable-diagnostics or test. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event/state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0H	Offset	Reset Value
Configuration for LED Pin 0	**$1F.01E2_H$**	**0070_H**

15							8



Field	Bits	Type	Description
CON	7:4	RW	**Constant On Configuration** The Constant-ON field selects in which PHY states the LED is constantly on. **Constants** 0000_B**NONE** LED does not light up constantly 0001_B**LINK10** LED is on when link is 10 Mbit/s 0010_B**LINK100** LED is on when link is 100 Mbit/s 0011_B**LINK10X** LED is on when link is 10/100 Mbit/s 0100_B**LINK1000** LED is on when link is 1000 Mbit/s 0101_B**LINK10_0** LED is on when link is 10/1000 Mbit/s 0110_B**LINK100X** LED is on when link is 100/1000 Mbit/s 0111_B**LINK10XX** LED is on when link is 10/100/1000 Mbit/s 1000_B**PDOWN** LED is on when device is powered-down 1001_B**EEE** LED is on when device is in EEE mode 1010_B**ANEG** LED is on when auto-negotiation is running 1011_B**ABIST** LED is on when analog self-test is running 1100_B**CDIAG** LED is on when cable diagnostics are running 1101_B**COPPER** LED is on when the COPPER interface is selected 1110_B**FIBER** LED is on when the FIBER or an interface other than copper is selected 1111_B**RESERVED** Reserved for future use
BLINKF	3:0	RW	**Fast Blinking Configuration** The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. **Constants** 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbit/s 0010_B**LINK100** Blink when link is 100 Mbit/s 0011_B**LINK10X** Blink when link is 10/100 Mbit/s 0100_B**LINK1000** Blink when link is 1000 Mbit/s 0101_B**LINK10_0** Blink when link is 10/1000 Mbit/s 0110_B**LINK100X** Blink when link is 100/1000 Mbit/s 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbit/s 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running

Similar Registers

The following registers are identical to the Register **LED0H** defined above.

Table 71 Similar Registers

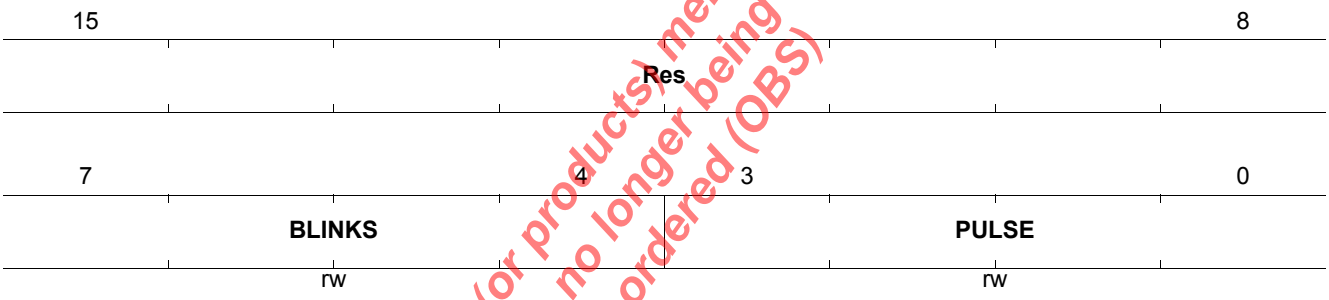
Register Short Name	Register Long Name	Offset Address	Reset Value
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	0020_H
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	0040_H
LED3H	Configuration for LED Pin 3	$1F.01E8_H$	0040_H

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event or state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0L **Offset** **Reset Value**

Configuration for LED Pin 0 **$1F.01E3_H$** **0003_H**



Field	Bits	Type	Description
BLINKS	7:4	RW	**Slow Blinking Configuration** The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. **Constants** 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbit/s 0010_B**LINK100** Blink when link is 100 Mbit/s 0011_B**LINK10X** Blink when link is 10/100 Mbit/s 0100_B**LINK1000** Blink when link is 1000 Mbit/s 0101_B**LINK10_0** Blink when link is 10/1000 Mbit/s 0110_B**LINK100X** Blink when link is 100/1000 Mbit/s 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbit/s 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running

Field	Bits	Type	Description
PULSE	3:0	RW	**Pulsing Configuration** The pulse field is a mask field by which certain events can be combined, e.g. TXACT|RXACT, to generate a pulse on the LED in case such an event has been detected. **Constants** 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**RES** Reserved

Similar Registers

The following registers are identical to the Register **LED0L** defined above.

Table 72 Similar Registers

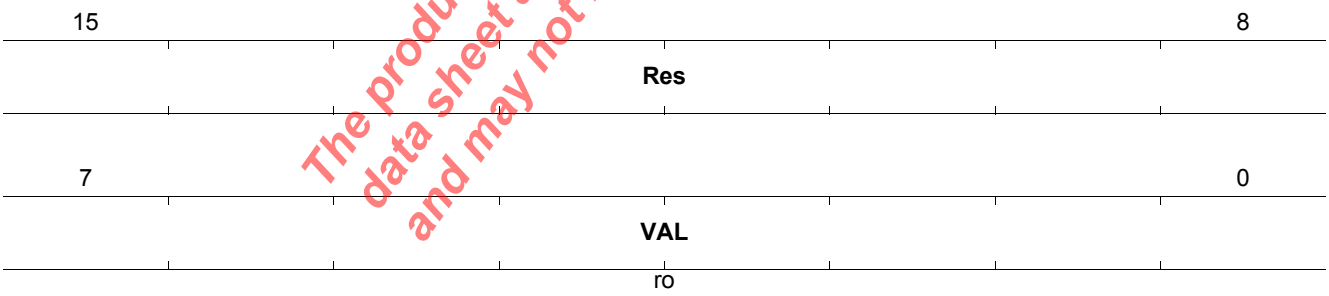
Register Short Name	Register Long Name	Offset Address	Reset Value
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	0000_H
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	0000_H
LED3L	Configuration for LED Pin 3	$1F.01E9_H$	0020_H

High Byte of the EEE Link-Fail Counter

High Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_H **Offset** **Reset Value**

High Byte of the EEE Link-Fail Counter **$1F.01EA_H$** **0000_H**

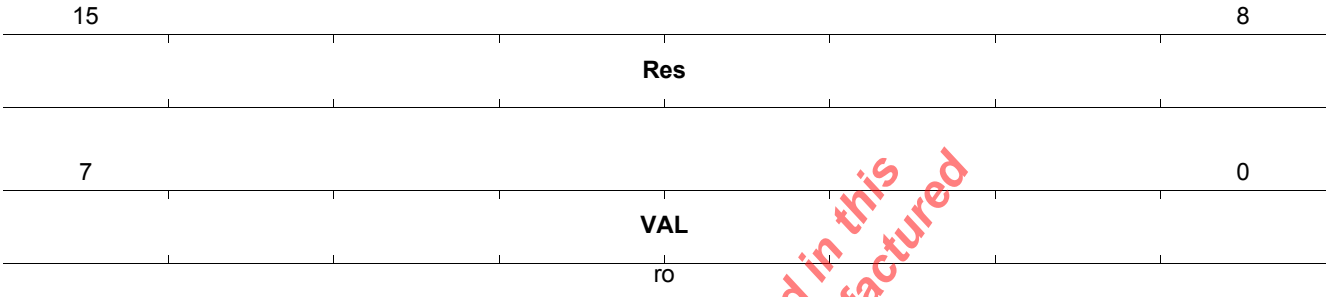


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** High byte of the EEE_RXERR_LINK_FAIL counter. A read access to the low byte also clears the high byte of this counter.

Low Byte of the EEE Link-Fail Counter

Low Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_L	Offset	Reset Value
Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	0000_H

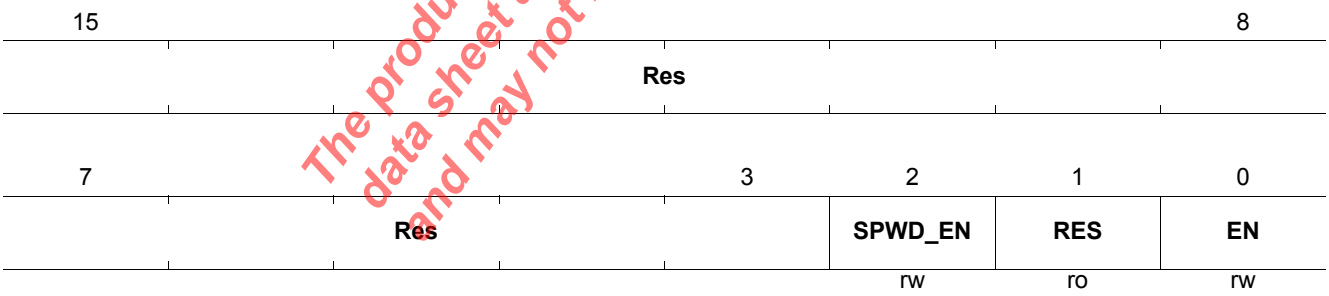


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** Low byte of the EEE_RXERR_LINK_FAIL counter. A read access to this byte also clears the high byte of this counter.

Wake-On-LAN Control Register

Wake-On-LAN Control Register.

WOLCTRL	Offset	Reset Value
Wake-On-LAN Control Register	$1F.0781_H$	0000_H



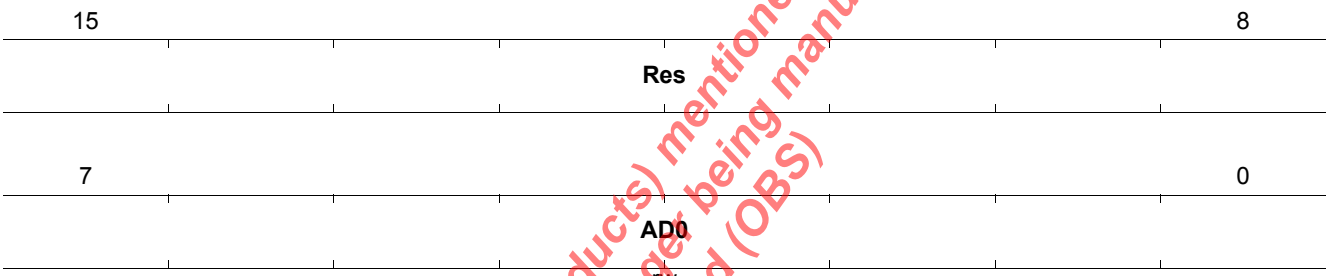
Field	Bits	Type	Description
SPWD_EN	2	RW	**Secure-ON Password Enable** If enabled, checks for the Secure-ON password after the 16 MAC address repetitions. **Constants** 0_B **DISABLED** Secure-On password check is disabled 1_B **ENABLED** Secure-On password check is enabled
RES	1	RO	**Reserved** Must always be written to zero!

Field	Bits	Type	Description
EN	0	RW	**Enables the Wake-On-LAN functionality** If Wake-On-LAN is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT.WOL, and optionally also via interrupt. **Constants** 0_B **DISABLED** Wake-On-LAN functionality is disabled 1_B **ENABLED** Wake-On-LAN functionality is enabled

Wake-On-LAN Address Byte 0

Wake-On-LAN Address Byte 0.

WOLAD0	Offset	Reset Value
Wake-On-LAN Address Byte 0	**1F.0783$_H$**	**0000$_H$**



Field	Bits	Type	Description
AD0	7:0	RW	**Address Byte 0** Defines byte 0 of the WOL-designated MAC address to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register **WOLAD0** defined above.

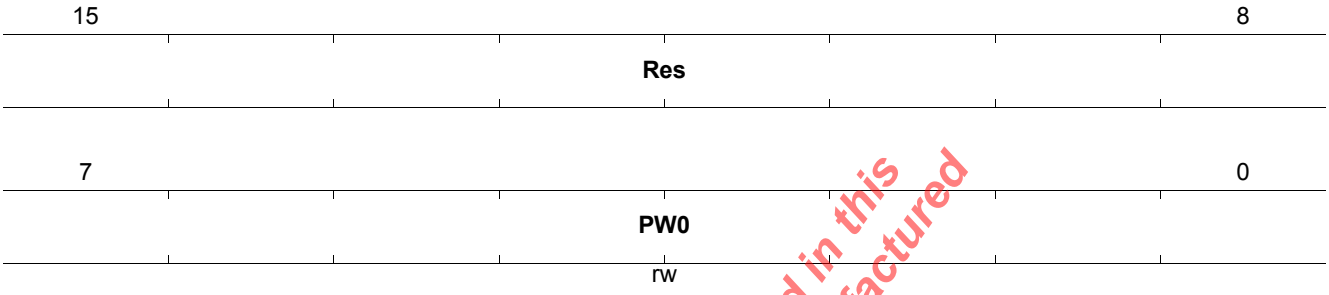
Table 73 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLAD1	Wake-On-LAN Address Byte 1	1F.0784$_H$	0000$_H$
WOLAD2	Wake-On-LAN Address Byte 2	1F.0785$_H$	0000$_H$
WOLAD3	Wake-On-LAN Address Byte 3	1F.0786$_H$	0000$_H$
WOLAD4	Wake-On-LAN Address Byte 4	1F.0787$_H$	0000$_H$
WOLAD5	Wake-On-LAN Address Byte 5	1F.0788$_H$	0000$_H$

Wake-On-LAN SecureON Password Byte 0

Wake-On-LAN SecureON Password Byte 0.

WOLPW0	Offset	Reset Value
Wake-On-LAN SecureON Password Byte 0	$1F.0789_H$	0000_H



Field	Bits	Type	Description
PW0	7:0	RW	**SecureON Password Byte 0** Defines byte 0 of the WOL-designated SecureON password to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register WOLPW0 defined above.

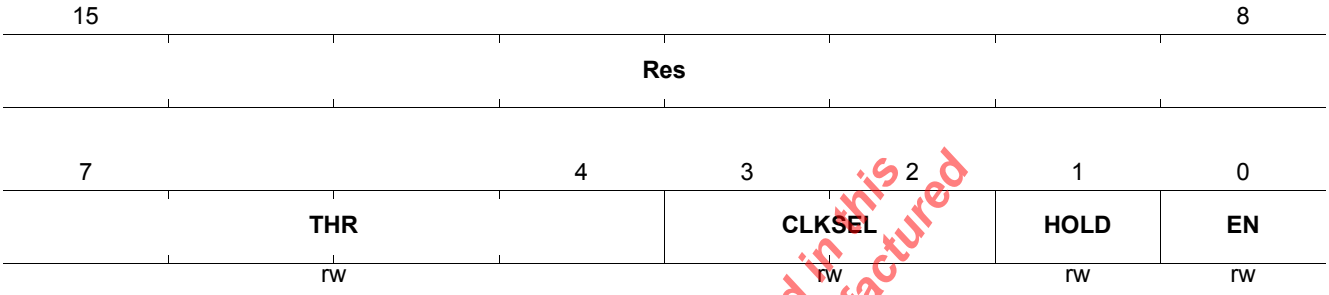
Table 74 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLPW1	Wake-On-LAN SecureON Password Byte 1	$1F.078A_H$	0000_H
WOLPW2	Wake-On-LAN SecureON Password Byte 2	$1F.078B_H$	0000_H
WOLPW3	Wake-On-LAN SecureON Password Byte 3	$1F.078C_H$	0000_H
WOLPW4	Wake-On-LAN SecureON Password Byte 4	$1F.078D_H$	0000_H
WOLPW5	Wake-On-LAN SecureON Password Byte 5	$1F.078E_H$	0000_H

Configuration for Synchronous Ethernet

This register allow management configuration of the SyncE clocking reference

PD_CTL	Offset	Reset Value
Configuration for Synchronous Ethernet	$1F.07FE_H$	0000_H



Field	Bits	Type	Description
THR	7:4	RW	**THR** Control the Threshold for detection of Lost of Reference clock.
CLKSEL	3:2	RW	**CLKSEL** This enable management selection of the type of reference clock we are receiving **Constants** 00_B **AN1** The Reference clock is 8 kHz. Special request for AN application 01_B **EEC1** The Reference clock is 2.048 MHz according to EEC-Option 1 10_B **EEC2** The Reference clock is 1.544 MHz according to EEC-Option 2 11_B **AN2** Reserved
HOLD	1	RW	**HOLD** Force the SyncE into HOLD over mode. This is the mode we enter when we detect Lost of reference. To hold the adapted Frequency so that we are able to sustain the reference clock generation within error of 4.6ppm. **Constants** 0_B **NORM** HW control of the entry/exit of Hold-Over mode 1_B **FHOLD** Force Hold Over mode
EN	0	RW	**EN** Enable Synchronous Ethernet Support **Constants** 0_B **DISABLE** Normal Ethernet operation 1_B **ENABLE** SyncE is enabled

5 Electrical Characteristics

This chapter defines the Electrical Characteristics to which the Intel® Ethernet Switch device conforms.

Note: This chapter is preliminary draft and subject to change.

5.1 Absolute Maximum Ratings

Table 75 shows the Absolute Maximum Ratings for Intel® Ethernet Switch.

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

Table 75 Absolute Limit Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature Limits	T_{STG}	-55.0	–	125.0	°C	–
Moisture Level 3 Temperature Limits	T_{ML3}	–	–	260.0	°C	According to IPS J-STD 020
DC Voltage Limits on VDDP Pins	V_{DDP}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDH Pins	V_{DDH}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDR Pins	V_{DDR}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDL Pins	V_{DDL}	-0.5	–	+1.26	V	–
DC Voltage Limits on VDD Pins	V_{DD}	-0.5	–	+1.26	V	–
DC Voltage Limits on any other pins[1] with respect to the ground	V_{DC}	-0.5	–	V_{DDx}+0.5	V	Unless specified otherwise
ESD HBM Robustness	$V_{ESD,HBM}$	–	–	1000.0	V	According to ANSI/ESDA/JEDEC JS-001-2014
ESD CDM Robustness	$V_{ESD,CDM}$	–	–	250.0	V	According to JEDEC JESD22-C101

1) This means any pin which is not a supply pin out of one of the domains: V_{DDP}, V_{DDA}, V_{DDH}, V_{DDR}, V_{DDL}, V_{DD}

5.2 Operating Range

Table 76 defines the limit values of voltages and temperature which may be applied to guarantee proper operation of the Intel® Ethernet Switch.

Table 76 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature under Bias	T_A	0	–	70.0	°C	–
Junction temperature	T_j	0	–	125.0	°C	–
Pad-Supply Voltage	V_{DDP}	3.13	3.30	3.47	V	3.3 V supply
High-Supply Voltage	V_{DDH}	3.13	3.30	3.47	V	3.3 V supply
RGMII PAD-Supply Voltage	V_{DDR}	3.13	3.30	3.47	V	3.3 V supply
		2.37	2.50	2.63	V	2.5 V supply
Low-Supply Voltage	V_{DDL}	1.05	1.10	1.15	V	1.1 V supply
Core-Supply Voltage	V_{DD}	1.05	1.10	1.15	V	1.1 V supply
Digital Input Voltage (Except RGMII Pins)	V_{ID}	-0.30	–	V_{DDP}+0.3	V	
Digital Input Voltage (RGMII Pins)	V_{ID}	0.00	–	V_{DDR}	V	
XTAL1 Input Voltage	V_{ID}	-0.30	–	V_{DDH}+0.3	V	AC Coupled
Ground	V_{SS}	0.00	0.00	0.00	V	–

5.3 Power Consumption

Table 77 Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MAX POWER CASE: 5-GPHY-ports 1G link+traffic, 100m cable; 2x RGMII traffic						
	I_{DDH}	–	300	330	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	480	530	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	780	830	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	7	10	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C
10m POWER CASE: 5-GPHY-ports 1G link+traffic, 10m cable; 2x RGMII traffic						
	I_{DDH}	–	300	330	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	460	450	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	690	750	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	7	10	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C
100BASE-T POWER CASE: 5-GPHY-ports 100 Mbps link+traffic, 100m cable; 2x RGMII traffic						
	I_{DDH}	–	115	125	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	210	230	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	220	260	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	7	10	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C
EEE NO-TRAFFIC POWER CASE: 5-GPHY-ports 1G link no-traffic, 2x RGMII IDLE						
	I_{DDH}	–	70	80	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	180	200	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	300	350	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	7	10	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C
NO-LINK POWER CASE: 5-GPHY-ports no-link+traffic, 2x RGMII IDLE						
	I_{DDH}	–	60	70	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	80	90	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	150	170	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	7	10	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C
RESET POWER CASE: 5-GPHY-ports Reset, 2x RGMII Reset						
	I_{DDH}	–	30	40	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	10	15	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	I_{DD}	–	15	25	mA	V_{DD} = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR}$	–	1	3	mA	$V_{DDP/DDR}$ = 3.3 V, T_A = 25 °C

5.4 DC Characteristics

The following sections investigate the DC characteristics of the Intel® Ethernet Switch external interfaces.

5.4.1 Digital Interfaces

This chapter defines the DC characteristics of the digital interfaces.

5.4.1.1 GPIO Interfaces

This chapter defines the DC characteristics of the GPIO Interface comprised of the following interfaces:

- MDIO
- SPI
- UART
- Interrupts
- Clock Outputs
- General Purpose IO
- LED
- JTAG

The DC characteristics for V_{DDP}=3.3 V are summarized in Table 78.

Table 78 DC Characteristics of the GPIO Interfaces (VDDP=3.3V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	0.7*V_{DDP}	–	V_{DDP}+0.3	V	–
Input Low Voltage	V_{IL}	-0.3	–	0.3*V_{DDP}	V	–
Output High Voltage	V_{OH}	V_{DDP}-0.4	–	–	V	I_{OH}= 2, 4, 8, 12 mA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL}= 2, 4, 8, 12 mA

5.4.1.2 GMII/RGMII Transmit Interfaces

This chapter defines the DC characteristics of the RGMII/GMII transmit Interfaces. The DC characteristics summarized in **Table 79** are valid for V_{DDR}=2.5 V and V_{DDR}=3.3 V.

Table 79 DC Characteristics of the Transmit RGMII/GMII Interfaces

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.1	–	V_{DDR}+0.3	V	5 pF
Output Low Voltage	V_{OL}	0	–	0.5	V	5 pF

5.4.1.3 GMII/RGMII Receive Interfaces

This chapter defines the DC characteristics of the RGMII/GMII receive Interfaces. The DC characteristics summarized in **Table 80** are valid for V_{DDR}=2.5 V and V_{DDR}=3.3 V.

Table 80 DC Characteristics of the Receive RGMII/GMII Interfaces

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.7	–	-	V	–
Input Low Voltage	V_{IL}	–	–	0.7	V	–

5.5 AC Characteristics

The following sections describe the AC characteristics of the external interfaces. The load capacitors are according to the specific interface standard. All non-specified interfaces use 30 pF as assumed loading.

5.5.1 Reset

Intel® Ethernet Switch supports an asynchronous hardware reset HRSTN. The timing requirements on the HRSTN pin to the are listed in **Table 81**. For better illustration the timings refer to the signal sequence waveforms depicted in **Figure 47**.

It is recommended that the voltage 3.3 V powers up before voltage 1.1 V. Voltage 1.1 V must never be higher than voltage 3.3 V ramp. Voltage 1.1 V must power up within t_{up} after 3.3 V powers up. After the power-supply settling time all primary input signals to the GSW150 should be defined. In particular this is valid for the device reset HRSTN. This reset must be held for a t_{reset} time. After releasing the reset the integrated PLL locks on the reference clock and the device boots up.

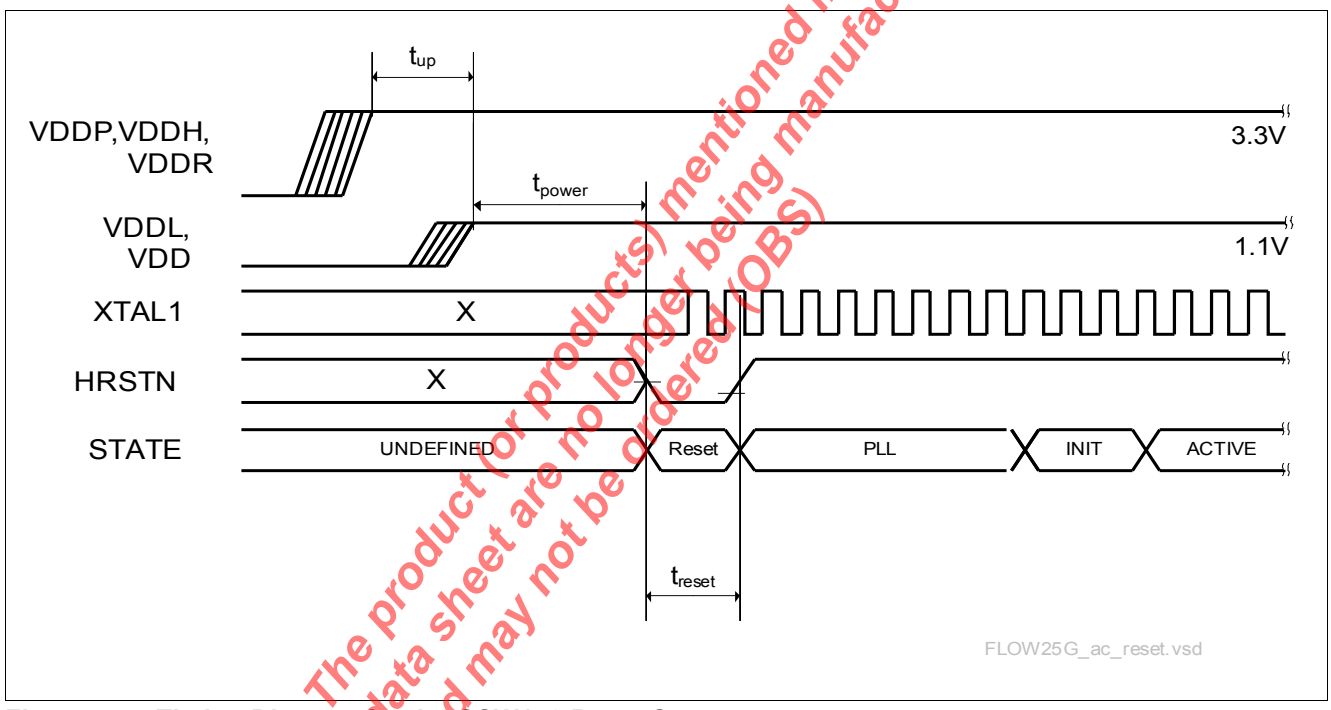


Figure 47 Timing Diagram for the GSW150 Reset Sequence

Table 81 AC Characteristics of the HRSTN pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply Sequence Time	t_{up}	–	–	100.0	ms	–
Power Supply Settling Time	t_{power}	–	–	50.0	ms	–
Reset Time	t_{reset}	200.0	–	–	ms	–

5.5.2 Power Supply

Table 82 lists the AC characteristics of the power supplies.

Table 82 AC Characteristics of the Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply Ripple on VDDL	R_{VDDL}	–	–	30.0	mV	Peak-Value
Power Supply Ripple on VDD	R_{VDD}	–	–	30.0	mV	Peak-Value
Power Supply Ripple on VDDP	R_{VDDP}	–	–	100.0	mV	Peak-Value
Power Supply Ripple on VDDH	R_{VDDH}	–	–	30.0	mV	Peak-Value
Power Supply Ripple on VDDR	R_{VDDR}	–	–	100.0	mV	Peak-Value

5.5.3 Input Clock

Table 83 list the input clock requirements when not using a crystal, i.e. when an external reference clock is injected into the XTAL1 pin of the Intel® Ethernet Switch, e.g. nominal frequency, frequency deviation, duty cycle and signal characteristics. If a crystal is applied to generate the reference clock using the integrated XO the clock requirements stated here are explicitly met as long as the specification for the crystal is satisfied.

Table 83 AC Characteristics of Input Clock on XTAL1 pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz input	f_{clk25}	–	25.0	–	MHz	–
Frequency with 40 MHz input	f_{clk40}	–	40.0	–	MHz	–
Frequency Deviation		-50.0	–	+50.0	ppm	–
Duty Cycle		45.0	50.0	55.0	%	–
XTAL1 Input Swing		0.9	-	V_{DDH}	V	–
Rise/Fall-Times		–	–	2.0	ns	-

5.5.4 GPC Output Clock

Table 84 list the output clock requirements on the GPC pin from the Intel® Ethernet Switch, e.g. nominal frequency, frequency deviation, duty cycle and signal characteristics.

Table 84 AC Characteristics of Output Clock on GPC pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Deviation		-50.0	–	+50.0	ppm	–
Duty Cycle		45.0	50.0	55.0	%	–
Rise/Fall-Times		–	–	2.0	ns	10 pF load

5.5.5 MDIO Interface

Figure 48 shows a timing diagram of the MDIO interface for a clock cycle in the read-, write- and turnaround-modus, respectively. The timing measures are annotated. The defined absolute values are summarized in Table 85.

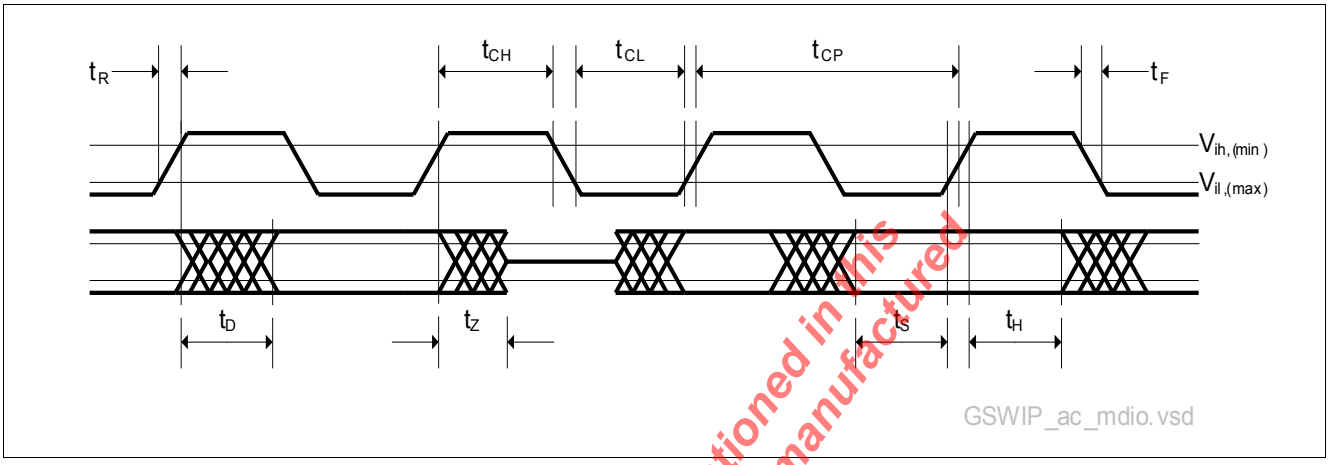


Figure 48 Timing Diagram for the MDIO Interface

Table 85 Timing Characteristics of the MDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC high time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the Gigabit Ethernet Switch.
MDC low time	t_{CL}	10.0	–	–	ns	
MDC clock period	t_{CP}	40	400.0	–	ns	
MDC clock frequency[1)]	t_{CP}	–	2.5	25.0	MHz	
MDC rise time	t_R	–	–	5.0	ns	
MDC fall time	t_F	–	–	5.0	ns	
MDIO Input Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	Gigabit Ethernet Switch Receive
MDIO Input Hold Time subject to ↑ MDC	t_H	0.0	–	–	ns	Gigabit Ethernet Switch Receive
MDIO Output Delay subject to ↑ MDC	t_D	10.0	–	t_{CP}-10	ns	Gigabit Ethernet Switch Transmit
Standard @2.5 MHz						
MDIO Output Delay subject to ↑ MDC	t_D	0.0	–	300.0	ns	PHY transmit
MDIO Output Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	MAC transmit
MDIO Output Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	MAC transmit

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

5.5.6 SMDIO Interface

Figure 49 shows a timing diagram of the SMDIO interface for a clock cycle in the read-, write- and turnaround-modus, respectively. The timing measures are annotated. The defined absolute values are summarized in Table 86.

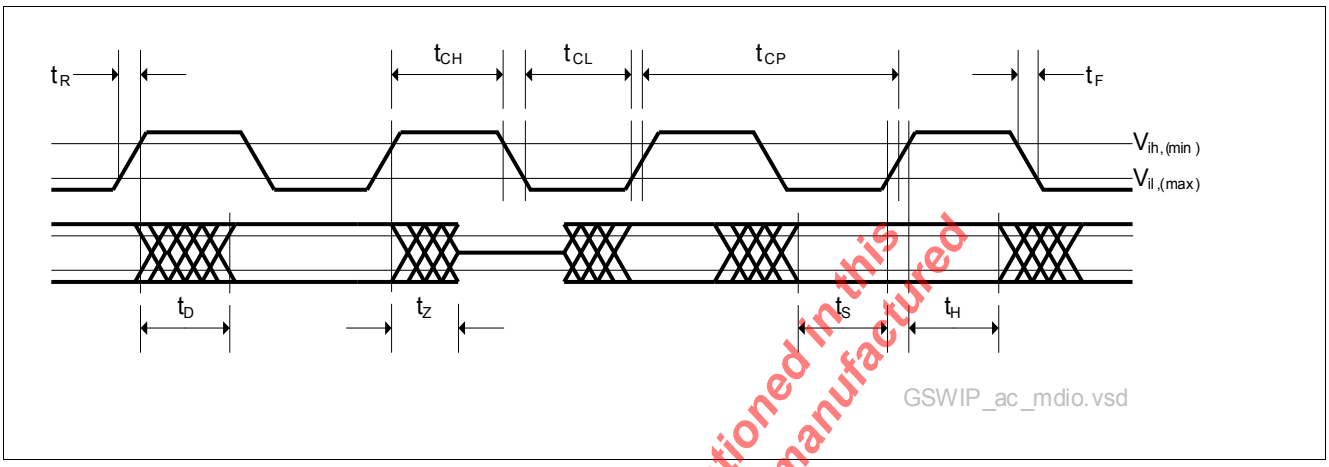


Figure 49 Timing Diagram for the SMDIO Interface

Table 86 Timing Characteristics of the SMDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC high time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the Gigabit Ethernet Switch.
MDC low time	t_{CL}	10.0	–	–	ns	
MDC clock period	t_{CP}	40.0	400.0	–	ns	
MDC clock frequency[1)]	t_{CP}	–	2.5	25.0	MHz	
MDC rise time	t_R	–	–	5.0	ns	
MDC fall time	t_F	–	–	5.0	ns	
MDIO Input Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	Gigabit Ethernet Switch Receive
MDIO Input Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	Gigabit Ethernet Switch Receive
MDIO Output Delay Time subject to ↑ MDC	t_D	0.0	–	10	ns	Gigabit Ethernet Switch Transmit
Standard @2.5 MHz						
MDIO Output Delay subject to ↑ MDC	t_D	0.0	–	300.0	ns	PHY transmit
MDIO Output Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	MAC transmit
MDIO Output Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	MAC transmit

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

5.5.7 GMII/RGMII Interface Timing Characteristics

The following sections investigate the timing characteristics of the xMII interfaces.

5.5.7.1 GMII Interface Mode

This section investigates the timing characteristics of the GMII interface at the Gigabit Ethernet Switch. This interface is conform to the GMII specification as defined in IEEE802.3-2005 clause 35. The Standard Requirements are exceeded wherever applicable.

Transmit Timing Characteristics

Figure 50 shows the timing diagram of the transmit GMII interface at the Gigabit Ethernet Switch. It is referred by Table 87 which characterize the timing requirements for 1000 Mbps.

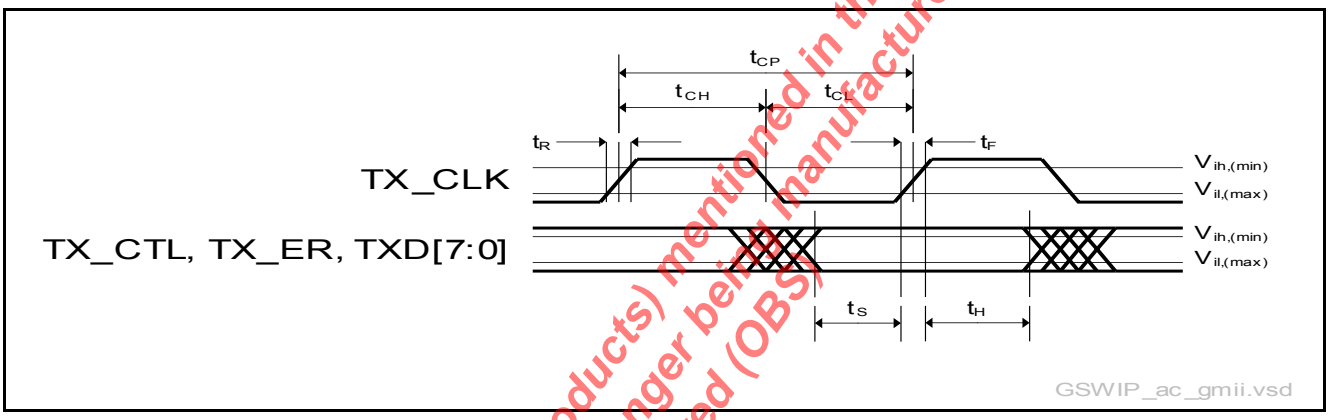


Figure 50 Transmit Timing Diagram of the GMII

Table 87 Transmit Timing Characteristics of the GMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit Clock Frequency (TX_CLK)	f_{TX_CLK}	125.0-100ppm	125.0	125.0+100ppm	MHz	Long Term Average Frequency
Transmit Clock Period (TX_CLK)	t_{CP}	7.5	8.0	8.5	ns	Measured according to IEEE802.3 clause 35.4.1
Transmit Clock High Time (TX_CLK)	t_{CH}	2.5	4.0	5.5	ns	
Transmit Clock Low Time (TX_CLK)	t_{CL}	2.5	4.0	5.5	ns	
Transmit Clock Rise Time (TX_CLK)	t_R	–	–	1.0	ns	
Transmit Clock Fall Time (TX_CLK)	t_F	–	–	1.0	ns	
Setup time subject to ↑ TX_CLK	t_S	2.5	–	–	ns	
Hold time subject to ↑ TX_CLK	t_H	0.5	–	–	ns	
Standard						
Setup time subject to ↑ TX_CLK	t_S	2.5	–	–	ns	
Hold time subject to ↑ TX_CLK	t_H	0.5	–	–	ns	

Receive Timing Characteristics

Figure 51 shows the timing diagram of the receive GMII interface at the Gigabit Ethernet Switch. It is referred by Table 88 which characterize the timing requirements.

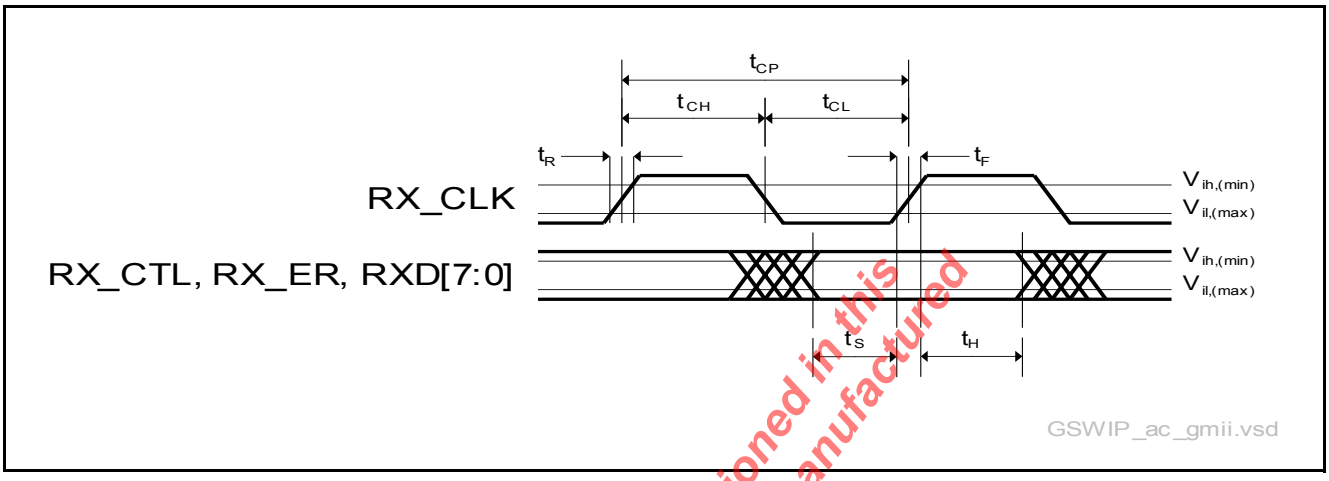


Figure 51 Receive Timing Diagram of the GMII

Table 88 Receive Timing Characteristics of the GMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive Clock Period (RX_CLK)	t_{CP}	7.5	8.0	8.5	ns	Measured according to IEEE802.3 clause 35.4.1
Receive Clock High Time (RX_CLK)	t_{CH}	3.5	4.0	4.5	ns	
Receive Clock Low Time (RX_CLK)	t_{CL}	3.5	4.0	4.5	ns	
Receive Clock Rise Time (RX_CLK)	t_R	–	–	1.0	ns	
Receive Clock Fall Time (RX_CLK)	t_F	–	–	1.0	ns	
Setup time subject to ↑ RX_CLK	t_S	2.0	–	–	ns	
Hold time subject to ↑ RX_CLK	t_H	0.2[1)]	–	–	ns	
Standard						
Setup time subject to ↑ RX_CLK	t_S	2.0	–	–	ns	
Hold time subject to ↑ RX_CLK	t_H	0.0	–	–	ns	

1) This hold time violates the standard. According to standard, hold time shall be 0ns.

5.5.7.2 RGMII Interface

This section investigates the timing characteristics of the RGMII interface at the Gigabit Ethernet Switch. Unless no HSTL voltages are supported this interface is conform to the RGMII specification v1.3 and v2.0. The RGMII interface can operate at speeds of 10 Mbps, 100 Mbps and 1000 Mbps.

Timing Characteristics

Figure 52 shows the timing diagram of the RGMII interface at the Gigabit Ethernet Switch. It is referred by Table 89 which characterize the timing requirements. Note that the setup and hold times are subject to the internal version of the TX_CLK/RX_CLK which is the external clock delayed by the integrated delay which is adjustable in steps of 0.5ns via PCDU register configuration. If the integrated delay is not used, e.g. because its implemented externally by PCB wire delays, it must be set to zero in which case all the timings are related directly to the TX_CLK/RX_CLK at the pin.

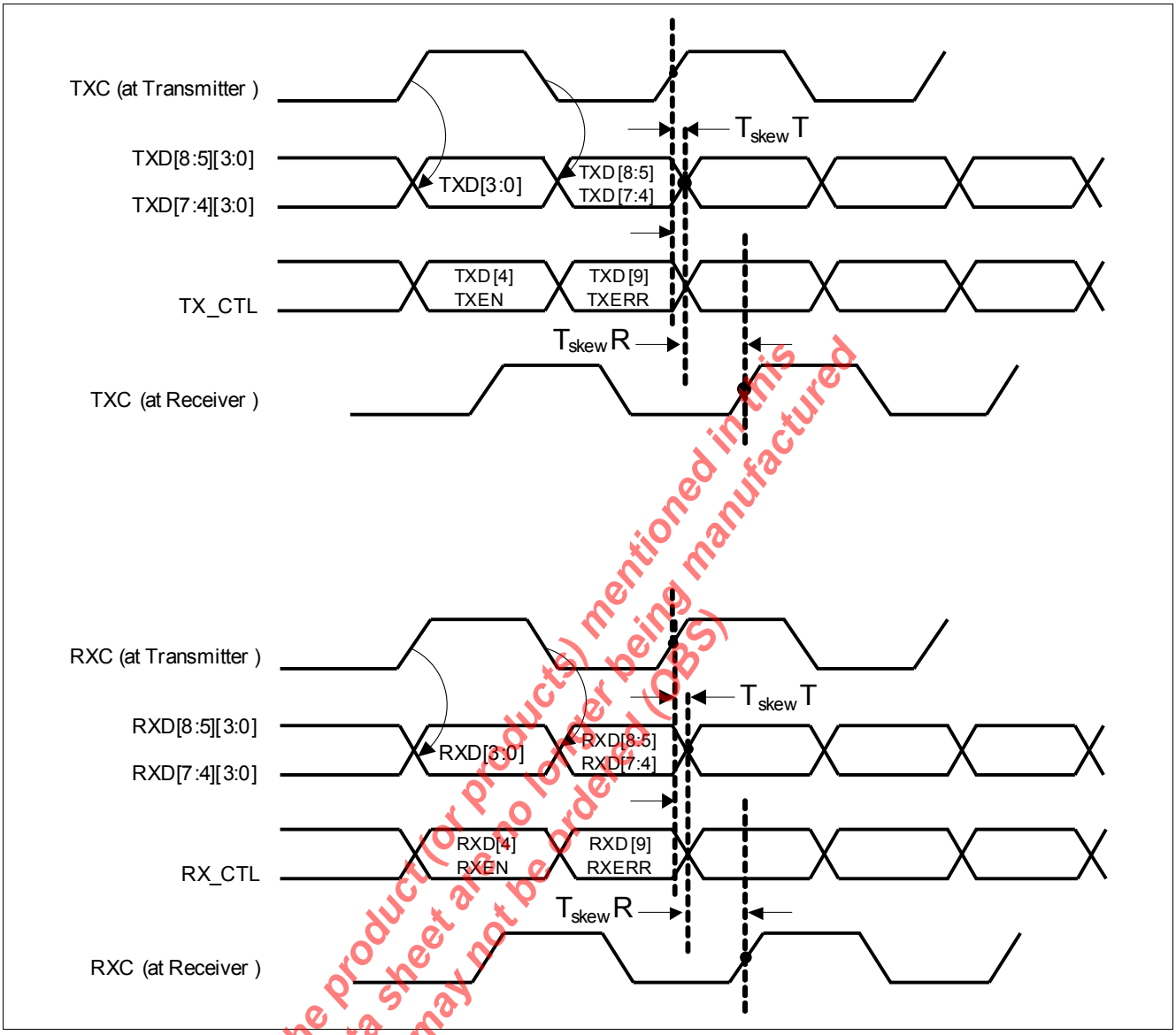


Figure 52 Timing Diagram of the RGMII

Table 89 Timing Characteristics of the RGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock Frequency (RX_CLK/TX_CLK)	f_{CLK}	-50ppm	125.0	+ 50ppm	MHz	For 1000 Mbps speed.
		-50ppm	25.0	+ 50ppm	MHz	For 100 Mbps speed.
		-50ppm	2.5	+ 50ppm	MHz	For 10 Mbps speed.
Clock Period (RX_CLK/TX_CLK)	t_{CP}	7.2	8.0	8.8	ns	For 1000 Mbps speed.
		36.0	40.0	44.0	ns	For 100 Mbps speed.
		360.0	400.0	440.0	ns	For 10 Mbps speed.
Duty Cycle[1)]	t_H/t_{CP}, t_L/t_{CP}	45.0	50.0	55.0	%	Speed Independent
Clock Rise Time (RX_CLK/TX_CLK)	t_R	–	–	750.0	ps	20%→80%
Clock Fall Time (RX_CLK/TX_CLK)	t_F	–	–	750.0	ps	80%→20%
Clock to Data Skew at Transmitter	t_{SkewT}	-0.5	0.0	0.5	ns	
Clock to Data Skew at Receiver	t_{SkewR}	1	1.8	2.6	ns	
Integrated Receive Clock Delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via registers

1) Duty Cycle may be stretched/shrunk during speed changes. Such an even last no longer than three t_{CP} at lowest speed.

5.5.8 Test Interface

The Test interface is used for boundary scan.

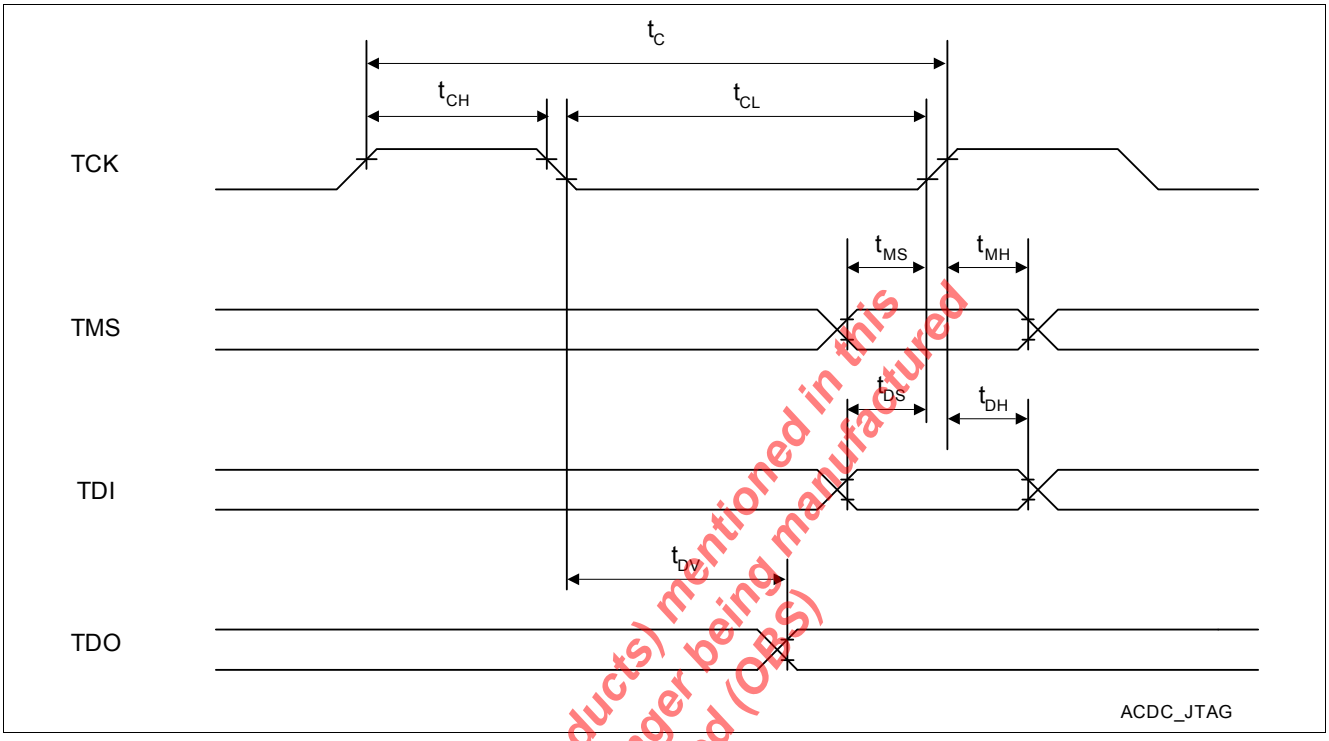


Figure 53 Test Interface Timing

The timing values are described in Table 90 and Table 91.

Table 90 Test Interface Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_C	100	–	–	ns	–
TCK High Time	t_{CH}	40	–	–	ns	–
TCK Low Time	t_{CL}	40	–	–	ns	–

Table 91 JTAG Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS setup time	t_{MS}	40	–	–	ns	–
TMS hold time	t_{MH}	40	–	–	ns	–
TDI setup time	t_{DS}	40	–	–	ns	–
TDI hold time	t_{DH}	40	–	–	ns	–
Hold: $\overline{\text{TRST}}$ after TCK	t_{HD}	10	–	–	ns	–
TDO valid delay	t_{DV}	–	–	60	ns	–

5.5.9 Crystal Specification

In the reference design, the crystal is attached to the Intel® Ethernet Switch SoC and must follow the specification in Table 92.

Table 92 Specification of the Crystal

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz input	f_{clk25}	–	25.0	–	MHz	–
Frequency with 40 MHz input	f_{clk40}	–	40.0	–	MHz	–
Total Frequency Stability	–	-50	–	+50	ppm	Refer to sum of all effects: eg. general tolerance, aging, temperature dependency
Series Resonant Resistance	–	–	–	40	Ω	–
Drive Level	–	0.08	0.10	0.2	mW	–
Load Capacitance	C_L	16	-	30	pF	–
Shunt Capacitance	C_0	–	-	7	pF	–

6 Package Outline

The product is assembled in PG-MRQFN-134-C-1A package which complies with regulations requiring lead free material.

Table 93 JEDEC Thermal Resistance Package Parameter

Item	Description/Value
Package Type	PG-MRQFN-134-C-1A
Thermal Resistance Junction to Ambient (Reference to JEDEC JESD51-2)	$R_{th,\ JA}$ = 20.6 K/W Psi-JCTop = 0.61 K/W Psi-JB = 8.6 K/W
Thermal Resistance Junction to Case (Reference to JEDEC JESD15-3)	$R_{th,\ JCtop}$ = 17.2 K/W
	$R_{th,\ JCbot}$ = 11.9 K/W

Note: The above values are based on JEDEC standard thermal simulation condition.

Package outline and dimensions are shown in **Figure 54** and **Figure 55**.

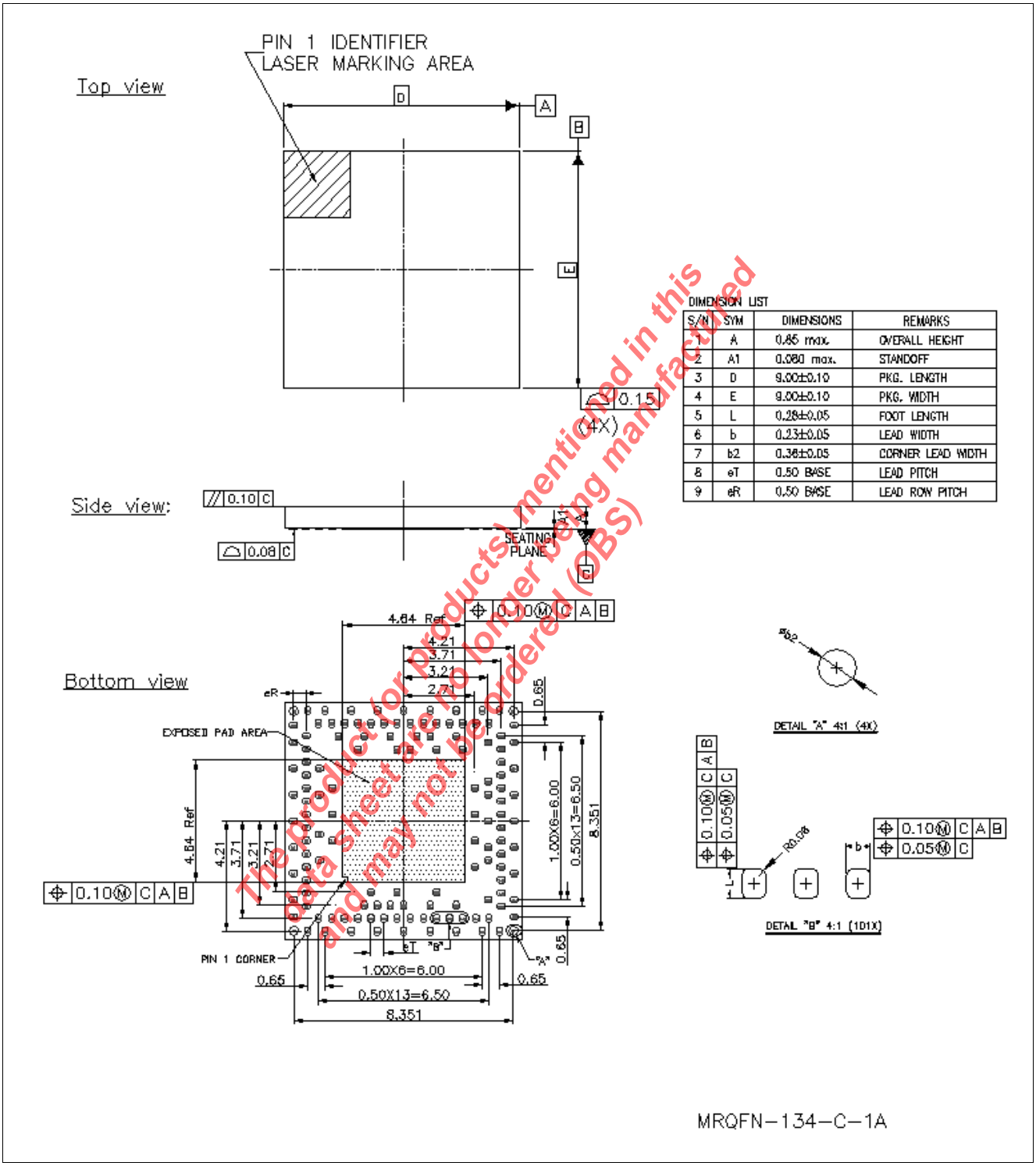


Figure 54 PG-MRQFN-134-C-1A 9 mm x 9 mm Package Outline

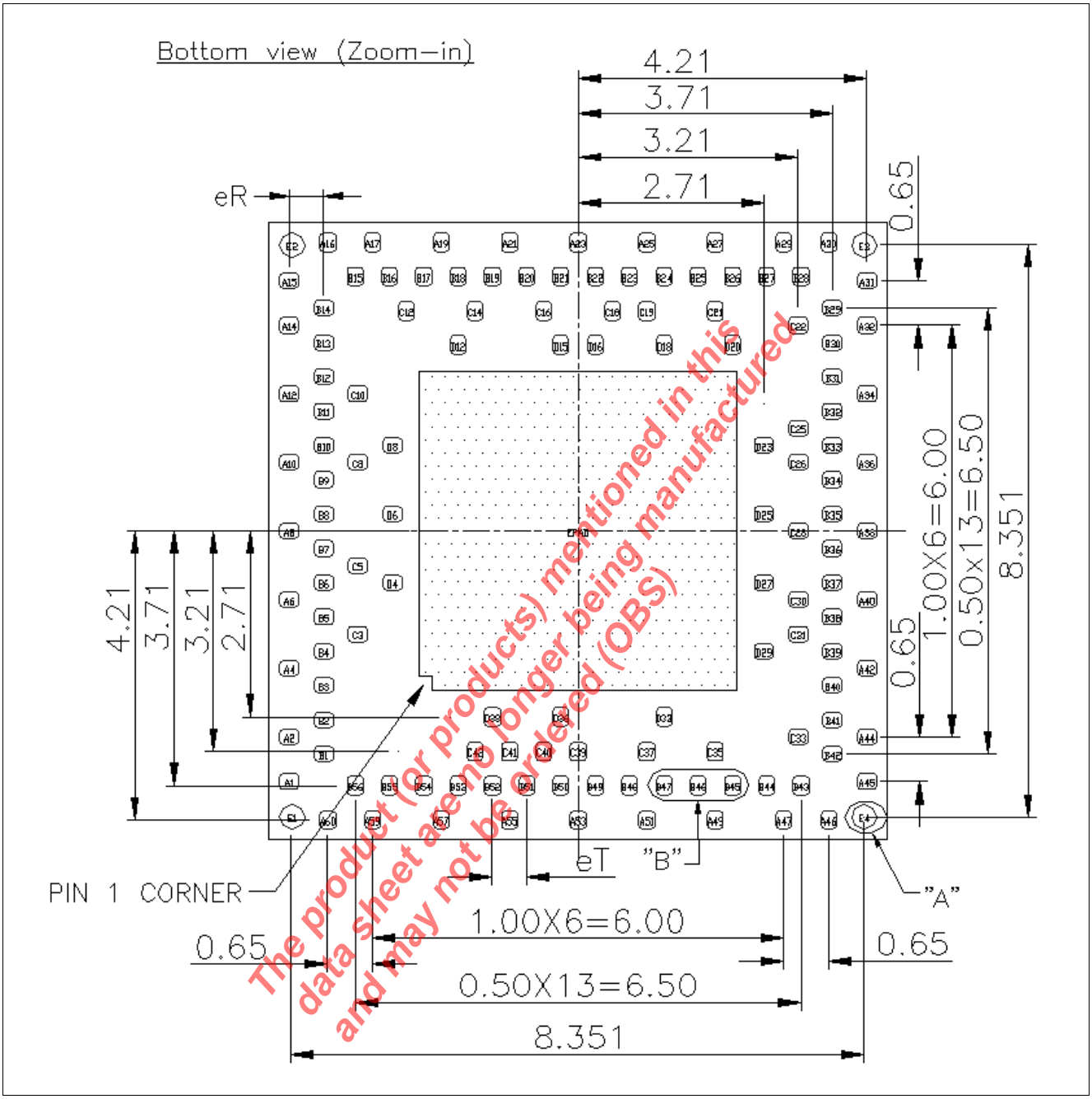


Figure 55 PG-MRQFN-134-C-1A 9 mm x 9 mm Package Outline - Bottom View

6.1 Chip Identification and Ordering Information

Figure 56 shows the marking pattern on the Intel® Ethernet Switch (GSW150) device.

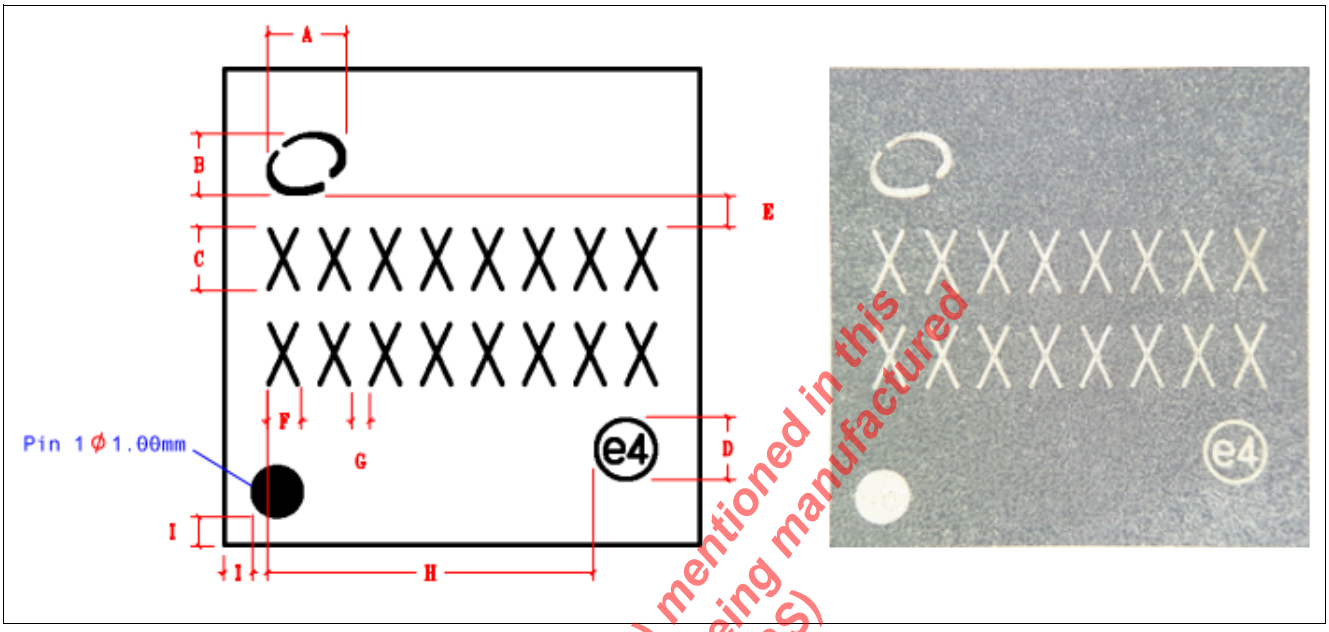


Figure 56 Chip Marking of GSW150

Table 94 explains the chip marking information and Table 95 provides sales ordering information.

Table 94 Chip Marking Pattern

Marking	Description
Text Line 1 (Logo)	Intel - Swirl
Text Line 2 (FPO#)	<acc. to assembly lot marking instruction>
Text Line 3 (S-Spec#)	See Table 95
Text Line 4 (Pb-free symbol)	e4

Table 95 Product Naming

Product Name	Former Lantiq Sales Code	Ordering Code	S-Spec#
GSW150	PEB 7084 M V1.1	PEB7084MV11	SLLVE
GSW150	PEB 7084 M V1.2	PEB7084MV12	SLLW4