** PRELIMINARY **

MxL93642 and MxL93643

Product Brief

400G PAM4 DSP SoC

General Description

The MxL9364x is a highly integrated PAM4 DSP SoC that enables 400Gbps optical interconnects using 100Gbps over a single optical wavelength (100G/λ).

The device has a high-speed electrical interface with eight transmit (Tx) and receive (Rx) input/output (I/O) that connect electrically through a module connector to the host ASIC. The device also has a high-speed optical side interface that has four Tx and Rx I/O connecting through the optical components to optical fibers.

The electrical interface supports 106.25Gbps PAM4 signaling per lane over C2M host channels.
The optical interface supports 106.25Gbps PAM4 signaling per wavelength for DR, FR, and LR applications.

The device supports DSP functions including Line-side Tx digital pre-distortion (DPD), transmit pre-emphasis (TX FIR), receiver feed forward equalization (FFE) and decision feedback equalization (DFE).

The MxL9364x, in a 12mm × 12mm package, includes integrated TOSA drivers with differential and single ended options for both SiPh and EML implementations. It offers exceptional signal integrity for 112G signals in a compact footprint suitable for next generation optical module form-factors such as QSFP-DD and OSFP.

Applications

- QSFP-DD optical modules
- QSFP optical modules
- OSFP optical modules

Features

- 400G capacity that enables 400G DR4, FR4, LR4.
- 400G to 100G break-out mode
- Tx equalization includes pre-emphasis, digital predistortion, and reflection cancellation
- Rx equalization includes CTLE, multi-tap FFE and DFE, and reflection cancellation
- Integrated crystal oscillator eliminates the need for a costly reference clock source
- Small package size to enable the QSFP-DD space requirements
- BER monitoring
- SNR/Histogram reporting for each receiver on both electrical and optical interfaces
- Diagnostic loop-back and test pattern generation and error checking
- SPI and I^2C slave interface to communicate to module MCU
- SPI master for flash memory interface
- I^2C master interface for TIA direct control
- Embedded CPU for real-time control
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected

Supported Standards

- OIF-CEI-56G-VSR-PAM4, OIF-CEI-112G-VSR-PAM4
- IEEE Std 802.3bs, 802.3cd, P802.3ck, P802.3cu

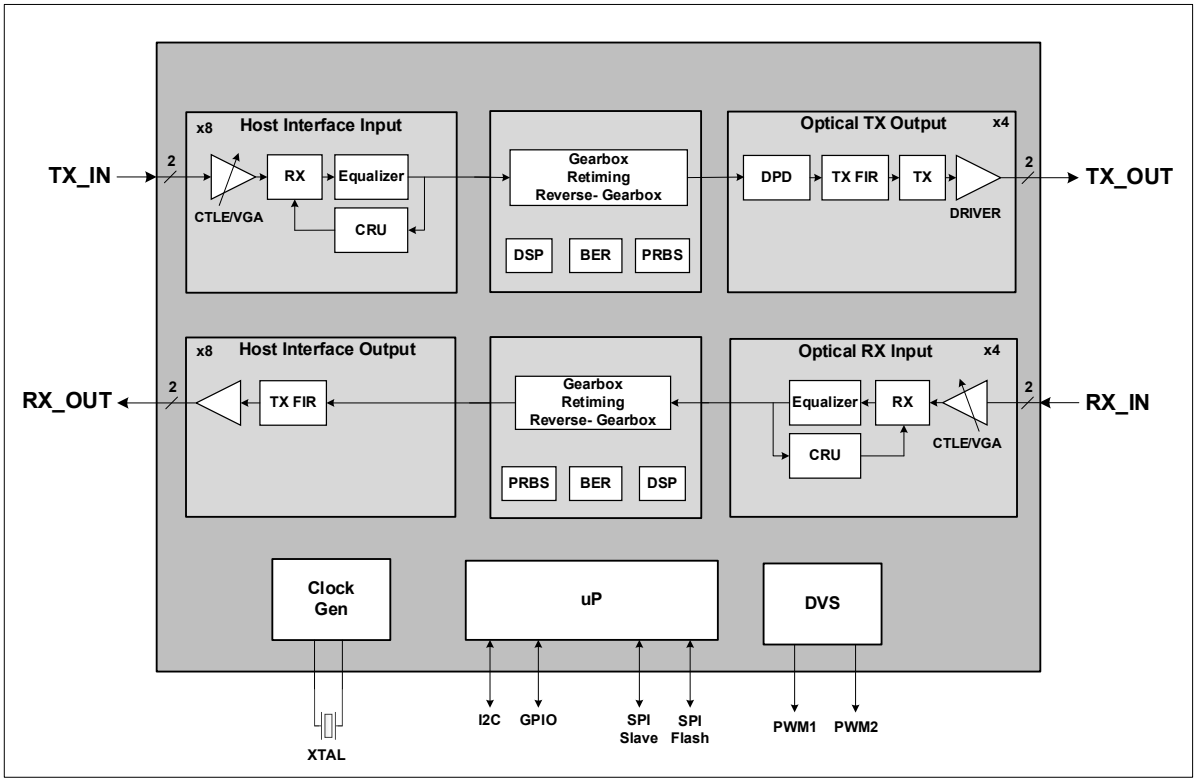

Figure 1: MxL9364x Simplified Block Diagram

Ordering Information

Marketing Part Number	Ordering Part Number	Description	Package	Shipping
MxL93642	MxL93642-AP-T	400G DSP with integrated driver	FCFBGA 12mm x 12mm	Tray
MxL93643	MxL93643-AP-T	400G DSP without integrated driver		

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