



Integrated Quad RF Transceiver with Single Feedback Receiver

General Description

The MxL1600 is a family of highly integrated and low power consumption multi-port radio frequency (RF) transceivers for wireless infrastructure radios. Their powerful combination of high integration, ultra-low power dissipation, high performance, and software-defined programmability make them optimal solutions for 2G, 3G, 4G, and 5G macro, massive Multiple-Input/Multiple-Output (MIMO), and small cell radio platforms.

The MxL1600 family integrates four transmitters (Tx), four receivers (Rx), and up to two feedback receivers (FBRX). They are tunable to operate over a frequency range from 380 to 6000 MHz. Each Rx is configurable to support wide signal bandwidths of up to 400 MHz. Each Tx and FBRX is configurable to support wider signal bandwidths up to 850 MHz to facilitate digital pre-distortion algorithms.

The MxL1600 series software defined bandwidth and tuning flexibility is power-efficiently delivered using a direct conversion RF architecture. This architecture is underpinned by integrated digital radio processing functions and low-noise, on-chip local oscillators (LO). An optional external Rx LO input is available when supporting Multi-RAT GSM.

The MxL1600 supports a JESD204 system interface, programmable to operate in either JESD204B or JESD204C mode with lane rates up to 32Gbps.

The MxL1600 has an embedded microcontroller subsystem that simplifies configuration, calibration, and management of the device.

The MxL1600 family are pin and software compatible with the MxL1500 series. Users can alternatively choose the MxL1500 for radios which do not support multi-RAT GSM.

Applications

- 2G/3G/4G/5G Macro-cell radios
- Massive MIMO radios
- Small cell radios
- Distributed Antenna Systems (DAS)
- Repeaters

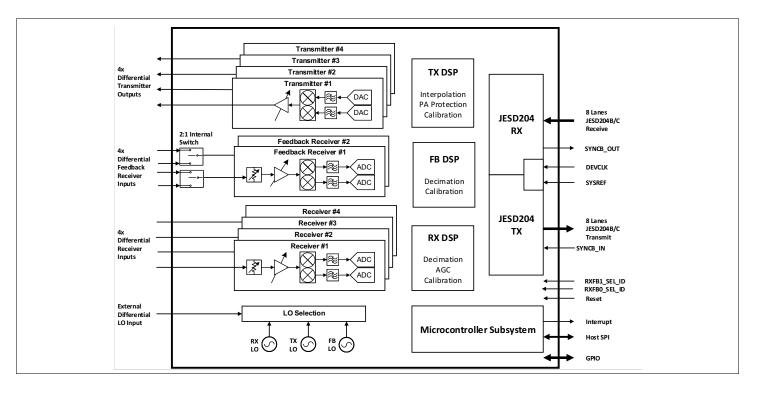
Features

- Four transmitters
- Four receivers
- Up to two feedback receivers
- Integrated dual-input RF switches per FBRX
- RF range from 380 to 6000 MHz
- Rx bandwidth up to 400 MHz
- Tx/FBRX synthesis bandwidth over 850 MHz
- 2G/3G/4G/5G air interface support
- External LO input for multi-RAT GSM mode
- FDD and TDD operation
- Ultra-low power consumption
- Fast power-up and power-down modes
- Deep sleep power saving modes
- Tx power amplifier protection
- Rx gain control
- IQ Imbalance and LO feed-through correction
- JESD204B or JESD204C system interface
- Up to 8 JESD204 TX lanes
- Up to 8 JESD204 RX lanes
- Embedded CPU for control, calibration, and status reporting
- SPI control interface
- GPIO for fast control and status reporting
- JTAG boundary scan including support for AC-coupled differential SERDES interfaces
- 1.8V, 1.2V, 0.8V, and 0.76V power supplies
- 15 x 15 mm, 324 balls, 0.8 mm pitch FCBGA package with exposed die

Supported Standards

- 3GPP Single RAT UTRA and E-UTRA
- 3GPP Multi-RAT GSM, UTRA and E-UTRA
- 3GPP 5G NR Standard
- JEDEC JESD204B, Subclasses 0 and 1
- JEDEC JESD204C, Subclasses 0 and 1
- JTAG IEEE1149.1 and IEEE1149.6

Block Diagram



Ordering Information

Table 1: Ordering Information

Marketing Part Number	Ordering Part Number	Package	Shipping
MxL1600	MxL1600-AS-T	FCBGA	Tray



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