MxL83433 and MxL83434

32Mbps Quad RS-485/422 Receiver with High IEC ESD and EFT

Data Sheet

General Description

The MxL83433 and MxL83434 are a family of monolithic quadruple differential line RS-485/RS-422 receivers that support communication up to 32Mbps in harsh industrial environments. The bus pins tolerate IEC electrical fast transients (EFT), IEC electrostatic discharge (ESD), offer a wide input voltage range, and input hysteresis.

Guaranteed low propagation delays and channel-to-channel and part-to-part propagation delay skews ensure maximum system performance.

A wide range of product options offers designers optimized solutions for their system. The eight product offerings include two package options, two temperature options, and two enable configurations to choose from. These options coupled with wide power supply range support (from 3.3V to 5V) provide a versatile portfolio that you can use in applications ranging from high-speed motor drives to wireless infrastructure and building automation. The integration of four receiver channels into compact TSSOP or NSOIC packages makes these products well suited for space-constrained enclosures that require robust, high-performance communication.

The MxL83433 device offers global enable pins, which allow all four channels to be enabled or disabled simultaneously. The MxL83434 device provide paired enable pins, allowing for the flexibility to control two channels at a time. Industry standard footprint and pinout ensure seamless compatibility for existing designs.

Features

- Meets or exceeds the requirements of the *TIA/EIA-485A* and *EIA/TIA-422B* standards
- Supply voltage from 3.3V to 5V
- Extended operating temperature range from –40°C to 125°C
- Extended operation common-mode range of ±15V
- Fail-safe open receiver (Rx) inputs
- 1/4 unit load (128 bus nodes)
- Available in global or paired enable configurations
- High-data rates up to 32Mbps
- Glitch-free power-up/power-down for hot swap capability
- Low channel-to-channel propagation delay skew
- Robust system protection:
  - ±4kV EFT (*IEC 61000-4-4*)
  - ±12kV ESD Contact (*IEC 61000-4-2*)
  - ±15kV ESD Human Body Model

Applications

- Industrial and process control equipment
- Level translators
- Telecommunication equipment
- High-performance motor drives
- Smart Grid
- Industrial transport

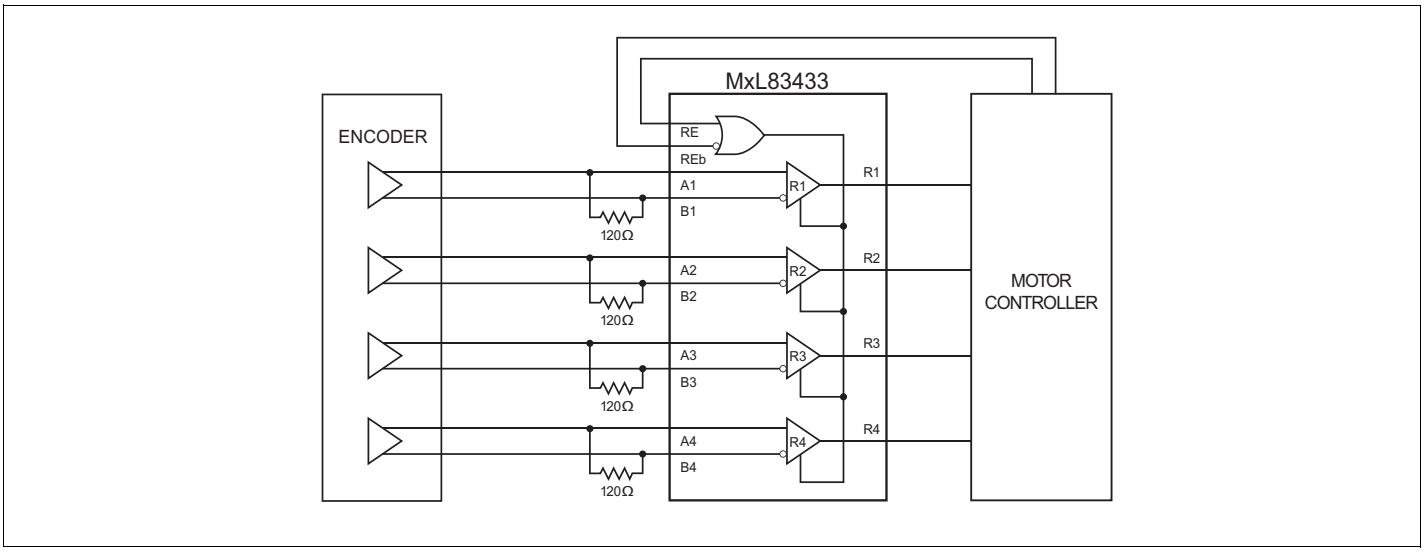


Figure 1: Typical Application Schematic

Revision History

Document No.	Release Date	Change Description
275DSR01	June 26, 2024	Initial final release.

Table of Contents

List of Figures

List of Tables

Specifications

Absolute Maximum Ratings

Important: Stresses beyond absolute maximum ratings listed in Table 1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply Voltage (V_{CC})	–0.3	6	V
Control Input Voltage (RE, REb, RE12, RE34)	–0.3	V_{CC} + 0.3	V
Receiver Input Voltage (AX, BX)	–25	25	V
Receiver Output Voltage (RX)	–0.3	V_{CC} + 0.3	V
Receiver Output Short-Circuit Current	–40	40	mA
Maximum Storage Temperature	–65	150	°C

ESD and EFT Ratings

Table 2: ESD and EFT Ratings

Parameter	Limit	Units
HBM - Human Body Model (pins AX and BX)	±15	kV
IEC 61000-4-2 Airgap Discharge (pins AX and BX)	±16	kV
IEC 61000-4-2 Contact Discharge (pins AX and BX)	±12	kV
IEC 61000-4-4 Electrical Fast Transient (pins AX and BX)	±4	kV

Thermal Information

Table 3: Thermal Information

Symbol	Thermal Metric	NSOIC16	TSSOP16	Units
θ_{JA}	Junction-to-Ambient Thermal Resistance	60.10	85.38	°C/W
Ψ_{JT}	Thermal Metric	3.56	1.60	°C/W
Ψ_{JB}	Junction-to-Board, at Tab	41.13	58.77	°C/W
θ_{JB}	Junction-to-Board	42.46	59.94	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	29.32	32.01	°C/W

Note: JESD51-5 (4-Layer) PCB.

Table 4: Power Dissipation

Parameter	Description	Minimum	Typical		Maximum	Unit
			MxL83433	MxL83434		
PD	All receivers—DISABLE (RE = 0V, REb = V_{CC} for MxL83433) (RE12 = RE34 = 0V for MxL83434) V_{CC} = 5.5V, T_A = 125C, 50% duty cycle square wave at 32Mbps with $\|V_{ID}\|$ = 3V.	-	17.5	18	-	mW
	All receivers—ENABLE (RE = V_{CC}, REb = 0V for MxL83433) (RE12 = RE34 = V_{CC} for MxL83434) V_{CC} = 5.5V, T_A = 125C, 50% duty cycle square wave at 32Mbps with $\|V_{ID}\|$ = 3V.	-	82	80	-	mW

Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Supply Voltage	3.0	5.5	V
V_{IH}	High Level Input Voltage (RE, REb, RE12, RE34)	2.0	-	V
V_{IL}	Low Level Input Voltage (RE, REb, RE12, RE34)	-	0.8	V
V_{CM}	Extended Operational Common-Mode Input Voltage (V_{CC} = 4.5 – 5.5V)	–15	15	V
V_{CM}	Extended Operational Common-Mode Input Voltage (V_{CC} = 3.0 – 5.5V)	–7	12	V

Electrical Characteristics

Unless otherwise noted, VCC = 3V to 5.5V, ambient temperature $T_{MIN} < T_A < TM_{AX}$. Typical values are at V_{CC} = 3.3V, ambient temperature T_A = 25°C. The specifications apply over the full operating range from –40°C to 125°C unless otherwise noted.

Table 6: Receiver DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_I	Receiver Input Current (AX, BX)	V_{CC} = 0 or 5.5V, V_I = 12V	-	140	250	µA
		V_{CC} = 0 or 5.5V, V_I = –7V	–200	115	-	µA
		V_{CC} = 0 or 5.5V, V_I = 15V	-	200	300	µA
		V_{CC} = 0 or 5.5V, V_I = –15V	–350	220	-	µA
R_{IN}	Receiver Input Resistance	–15V ≤ $V_{A/B}$ ≤ 15V, ΔV/ΔI, power on or off	48	-	-	kΩ
V_{TH+}	Receiver Positive-going Input Threshold	For 3V ≤ V_{CC} ≤ 5.5V: Over common-mode range from –7V to 12V	-	-	0.2	V
		For 4.5V ≤ V_{CC} ≤ 5.5V: Over common-mode range from –15V to 15V	-	-	0.3	V
V_{TH-}	Receiver Negative-going Input Threshold	For 3V ≤ V_{CC} ≤ 5.5V: Over common-mode range from –7V to 12V	–0.2	-	-	V
		For 4.5V ≤ V_{CC} ≤ 5.5V: Over common-mode range from –15V to 15V	–0.3	-	-	V
V_{HYS}	Input Hysteresis	Over common-mode range from –15V to 15V	-	120	-	mV
	Logic Inputs and Receiver Outputs					
V_{IL}	Input Logic Threshold Low	RE, REb, RE12, RE34	-	-	0.8	V
V_{IH}	Input Logic Threshold High	RE, REb, RE12, RE34	2.0	-	V_{CC}	V
V_{IHYS}	Input Logic Hysteresis	RE, REb, RE12, RE34	-	100	-	mV
I_{IL}	Logic Input Current	RE, RE12, RE34 (pull-down)	–1	-	100	µA
		REb (pull-up)	–100	-	1	µA
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{ID} = 200mV, 3V ≤ V_{CC} ≤ 5.5V	V_{CC} – 0.6	-	-	V
		I_{OH} = –8mA, V_{ID} = 200mV, 4.5V ≤ V_{CC} ≤ 5.5V	V_{CC} – 0.6	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{ID} = –200mV, 3V ≤ V_{CC} ≤ 5.5V	-	0.2	0.4	V
		I_{OL} = 8mA, V_{ID} = –200mV, 4.5V ≤ V_{CC} ≤ 5.5V	-	0.2	0.4	V
I_{OZR}	Output High-Impedance Current	0 ≤ V_{RO} ≤ 5.5V, RE, RE12, RE34 = 0V, REb = V_{CC}	–1	-	1	µA
	Device					
I_{CC}	Supply Current	RE, RE12, RE34 = V_{CC} or REb = GND	-	3.0	7	mA

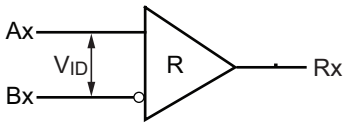
Receiver Switching Characteristics—MxL83433 and MxL83434 (32Mbps)

Unless otherwise noted, V_{CC} = 3V to 5.5V, ambient temperature $T_{MIN} < T_A < TM_{AX}$. Typical values are at V_{CC} = 3.3V, ambient temperature T_A = 25°C. The specifications apply over the full operating range from –40°C to 125°C unless otherwise noted.

Table 7: Receiver Switching Characteristics (32Mbps)

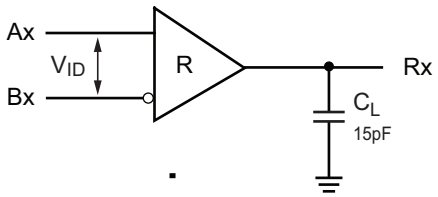
Symbol	Parameter	Conditions	Min	Typ	Max	Units
-	Maximum Data Rate	$\|V_{ID}\|$ = 1.5V, C_L = 15pF	32	-	-	Mbps
t_{RPLH}, t_{RPHL}	Receiver Propagation Delay	$\|V_{ID}\|$ = 1.5V, C_L = 15pF (Figure 3 on page 5).	-	7.5	17	ns
$\|t_{RPHL} – t_{RPLH}\|$	Receiver Skew		-	2	6	ns
t_r	Receiver Output Rise/Fall Time	$\|V_{ID}\|$ = 1.5V, C_L = 15pF	-	3	7	ns
t_f			-	3	7	ns
$t_{SK(C-C)}$	Channel-to-Channel Delay Skew	$\|V_{ID}\|$ = 1.5V, C_L = 15pF, same supply voltage and operating temperature.	-	-	6	ns
$t_{SK(P-P)}$	Part-to-Part Propagation Delay Skew		-	-	12	ns
t_{RHZ}	Receiver Disable Time from Output High	C_L = 15pF, R_L = 1kΩ (Figure 4 on page 6).	-	8	25	ns
t_{RLZ}	Receiver Disable Time from Output Low		-	8	25	ns
t_{RZH}	Receiver Enable Time to Output High		-	9	30	ns
t_{RZL}	Receiver Enable Time to Output Low		-	9	30	ns

Test Circuits and Timing Diagrams



REb/RE/RE12/RE34 = Enabled

Figure 2: Receiver DC Test Circuit



REb/RE/RE12/RE34 = Enabled

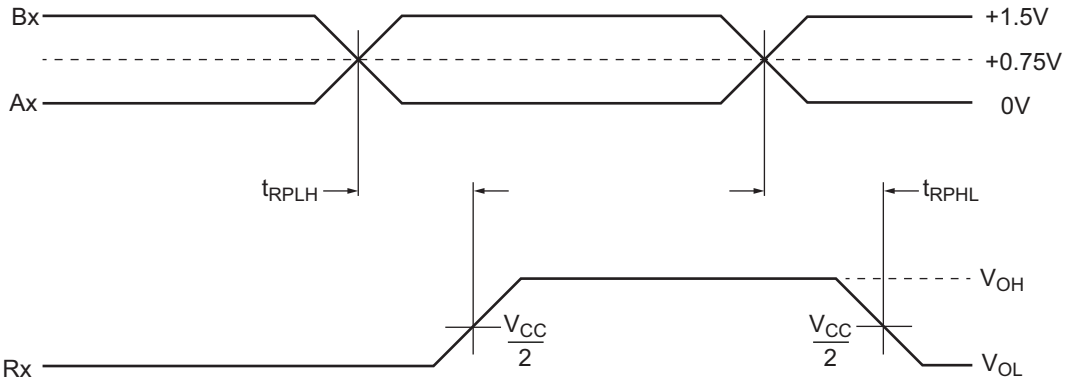


Figure 3: Receiver Propagation Delay Test Circuit and Timing Diagram

Note: C_L includes probe and trace capacitance.

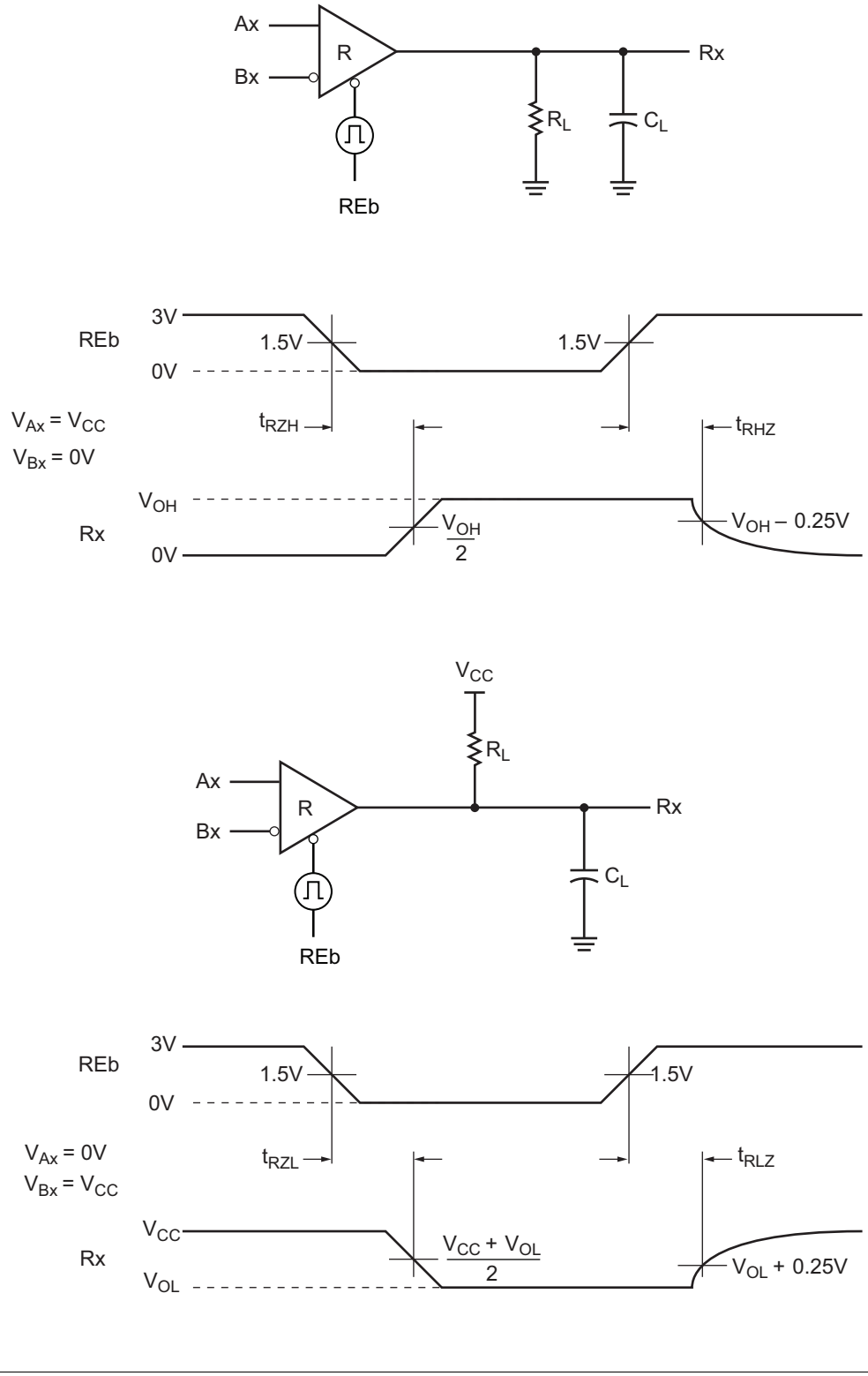


Figure 4: Receiver Enable and Disable Times Test Circuit and Timing Diagram for REb

Note: C_L includes probe and trace capacitance.

Typical Performance Characteristics

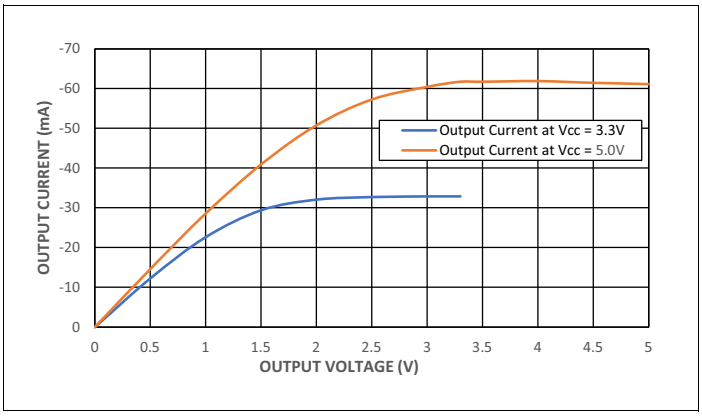


Figure 5: Output Current vs Output Low Voltage

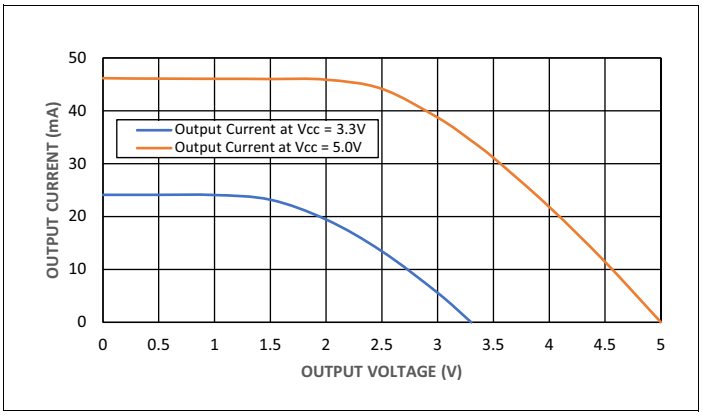


Figure 6: Output Current vs Output High Voltage

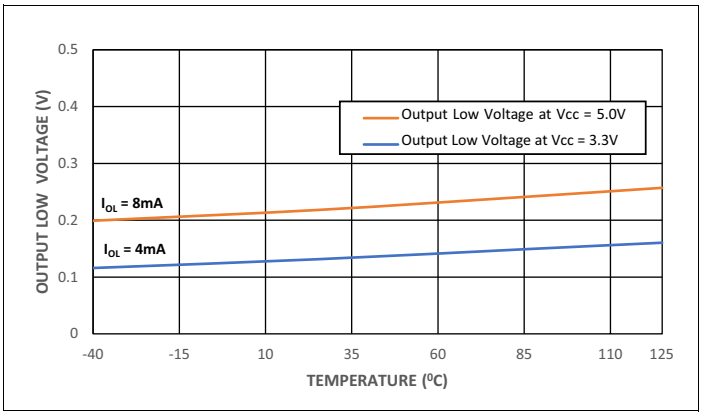


Figure 7: Output Low Voltage vs Temperature

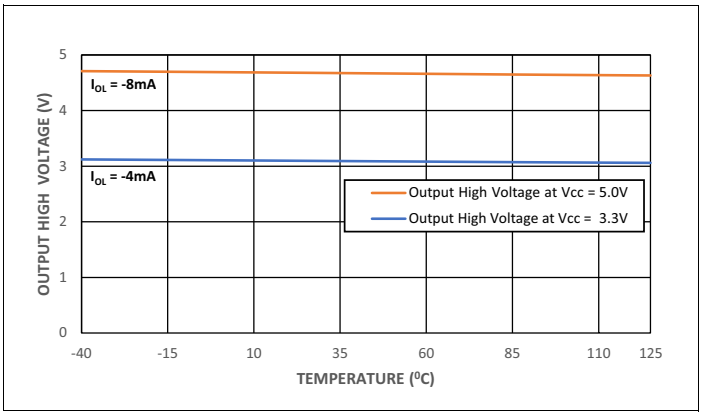


Figure 8: Output High Voltage vs Temperature

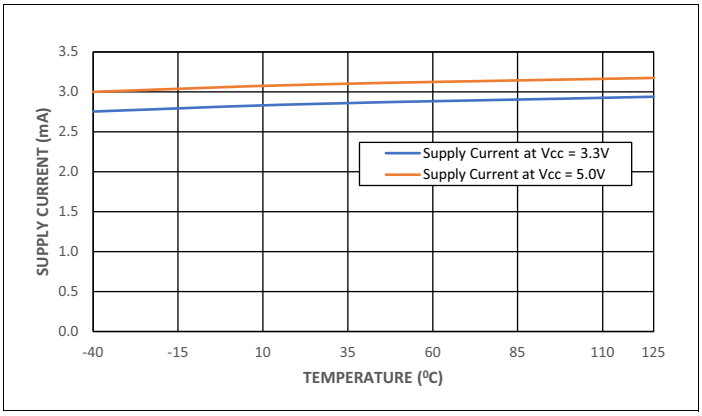


Figure 9: Supply Current vs. Temperature

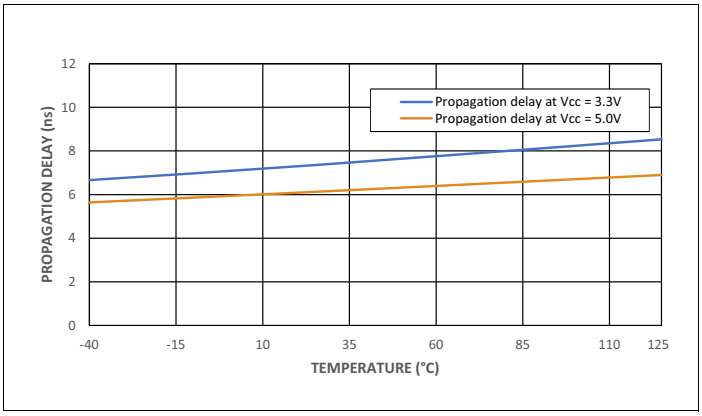


Figure 10: Propagation Delay vs. Temperature

Function Tables

Table 8: Receiver Enable Logic Configuration (MxL83433)

Receiver Enable					
Inputs		**Outputs**			
RE	REb	R1	R2	R3	R4
0	0	Enable	Enable	Enable	Enable
0	1	High-Z	High-Z	High-Z	High-Z
1	0	Enable	Enable	Enable	Enable
1	1	Enable	Enable	Enable	Enable

Table 9: Receiver Enable Logic Configuration (MxL83434)

Receiver Enable					
Inputs		**Outputs**			
RE12	RE34	R1	R2	R3	R4
0	0	High-Z	High-Z	High-Z	High-Z
0	1	High-Z	High-Z	Enable	Enable
1	0	Enable	Enable	High-Z	High-Z
1	1	Enable	Enable	Enable	Enable

Table 10: General Configuration

Differential $V_{ID} = \lvert V_{Ax}\text{-}V_{Bx} \rvert$	**RE/REb/RE12/RE34**	**Rx Output**
$V_{ID} \geq V_{TH+}$	Enabled	H
$V_{TH-} \leq V_{ID} \leq V_{TH+}$	Enabled	Undefined
$V_{ID} \leq V_{TH-}$	Enabled	L
Open	Enabled	H
X	Disabled	High-Z

Pin Information

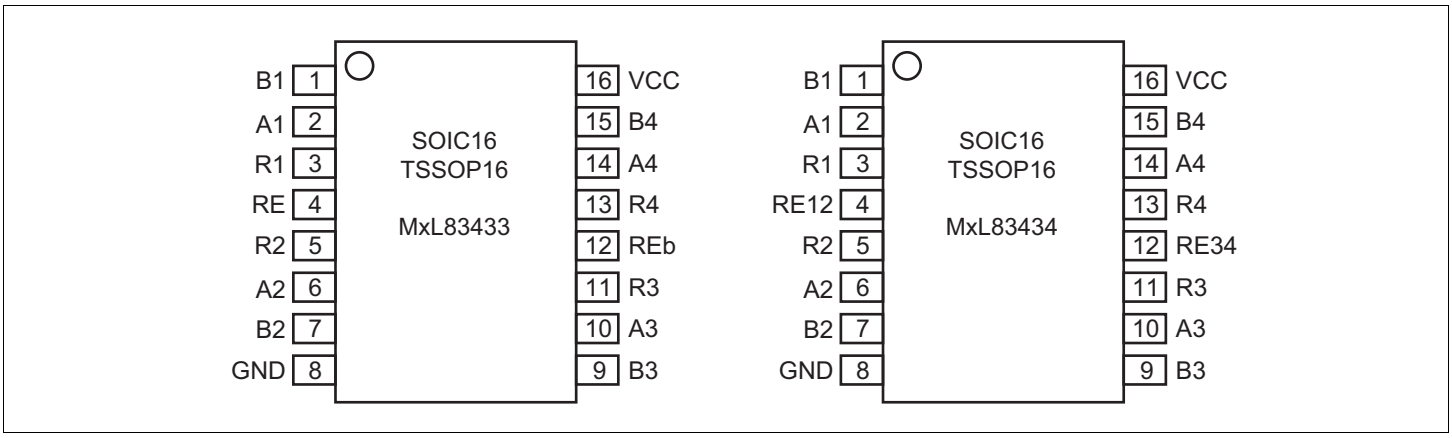


Figure 11: Pin Configuration

Pin Descriptions

Table 11: Pin Assignments

Pin Number	Pin Name		Function
	MxL83433	MxL83434	
1	B1	B1	Inverting receiver input.
2	A1	A1	Non-inverting receiver input.
3	R1	R1	Receiver output. For detailed functionality, see Table 10 on page 8.
4	RE	RE12	Active-High receiver output enable. ■ RE (MxL83433): Enables all four channels. Internal weak pull-down resistor. ■ RE12 (MxL83434): Enables channels 1 and 2. Internal weak pull-down resistor. For detailed functionality, see Table 8 on page 8 and Table 9 on page 8.
5	R2	R2	Receiver output. For detailed functionality, see Table 10 on page 8.
6	A2	A2	Non-inverting receiver input.
7	B2	B2	Inverting receiver input.
8	GND	GND	Ground.
9	B3	B3	Inverting receiver input.
10	A3	A3	Non-inverting receiver input.
11	R3	R3	Receiver output. For detailed functionality, see Table 10 on page 8.
12	REb	RE34	■ REb (MxL83433): Active-Low enable. Enables all four channels. Internal weak pull-up resistor. ■ RE34 (MxL83434): Active-High enable. Enables channels 3 and 4. Internal weak pull-down resistor. For detailed functionality, see Table 8 on page 8 and Table 9 on page 8.
13	R4	R4	Receiver output. For detailed functionality, see Table 10 on page 8.
14	A4	A4	Non-inverting receiver input.
15	B4	B4	Inverting receiver input.
16	VCC	VCC	System power supply input.

Application Information

The MxL83433 and MxL83434 are a family of monolithic quadruple differential line RS-485/RS-422 receivers that meet the necessary requirements for *TIA/EIA-485-A* and *TIA/EIA-422-B* serial interface standards. These devices are suitable for different applications ranging from high-speed motor drives to wireless infrastructure and building automation. The MxL83433 and MxL83434 devices are excellent choices for all space-constrained applications that require robust, high-performance communication, high immunity to electrical fast transient (EFT) protection (*IEC 61000-4-4*), and electrostatic discharge (ESD) protection (*IEC61000-4-2*).

This family has an extended common-mode range of –15V to 15V to accommodate ground potential differences between receiver nodes. These devices can operate with a wide supply voltage range from 3V to 5.5V and operate up to 32Mbps in both standard and extended industrial temperature ranges.

ESD Protection (IEC 61000-4-2)

The *IEC 61000-4-2* standard covers ESD testing and performance of finished equipment. However, it does not refer to integrated circuits. The MxL83433 and MxL83434 devices help you design equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. MaxLinear develops state-of-the-art structures employed on the bus pins to protect the device and the rest of the system against ESD damage during operation.

The receiver inputs of the MxL83433 and MxL83434 devices are specifically designed and characterized to provide high levels of system ESD protection.

Electrical Fast Transient Protection

Inductive loads such as relays, switch contractors, or industrial motors can create high-frequency bursts during their operations. Electrical fast transient (EFT) tests evaluate immunity of electrical and electronic equipment when subjected to repetitive electrical fast transient or bursts. The MxL83433 and MxL83434 devices are designed and qualified to a high level of EFT protection.

128 Receivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (1 unit load), and the standard driver can drive up to 32 unit loads (UL). The MxL83433 and MxL83434 receivers have a ¼-unit load receiver input impedance of 48kΩ, allowing up to 128 receivers to be connected in parallel on the bus line.

Standard Fail-Safe Receivers

The receiver inputs of the MxL83433 and MxL83434 devices guarantee to produce a logic-high output when the inputs are open-circuited (no termination resistor between inputs A and B). However, when the bus is terminated and the transmitters are disabled, the differential voltage between inputs A and B falls into the *undetermined* zone ($-200mV \leq V_{AB} \leq 200mV$). Consequently, the output becomes undefined. To properly maintain a fail-safe receiver output with a terminated bus line, input A must be biased at least 200mV above input B for the receiver output to produce a logic high for the standard fail-safe receiver.

For more information about the differences between standard and advanced RS-485/RS-422 fail-safe receivers, refer to the *RS-485 Advanced Fail-Safe Feature Application Note* (291AN).

Global Enable and Paired Enable Configurations

The MxL83433 device offers a global enable configuration. All four receiver outputs are enabled simultaneously when RE = V_{CC} or REb = GND.
When REb = V_{CC} and RE = GND, all four receiver outputs are in high impedance state.

The MxL83434 device offers a paired enable configuration. RE12 = V_{CC} enables channel 1 and channel 2 receivers. RE34 = V_{CC} enables channel 3 and channel 4 receivers. When RE12 = RE34 = GND, all outputs are disabled and all four receiver outputs are in high impedance state.

For more information about configuration, see Table 8 on page 8 and Table 9 on page 8.

Enhanced Receiver Noise Immunity

The MxL83433 and MxL834344 differential receivers feature a fully symmetrical threshold to maintain duty cycle of the signal even with small amplitude input signals. With a large receiver hysteresis, these devices can provide additional noise immunity over standard *RS-485/RS-422* receivers, preventing high frequency noise pulses from the *RS-485/RS-422* bus from appearing on the receiver outputs.

Low Propagation Delay and Skew

The MxL83433 and MxL83434 devices provide low propagation delays, low channel-to-channel skews, and low device-to-device skews, even between devices from different manufacturing lots. This feature allows multiple channels and devices to receive communication data with minimal skew with respect to each other.

Channel-to-channel skew ($t_{SK(C-C)}$) is defined as the difference between the maximum channel delay and minimum channel delay measured across all four channels within a single device keeping the same power supply, same input signal (V_{ID} and V_{CM}) and same operating temperature.

Part-to-part skew ($t_{SK(P-P)}$) is defined as the difference between the maximum channel delay and minimum channel delay measured across the devices from different manufacturing lots keeping the same power supply, same input signal (V_{ID} and V_{CM}) and same operating temperature.

Multi-Protocol Receive Mode Support

When communication is required between systems that support different interfaces, you can use the MxL83433 and MxL83434 receivers as a translation device to bridge between multiple interfaces. The following cases are possible usage between the host transmitter and the MxL83433 and MxL83434 receiver.

Case 1: Single-ended driver (TTL, CMOS, LVTTL, or LVCMOS) to TTL level logic output

The MxL83433 and MxL83434 devices can receive single-ended data from standard high-speed TTL, CMOS, LVTTL, or LVCMOS output driver. This is accomplished by tying one of the inputs to a fixed bias voltage at $V_{CC}/2$ and connecting the other input to the single-ended driver output. In this application, the MxL83433 and MxL83434 receivers act as a level shifter to convert variable-level signal input into TTL-level logic output. The receiver trip point can be adjusted to accommodate different driver output swings by changing the resistor divider at the bias input. Figure 12 shows the single-ended receiver configuration with driver from TTL, CMOS, LVTTL, or LVCMOS as output and receiver connected via a short PCB trace to non-inverting input A (+). The 4.7K resistors act as a voltage divider to set the inverting input B (-) at $V_{CC}/2$.

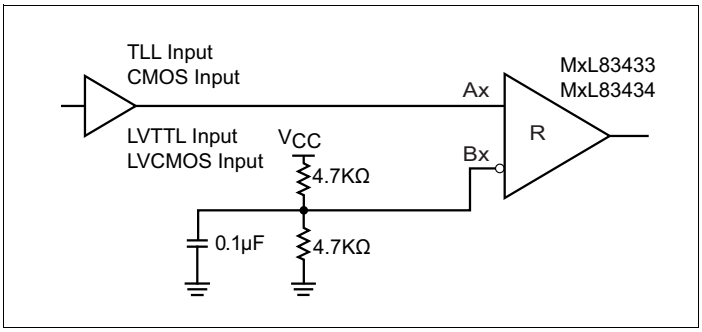


Figure 12: Multi-Protocol Receive Mode Support Case 1

Table 12: Multi-Protocol Receive Mode with various TTL, CMOS, LVTTL, or LVCMOS Level Input

Driver V_{CC}(V)	Input B (-) Bias at $V_{CC}/2$	Input A(+) Connect to Driver Output	5V Output R (TTL)	3.3V Output R (LVTTL)
5.0V	2.5V	TTL/CMOS (74ALS125, 74AC125…)	TTL output	LVTTL output
3.6V	1.8V	LVTTL (74LV125...)	TTL output	LVTTL output
3.3V	1.65V	LVCMOS (74LVC125...)	TTL output	LVTTL output

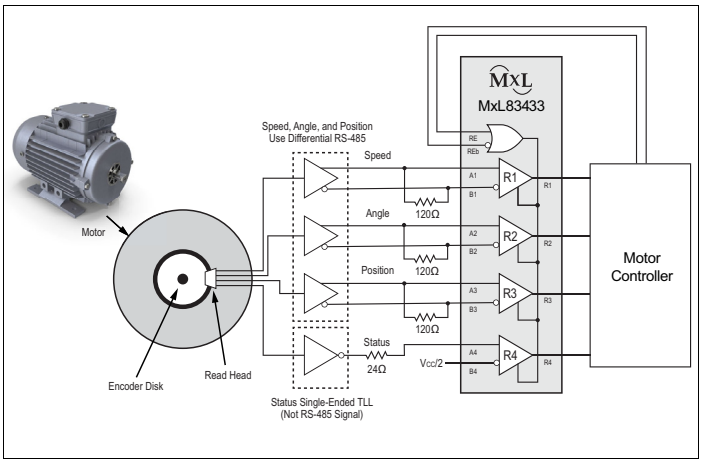


Figure 13: Application Block Diagram of Multi-Protocol Receive Mode

Case 2: Logic inversion to TTL level output

The MxL83433 or the MxL83434 receiver can be configured as a logic inverter for standard high-speed output driver. In this configuration, the input signal can be connected to inverting input B with voltage divider network connected to non-inverting input A.

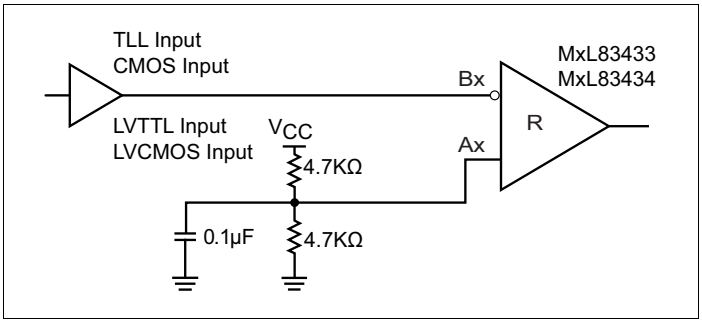


Figure 14: Multi-Protocol Receive Mode Support Case 2 (Logic Inversion)

Case 3: Single-ended RS-232 driver output to TTL level logic output (translation of RS-232 signal to TTL's level)

A single-ended RS-232 driver output can be converted to TTL level logic output by using the MxL83433 or MxL83434 as a receiver. The RS-232 driver typically has single-ended output swing from –5.5V to +5.5V and can be directly connected into terminal A with terminal B which connects to GND. This configuration supports conversion of RS-232 driver up to approximately 3Mbps.

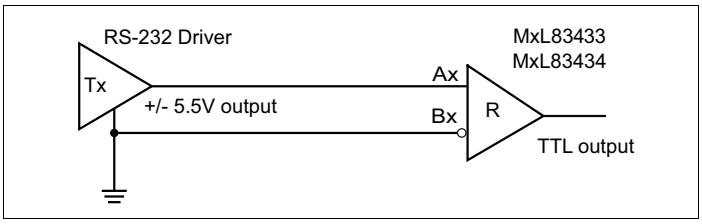


Figure 15: Multi-Protocol Receive Mode Support Case 3a

In some cases, the RS-232 driver output levels can be as high as ±15V. The MxL83433 and MxL83434 receiver inputs can tolerate up to ±15V with the maximum supported data rate of 250Kbps. To achieve higher data rates at ±15V, a resistor divider network with 2kΩ and 3kΩ resistors provides the required attenuation to satisfy the requirements listed in Table 13. It attenuates the RS-232 signal by 40%, reducing the output level from ±15V to ±9V. It allows conversion of the RS-232 driver output up to 1.5Mbps.

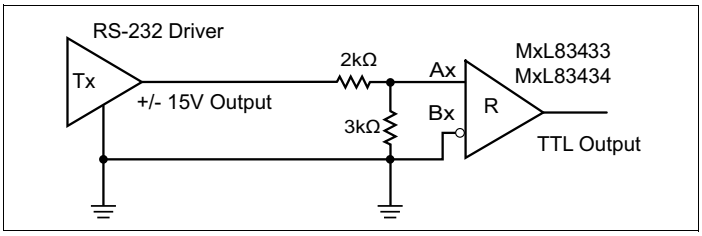


Figure 16: Multi-Protocol Receive Mode Support Case 3b

The following table lists the maximum data rate supported for multi-protocol receive mode operations.

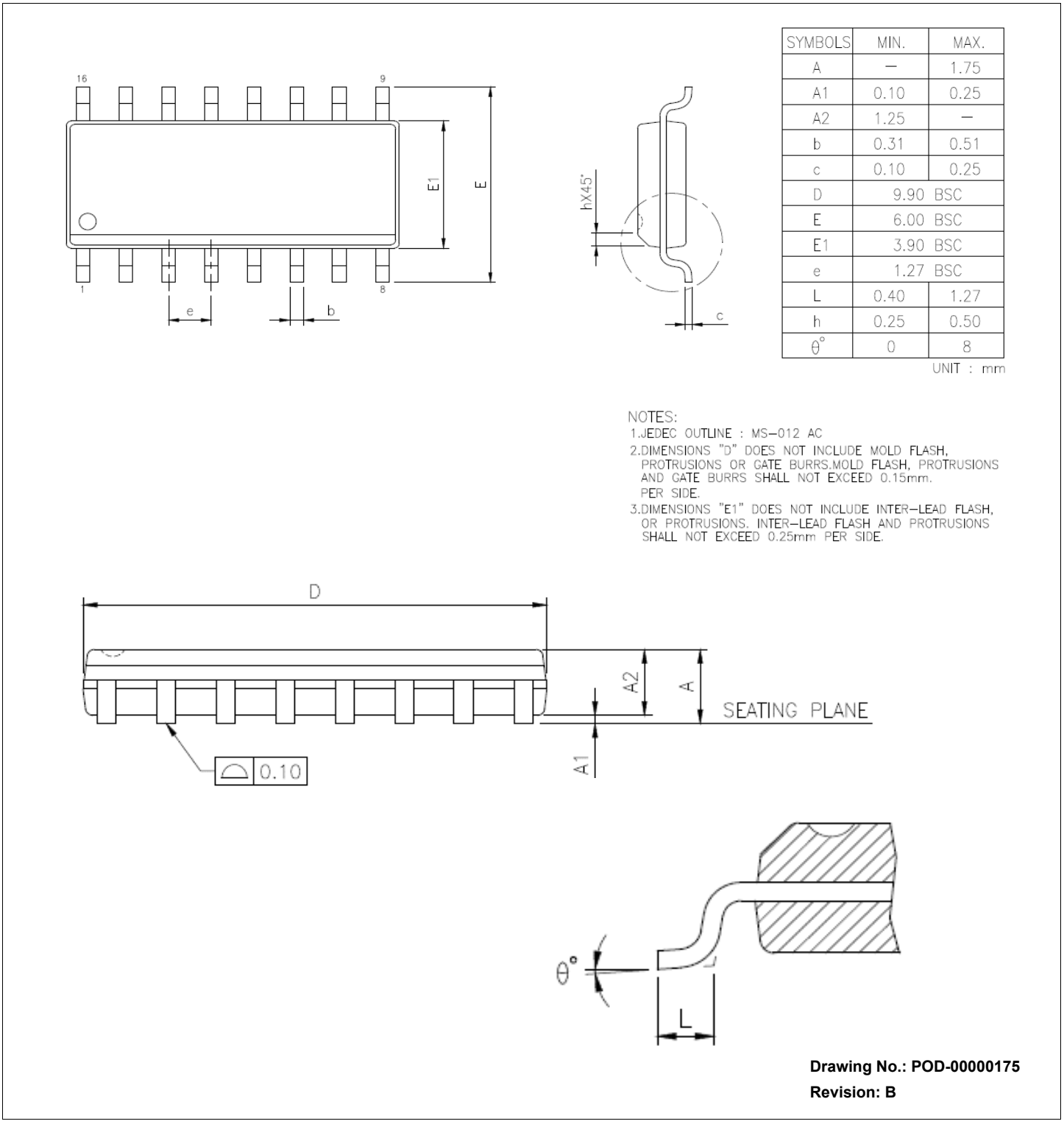
Table 13: Multi-Protocol Receive Mode Data Rate Support

Device	Multi-Protocol Receive Mode Input Voltage	Maximum Data Rate Achievable[1]
MxL83433 and MxL83434	±0.5V	12Mbps
	±1.0V	32Mbps
	±1.5V	32Mbps
	±2.0V	25Mbps
	±3.0V	15Mbps
	±5.0V	4Mbps
	±7.0V	2Mbps
	±9.0V	1.5Mbps
	±11.0V	1Mbps
	±13.0V	750Kbps
	±15.0V	250Kbps

1. These values are representative performance of a typical device with duty cycle of 60/40 percent under typical operating condition.

Mechanical Dimensions

NSOIC16



SYMBOLS	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

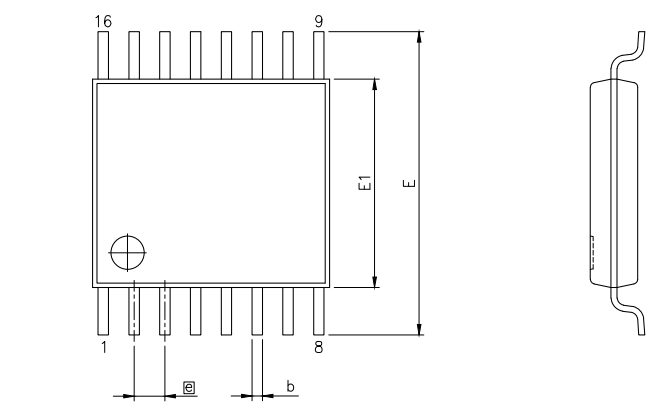
UNIT : mm

NOTES:
1. JEDEC OUTLINE : MS-012 AC
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

Drawing No.: POD-00000175
Revision: B

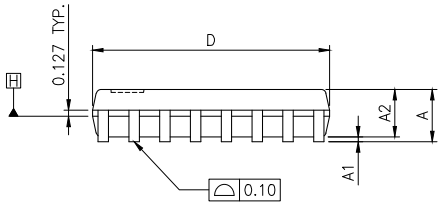
Figure 17: Mechanical Dimensions—NSOIC16

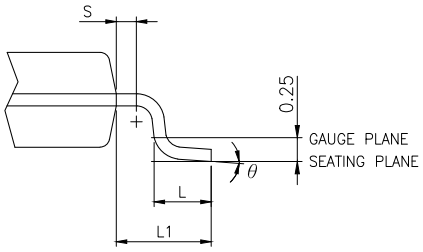
TSSOP16



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





NOTES:
1. JEDEC OUTLINE : MO-153 AB
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

Drawing No.: POD-00000176
Revision: C

Figure 18: Mechanical Dimensions—TSSOP16

Ordering Information

Table 14: Ordering Information

Ordering Part Number	Data Rate (Mbps)	Enables	Operating Temperature Range	Package	Packaging
MXL83433E-ADA-R	32	Global	–40°C to 125°C	NSOIC16	Tape and Reel
MXL83433E-AGA-R	32	Global	–40°C to 125°C	TSSOP16	Tape and Reel
MXL83434E-ADA-R	32	Paired	–40°C to 125°C	NSOIC16	Tape and Reel
MXL83434E-AGA-R	32	Paired	–40°C to 125°C	TSSOP16	Tape and Reel
MXL83433I-ADA-R	32	Global	–40°C to 85°C	NSOIC16	Tape and Reel
MXL83433I-AGA-R	32	Global	–40°C to 85°C	TSSOP16	Tape and Reel
MXL83434I-ADA-R	32	Paired	–40°C to 85°C	NSOIC16	Tape and Reel
MXL83434I-AGA-R	32	Paired	–40°C to 85°C	TSSOP16	Tape and Reel
MXL83433E-ADA-EVK-1	MxL83433 Evaluation Kit NSOIC16				
MXL83434E-AGA-EVK-1	MxL83434 Evaluation Kit TSSOP16				

Note:

- For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL83433 and www.maxlinear.com/MxL83434.
- For more information about the EVKs, refer to the refer to the *MxL83433 and MxL83434 EVK User Manual* (031UM).

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
760.692.0711
760.444.8598

www.maxlinear.com