



General Description

The MxL9364xA (MxL93642A and MxL93643A) are highly integrated PAM4 DSP SoCs that enable 400Gbps optical interconnects using 100Gbps over a single optical wavelength ($100G/\lambda$).

The devices have a high-speed electrical interface with eight transmit (Tx) and receive (Rx) input/output (I/O) that connect electrically through a module connector to the host ASIC.

The devices also have a high-speed optical side interface that has four Tx and Rx I/O that connect through the optical components to optical fibers.

The electrical interface supports 53.125Gbps PAM4 signaling per lane over C2M host channels.

The optical interface supports 106.25Gbps PAM4 signaling per wavelength for DR, FR, and LR applications.

The devices support DSP functions including line side Tx digital pre-distortion (DPD), transmit pre-emphasis (Tx FIR), and receive feed-forward equalization (Rx FFE).

The MxL9364xA, in a 12mm × 13mm package, includes integrated TOSA drivers with differential and single-ended options for both silicon photonics (SiPh) and electro-absorption modulated laser (EML) implementations. It offers exceptional signal integrity for signals in a compact footprint suitable for next generation optical module form-factors.

Applications

- QSFP-DD optical modules
- OSFP optical modules
- QSFP-DD AEC/ACC and AOC
- OSFP AEC/ACC and AOC

Features

- 400G gearbox capability that enables 400G DR4, FR4, LR4, VR4/SR4
- 400G to 100G break-out mode
- Tx equalization that includes pre-emphasis, digital pre-distortion, and reflection cancellation
- Rx equalization that includes CTLE, multi-tap FFE, and reflection cancellation
- Supports host channels with Nyquist loss in excess of 20dB
- Integrated crystal oscillator that eliminates the need for a costly reference clock source
- Small package size to enable the QSFP-DD space requirements
- Mission mode BER monitoring
- SNR/Histogram reporting for each receiver on both electrical and optical interfaces
- Diagnostic loop-back and test pattern generation and error checking
- SPI and I²C slave interface to communicate to module MCU
- SPI master for flash memory interface
- I²C master interface for TIA direct control
- Embedded CPU for real-time control
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected

Supported Standards

- IEEE Std 802.3bs
- IEEE Std 802.3cd
- IEEE Std 802.3cm
- IEEE Std 802.3cu
- IEEE Std 802.3db

Introduction

The MxL9364xA device is a highly integrated PAM4 DSP SoC that operates at a capacity of 400G and enables 100G for each optical wavelength. The SoC includes Tx DPD, Tx pre-emphasis (Tx FIR), and Rx equalization (FFE) functionality. Additional mission mode BER monitoring capabilities are also available.

The main mode of operation is the gearbox mode: the bit streams from a pair of electrical SerDes interfaces are multiplexed into a single stream at the bit level and transmitted to one optical SerDes interface. The bit stream from one optical SerDes interface is de-multiplexed into two separate streams at the bit level and transmitted to a pair of electrical SerDes interfaces. The bit streams from the electrical and optical SerDes interface are PAM-4 encoded.

IC Block Diagram

Figure 1 shows the functional block diagram of the MxL93642A device. The MxL93643A device is similar, however the output driver is not included in the optical Tx output block.

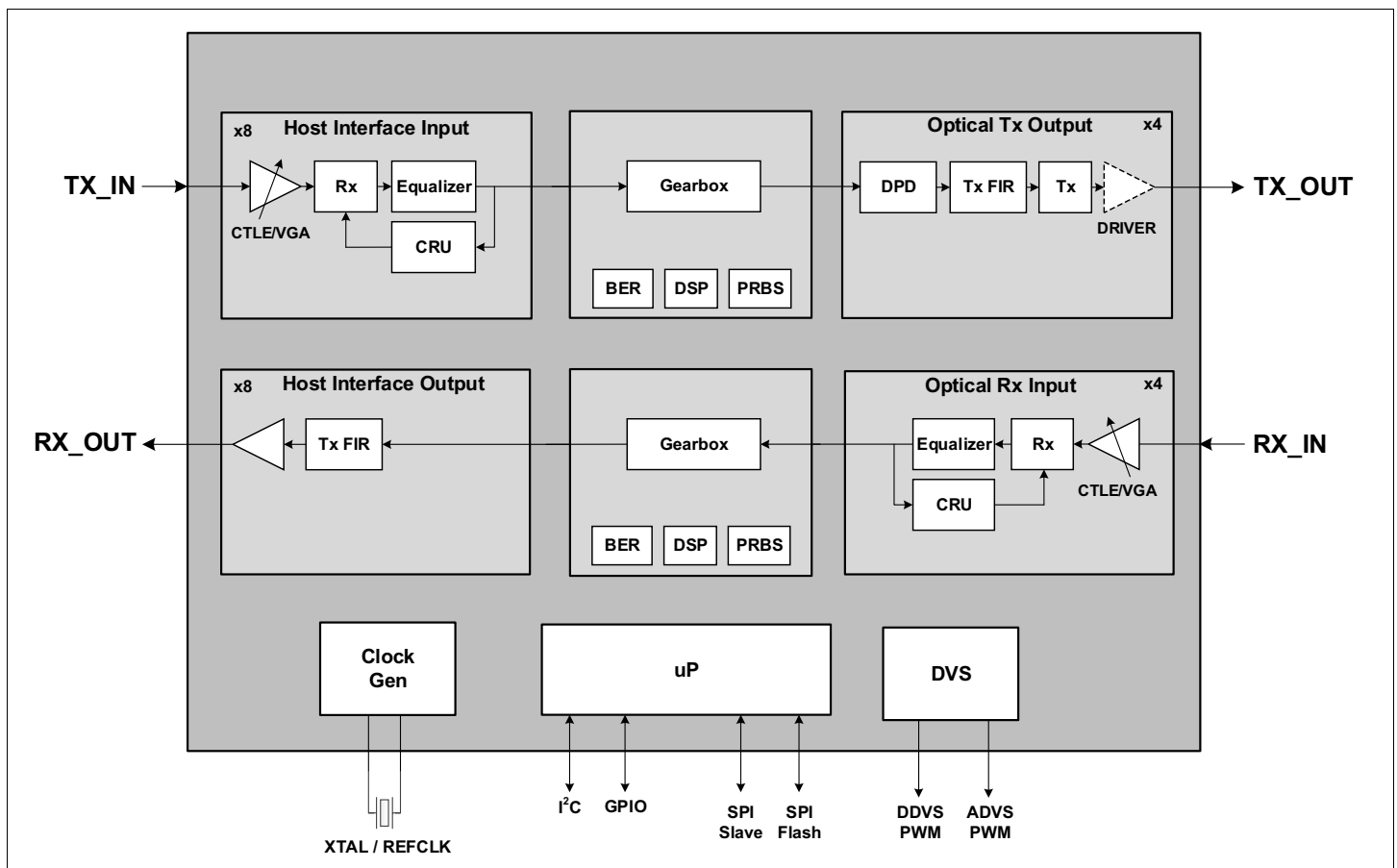


Figure 1: MxL93642A Simplified Block Diagram

Ordering Information

Table 1: Ordering Information

Marketing Part Number	Ordering Part Number	Description	Package	Shipping
MxL93642A	MXL93642A-PV-T	400G gearbox DSP with integrated driver.	FC-FBGA	Tray
MxL93643A	MXL93643A-PV-T	400G gearbox DSP without integrated driver.	FC-FBGA	Tray



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