MxL82203

16-bit I²C/SMBUS GPIO Expander
Preliminary Data Sheet

General Description

The MxL82203 is a 16-bit GPIO expander with an I²C/SMBus interface. After power-up, the MxL82203 has internal 100KΩ pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the MxL82203 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt behavior is configurable. It can be set to trigger on a rising edge, falling edge, or both edges. The interrupt condition is cleared either when the input returns to its original state or when the current input state is read.

The MxL82203 is an enhanced version of the PCA9539 and TCA9539. The MxL82203 is pin and software compatible with the PCA9539 and TCA9539(note: that software registers are compatible to thePCA9539, but the I²C slave address is different). The MxL82203 is available in 24-pin QFN and 24-pin TSSOP packages.

Applications

- Personal digital assistants (PDA)
- Cellular phones/data devices
- Battery-operated devices
- Global Positioning System (GPS)
- Bluetooth

Features

- 1.62V to 5.5V operating voltage
- 16 General Purpose I/Os (GPIOs)
- Maximum stand-by current of 1μA at +1.8V
- I²C/SMBus bus interface
- I²C clock frequency up to 1MHz
- Noise filter on SDA and SCL inputs
- Up to 16 I²C Slave Addresses
- Individually programmable inputs
- Internal pull-up resistors
- Polarity inversion
- Individual interrupt enable
- Rising edge and/or falling edge interrupt
- Input filter
- Individually programmable outputs
- Output level control
- Output three-state control
- Open-drain active low interrupt output
- Active-low reset input
- Pin and software compatible with PCA9539 and TCA9539
- 3kV HBM ESD protection per *JESD22-A114F*
- 200mA latch-up performance per *JESD78B*

Revision History

Document No.	Release Date	Change Description
296DSR00	May 20, 2026	Initial preliminary release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supply Voltage	-	6	V
Supply Current	-	160	mA
Ground Current	-	200	mA
External Current Limit of each GPIO	-	25	mA
Total Current Limit for GPIO[15:8] and GPIO[7:0]	-	100	mA
Total Current Limit for GPIO[15:0]	-	200	mA
Total Supply Current sourced by all GPIOs	-	160	mA
Operating Temperature	–40	+85	°C
Storage Temperature	–65	+150	°C
Power Dissipation	-	200	mW

Electrical Characteristics

DC Electrical Characteristics

DC Electrical characteristics at V_{cc} = 1.62V to 5.5V, T_A = 40°C to +85°C, unless otherwise specified.

Table 2: DC Electrical Characteristics

Symbol	Parameter	Limits 1.8V ± 10% Min	Limits 1.8V ± 10% Max	Limits 2.5V ± 10% Min	Limits 2.5V ± 10% Max	Limits 3.3V ± 10% Min	Limits 3.3V ± 10% Max	Limits 5V ± 10% Min	Limits 5V ± 10% Max	Units	Conditions
V_{IL}	Input Low Voltage	–0.3	0.3VCC	–0.3	0.3VCC	–0.3	0.3VCC	–0.3	0.3×VCC	V	Note 1
V_{IL}	Input Low Voltage	–0.3	0.2	–0.3	0.5	–0.3	0.8	–0.3	1.1	V	Note 2
V_{IH}	Input High Voltage	1.3	VCC	1.8	VCC	2.3	VCC	0.7×VCC	VCC	V	Note 1
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	2.0	5.5	2.3	5.5	V	Note 2
V_{OL}	Output Low Voltage	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{OL} = 3mA Note 3
V_{OL}	Output Low Voltage	0	0.5	0	0.5	0	0.5	0	0.5	V	I_{OL} = 8mA Note 4
V_{OL}	Output Low Voltage	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{OL} = 1.5mA I_{OL} = 4mA I_{OL} = 6mA Note 5
V_{OH}	Output High Voltage	1.2	-	1.8	-	2.6	-	4.1	-	V	I_{OH} = –8mA Note 4
I_{IL}	Input Low Leakage Current	-	±10	-	±10	-	±10	-	±10	µA	-
I_{IH}	Input High Leakage Current	-	±10	-	±10	-	±10	-	±10	µA	-
I_{CC}	Power Supply Current	-	50	-	100	-	200	-	400	µA	Note 6
I_{CC}	Power Supply Current	-	150	-	250	-	500	-	1000	µA	Note 7
I_{CCS}	Standby Current	-	1	-	2	-	5	-	7	µA	Note 8
C_{IN}	Input Pin Capacitance	-	5	-	5	-	5	-	5	pF	-
R_{GPIO}	GPIO pull-up Resistance	60	140	60	140	60	140	60	140	kΩ	100kΩ ±40%
$R_{RESET\#}$	Pull-up Resistence	35	85	35	85	35	85	35	85	KΩ	60kΩ ±40%

1. For I^2C input signals (SDA, SCL).

2. For GPIOs, A0, A1, and A2 signals.

3. For I^2C output signal SDA.

4. For GPIOs.

5. For IRQ# signal

6. Test 1: SCL frequency is 1MHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

7. Test 2: SCL frequency is 1MHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

8. Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

AC Electrical Characteristics

AC Electrical characteristics at V_{cc} = 1.62V to 5.5V, T_A = 40°C to +85°C, unless otherwise specified.

Table 3: AC Electrical Characteristics

Symbol	Parameter	Standard Mode I²C-Bus		Fast Mode I²C-Bus		Fast Mode Plus I²C-Bus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Operating Frequency	0	100	0	400	0	1000	kHz
T_{BUF}	Bus Free Time between STOP and START	4.7	-	1.3	-	0.5	-	µs
$T_{HD;STA}$	START Condition Hold Time	4.7	-	0.6	-	0.26	-	µs
$T_{SU;STA}$	START Condition Setup Time	4.7	-	0.6	-	0.26	-	µs
$T_{HD;DAT}$	Data Hold Time	0	-	0	-	0	-	ns
$T_{VD;ACK}$	Data Valid Acknowledge	-	3.45	-	0.9	-	0.45	µs
$T_{VD;DAT}$	SCL LOW to Data Out Valid	-	3.45	-	0.9	-	0.45	µs
$T_{SU;DAT}$	Data Setup time	250	-	150	-	50	-	ns
T_{LOW}	Clock LOW Period	4.7	-	1.3	-	0.5	-	µs
T_{HIGH}	Clock HIGH Period	4.0	-	0.6	-	0.26	-	µs
T_F	Clock/Data Fall Time	-	300	-	300	-	120	ns
T_R	Clock/Data Rise Time	-	1000	-	300	-	120	ns
T_{SP}	Pulse width of Spikes Tolerance	-	50	-	50	-	50	ns
T_{D1}	I²C-bus GPIO Output Valid	-	0.2	-	0.2	-	0.2	µs
T_{D4}	I²C Input Pin Interrupt Valid	-	4	-	4	-	4	µs
T_{D5}	I²C Input Pin Interrupt Clear	-	4	-	4	-	4	µs
T_{D15}	SCL Delay after Reset	3	-	3	-	3	-	µs

Pin Information

Pin Configuration

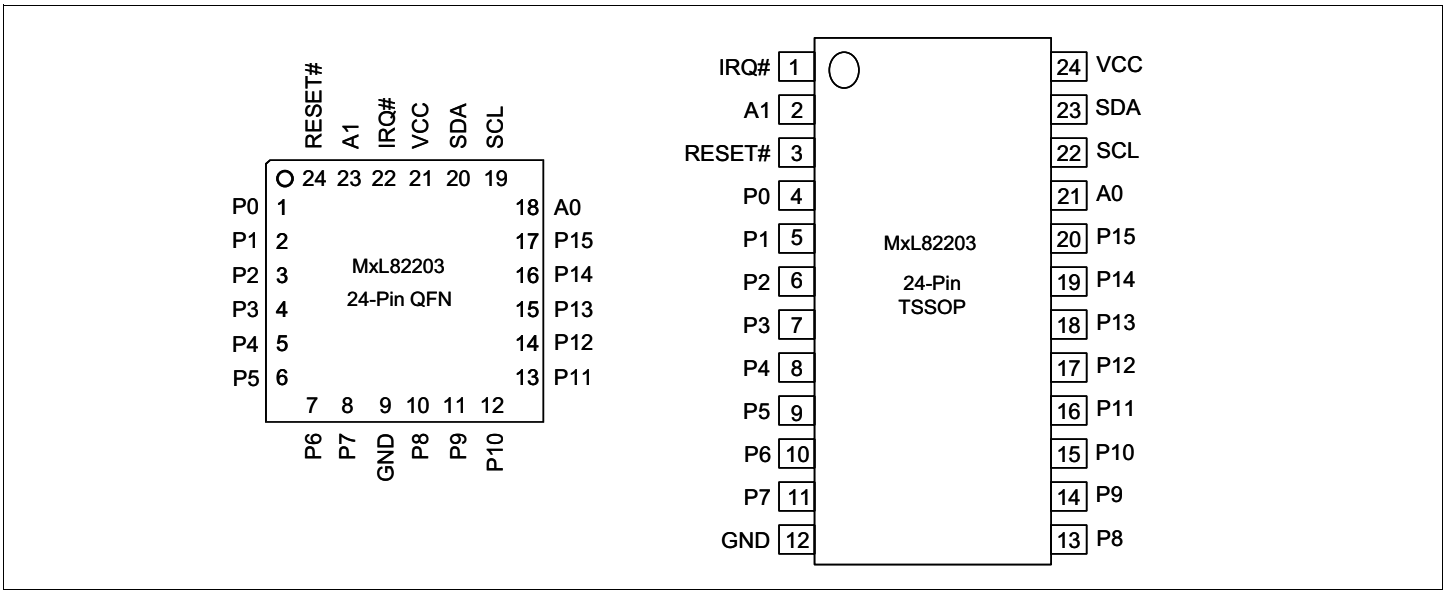


Figure 1: Pinout (Top View)

Pin Description

Table 4: Pin Description

Pin Name	QFN-24 Pin#	TSSOP-24 Pin#	Type	Description
I²C Interface				
SDA	20	23	I/O	I²C-bus data input/output (open-drain).
SCL	19	22	I	I²C-bus serial input clock.
IRQ#	22	1	OD	Interrupt output (open-drain, active low).
A0 A1	18 23	21 2	I	These pins select the I²C slave address. See Table 5 on page 8.
RESET#	24	3	I	Reset (active low) - A longer than 40ns low pulse on this pin resets the internal registers and all GPIOs are configured as inputs.
GPIOs				
P0 P1 P2 P3 P4 P5 P6 P7	1 2 3 4 5 6 7 8	4 5 6 7 8 9 10 11	I/O I/O I/O I/O I/O I/O I/O I/O	General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset.

Table 4: Pin Description

Pin Name	QFN-24 PIN#	TSSOP-24 PIN#	Type	Description
P8	10	13	I/O	General purpose I/O P8-P15. All GPIOs are configured as inputs upon power-up or after a reset.
P9	11	14	I/O	
P10	12	15	I/O	
P11	13	16	I/O	
P12	14	17	I/O	
P13	15	18	I/O	
P14	16	19	I/O	
P15	17	20	I/O	
Ancillary Signals				
VCC	21	24	Pwr	1.62V to 5.5V VCC supply voltage.
GND	9	12	Pwr	Power supply common, ground.
GND	Center Pad	-	Pwr	The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential.

Note: Pin type: I = Input, O = Output, I/O = Input/output, OD = Output Open Drain.

Block Diagram

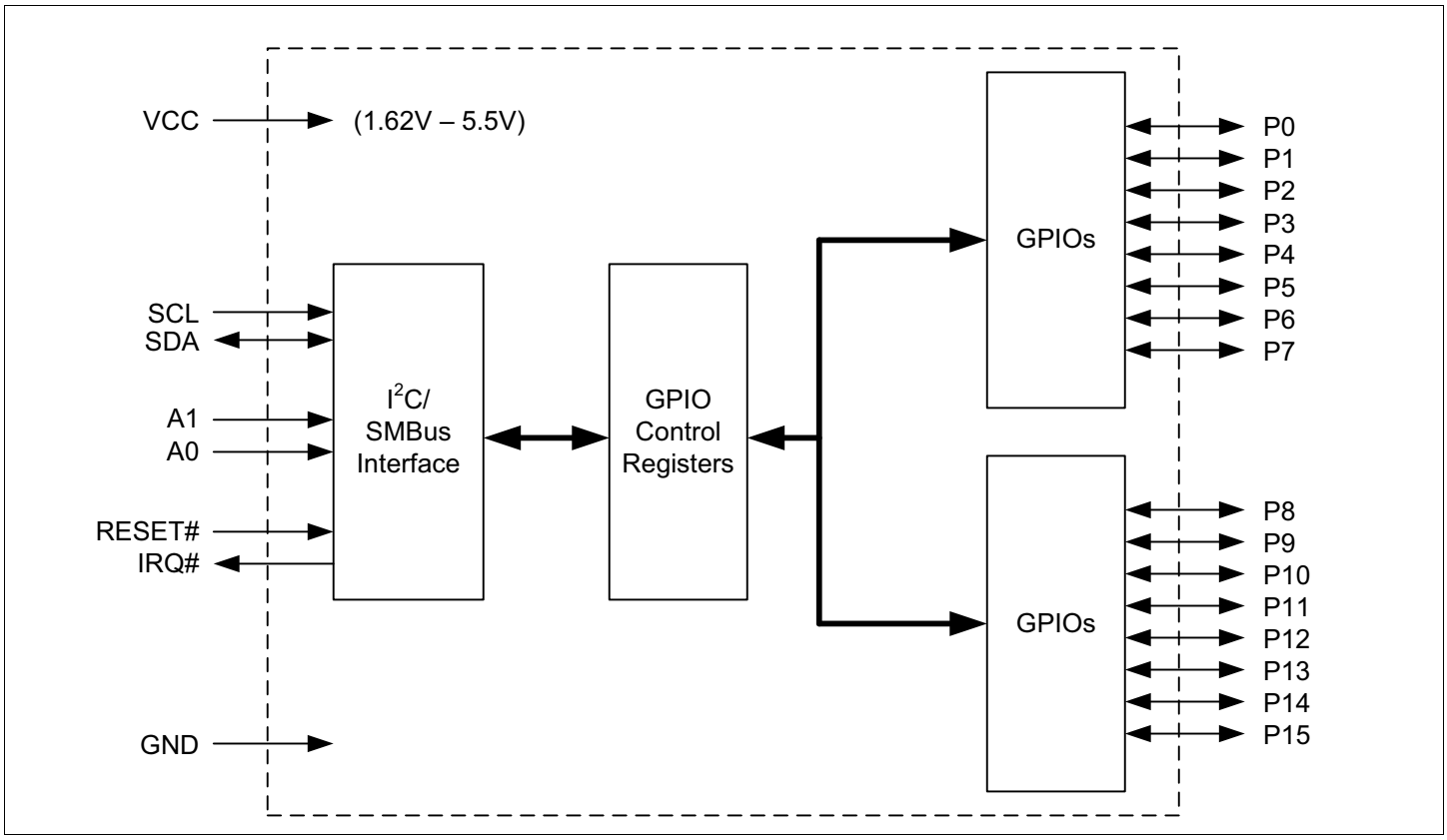


Figure 2: Functional Block Diagram

Functional Description

I²C-Bus Interface

The I²C-bus interface is compliant with the Standard-mode and fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the standard-mode, the serial clock and serial data can go up to 100kbps and in the fast-mode, the serial clock and serial data can go up to 400kbps.

The first byte sent by an I2C-bus master contains a start bit (SDA transition from high to low when SCL is high), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The MxL82203 responds to each write with an acknowledge (SDA driven LOW by MxL82203 for one clock cycle when SCL is HIGH). The last byte sent by an I2C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See the following figures. For complete details, refer to the I²C-bus specifications.

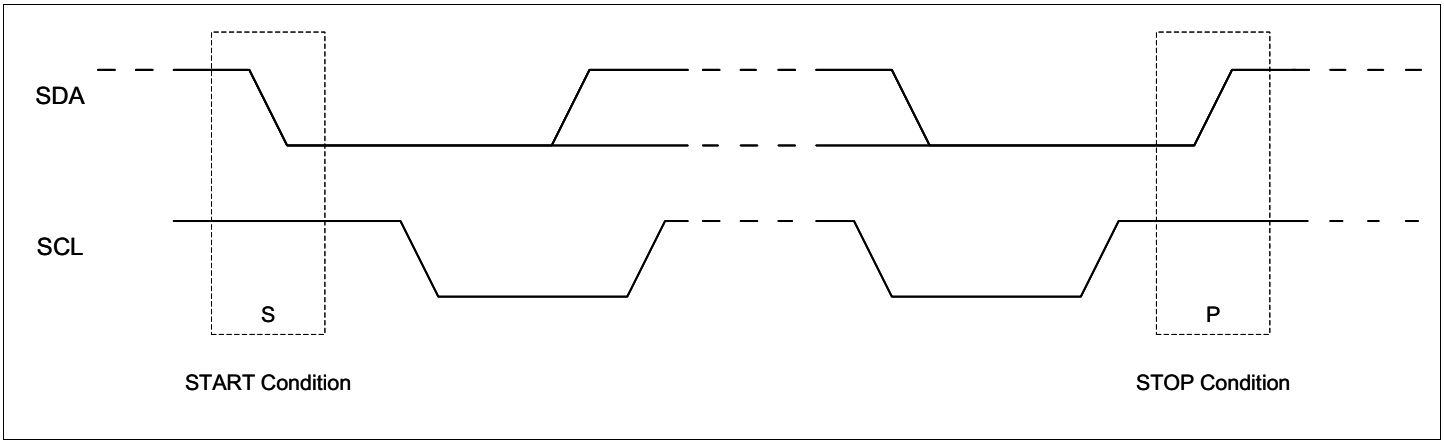


Figure 3: I²C Start and Stop Conditions

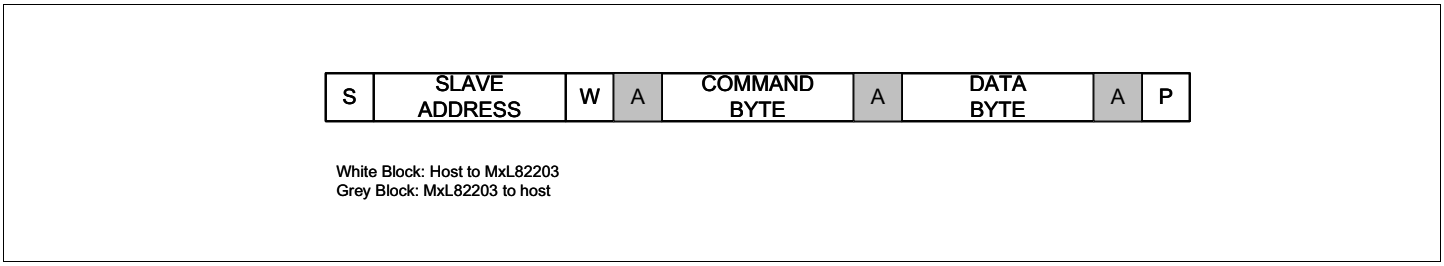


Figure 4: Master Writes To Slave

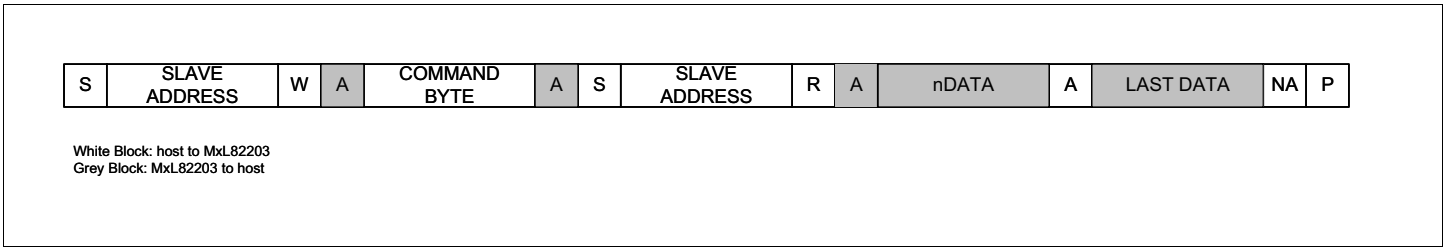


Figure 5: Master Reads From Slave

I2C-Bus Addressing

There can be different devices on the I2C-bus. To distinguish itself from the other devices on the I2C-bus, the MxL82203 has up to 16 I2C slave addresses using the A1-A0 address lines. The following table lists the different addresses that can be selected.

Table 5: I2C Address Map

A1	A0	I2C Address
SCL	GND	0x20 (0010 000X)
SCL	VCC	0x22 (0010 001X)
SDA	GND	0x24 (0010 010X)
SDA	VCC	0x26 (0010 011X)
SCL	SCL	0x30 (0011 000X)
SCL	SDA	0x32 (0011 001X)
SDA	SCL	0x34 (0011 010X)
SDA	SDA	0x36 (0011 011X)
GND	GND	0x40 (0100 000X)
GND	VCC	0x42 (0100 001X)
VCC	GND	0x44 (0100 010X)
VCC	VCC	0x46 (0100 011X)
GND	SCL	0x50 (0101 000X)
GND	SDA	0x52 (0101 001X)
VCC	SCL	0x54 (0101 010X)
VCC	SDA	0x56 (0101 011X)

I2C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is *0*, then it is a write transaction. If bit-0 is *1*, then it is a read transaction.

I2C Command Byte

An I2C command byte is sent by the I2C master following the slave address. The command byte indicates the address offset of the register that is accessed. The following table lists the command bytes for each register.

Table 6: I2C Command Byte (Register Address)

Command Byte	Register Name Description	Read/Write	Default Values
0x00	GSR1–GPIO State for P0-P7	Read-Only	0xXX
0x01	GSR2–GPIO State for P8-P15	Read-Only	0xXX
0x02	OCR1–Output Control for P0-P7	Read/Write	0xFF
0x03	OCR2–Output Control for P8-P15	Read/Write	0xFF
0x04	PIR1–Input Polarity Inversion for P0-P7	Read/Write	0x00
0x05	PIR2–Input Polarity Inversion for P8-P15	Read/Write	0x00
0x06	GCR1–GPIO Configuration for P0-P7	Read/Write	0xFF
0x07	GCR2–GPIO Configuration for P8-P15	Read/Write	0xFF
0x08	PUR1–Input Internal Pull-up Resistor Enable/Disable for P0-P7	Read/Write	0x00
0x09	PUR2–Input Internal Pull-up Resistor Enable/Disable for P8-P15	Read/Write	0x00
0x0A	IER1–Input Interrupt Enable for P0-P7	Read/Write	0x00
0x0B	IER2–Input Interrupt Enable for P8-P15	Read/Write	0x00
0x0C	TSCR1–Output Three-State Control for P0-P7	Read/Write	0x00
0x0D	TSCR2–Output Three-State Control for P8-P15	Read/Write	0x00
0x0E	ISR1–Input Interrupt Status for P0-P7	Read	0x00
0x0F	ISR2–Input Interrupt Status for P8-P15	Read	0x00
0x10	REIR1–Input Rising Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x11	REIR2–Input Rising Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x12	FEIR1–Input Falling Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x13	FEIR2–Input Falling Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x14	IFR1–Input Filter Enable/Disable for P0-P7	Read/Write	0xFF
0x15	IFR2–Input Filter Enable/Disable for P8-P15	Read/Write	0xFF

Interrupts

The following table lists the interrupt behavior of the different register settings for the MxL82203 device.

Table 7: Interrupt Generation and Clearing

GCR Bit	IER Bit	REIR Bit	FEIR Bit	IFR Bit	Interrupt Generated By	Interrupt Cleared By
1	0	X	X	X	No interrupts enabled (default).	N/A.
1	1	0	0	0	A rising or falling edge on the input.	Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR).
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
1	1	1	0	0	A rising edge on the input.	Reading the GSR register.
				1	A rising edge on the input and remains high for more than 1075ns.	
1	1	0	1	0	A falling edge on the input.	Reading the GSR register.
				1	A falling edge on the input and remains low for more than 1075ns.	
1	1	1	1	0	A rising or falling edge on the input.	Reading the GSR register.
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
0	x	x	x	x	No interrupts in output mode.	N/A

Register Description

GPIO State Register 1 (GSR1)—Read Only

The status of P7–P0 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR register). Reading this register clears an input interrupt (For complete details, see Table 7 on page 10). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (that is, this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

GPIO State Register 2 (GSR2)—Read Only

The status of P15–P8 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR register). Reading this register clears an input interrupt (For complete details, see Table 7 on page 10). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (that is, this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Output Control Register 1 (OCR1)—Read/Write

When P7–P0 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Control Register 2 (OCR2)—Read/Write

When P15–P8 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Polarity Inversion Register 1 (PIR1)—Read/Write

When P7–P0 are defined as inputs, this register inverts the polarity of the input value read from the input port register. If the corresponding bit in this register is set to *1*, the value of this bit in the GSR register is the inverted value of the input pin. If the corresponding bit in this register is set to *0*, the value of this bit in the GSR register is the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Polarity Inversion Register 2 (PIR2)—Read/Write

When P15–P8 are defined as inputs, this register inverts the polarity of the input value read from the input port register. If the corresponding bit in this register is set to *1*, the value of this bit in the GSR register is the inverted value of the input pin. If the corresponding bit in this register is set to *0*, the value of this bit in the GSR register is the actual value of the input pin. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

GPIO Configuration Register 1 (GCR1)—Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to *0* enables the GPIOs as outputs. Setting these bits to *1* enables the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

GPIO Configuration Register 2 (GCR2)—Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to *0* enables the GPIOs as outputs. Setting these bits to *1* enables the GPIOs as inputs. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Internal Pull-up Enable/Disable Register 1 (PUR1)—Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up or after reset, the internal pull-up resistors are disabled by default. Writing a ’1’ to these bits enables the internal pull-up resistors. Writing a ’0’ to these bits disables the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Internal Pull-up Enable/Disable Register 2 (PUR2)—Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up or after reset, the internal pull-up resistors are disabled by default. Writing a ’1’ to these bits enables the internal pull-up resistors. Writing a ’0’ to these bits disables the internal pull-up resistors. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Interrupt Enable Register 1 (IER1)—Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a *1* to these bits enables the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. No interrupts are generated for outputs when GCR bit is *0*. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Enable Register 2 (IER2)—Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a *1* to these bits enables the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. No interrupts are generated for outputs when GCR bit is *0*. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Output Three-State Control Register 1 (TSCR1)—Read/Write

This register can enable/disable the three-state mode of an output. Writing a *1* to these bits enables the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Three-State Control Register 2 (TSCR2)—Read/Write

This register can enable/disable the three-state mode of an output. Writing a *1* to these bits enables the three-state mode for the corresponding output pins. he MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Interrupt Status Register 1 (ISR1)—Read Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Status Register 2 (ISR2) - Read-Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Rising Edge Interrupt Enable Register 1 (REIR1) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Rising Edge Interrupt Enable Register 2 (REIR2) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Falling Edge Interrupt Enable Register 1 (FEIR1) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the falling edge. Writing a *1* to these bits makes that input generate an interrupt on the rising edge only. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Falling Edge Interrupt Enable Register 2 (FEIR2) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the falling edge. Writing a *1* to these bits makes that input generate an interrupt on the rising edge only. For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Filter Enable Register 1 (IFR1) - Read/Write

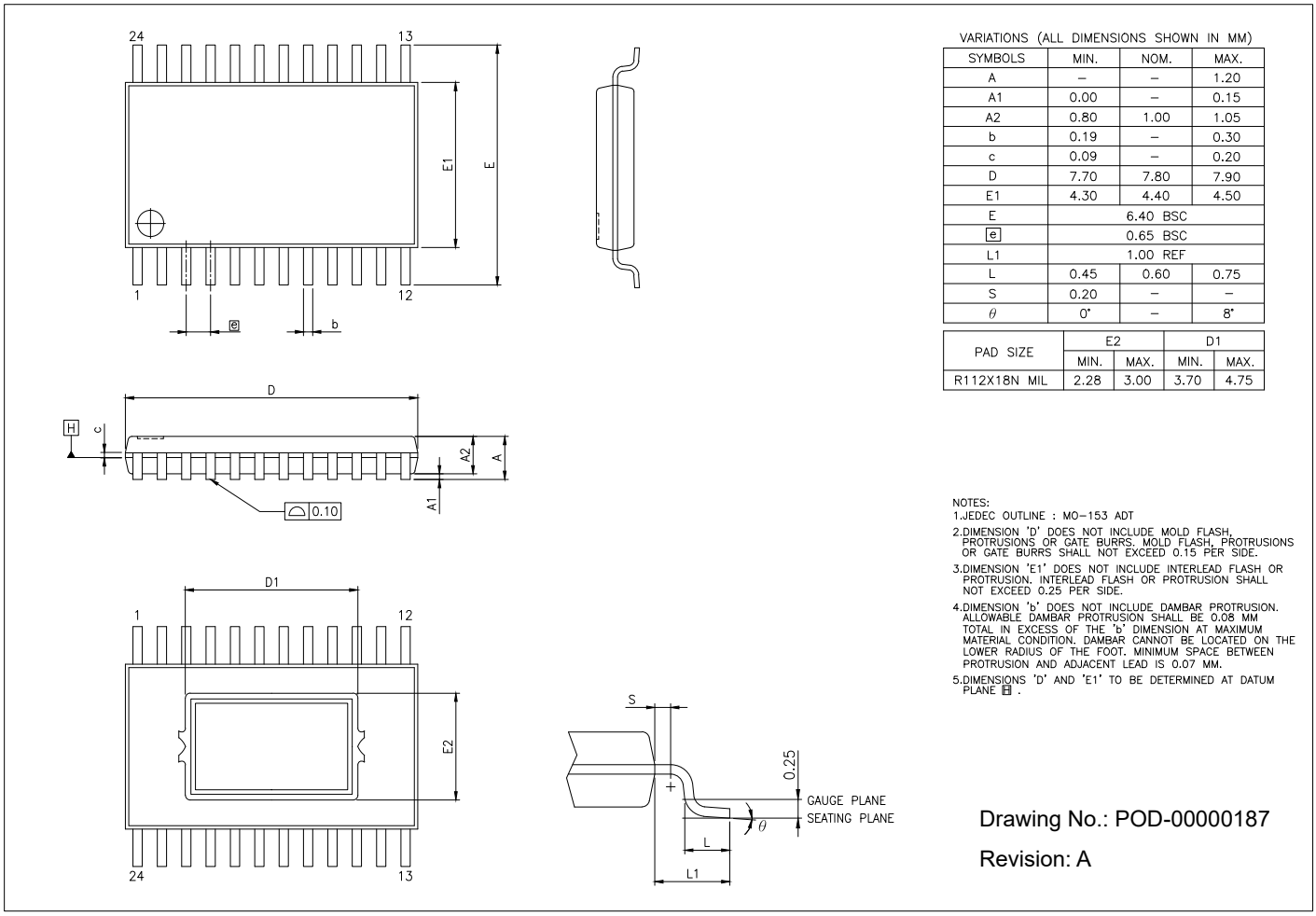
By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 225ns is filtered and do not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a *0* to these bits disables the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, For complete details, see Table 7 on page 10. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Filter Enable Register 2 (IFR2) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 225ns is filtered and is not generated an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a *0* to these bits disables the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, see Table 7 on page 10. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Mechanical Dimensions

TSSOP-24



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
R112X18N MIL	2.28	3.00	3.70	4.75

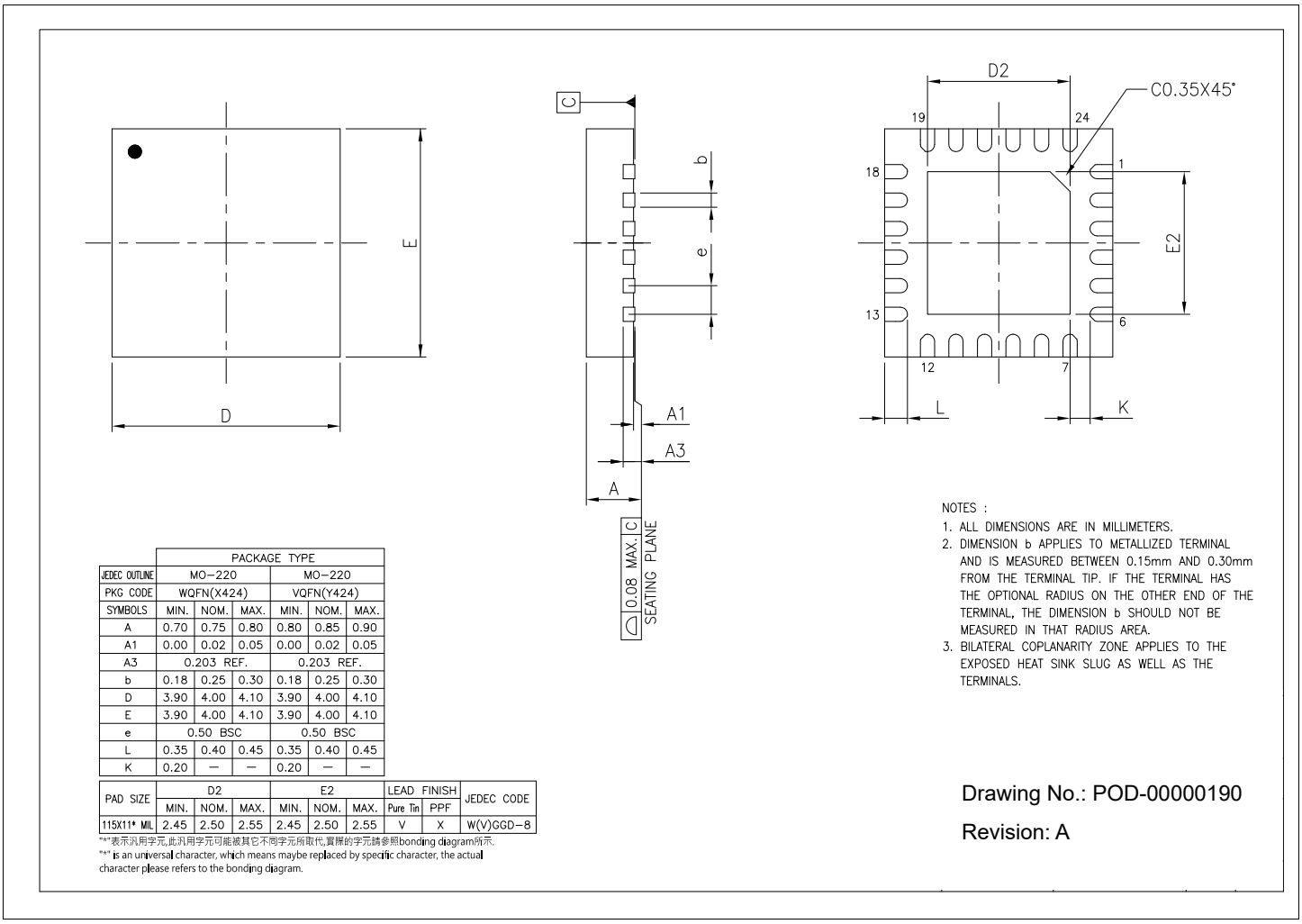
NOTES:
1. JEDEC OUTLINE : MO-153 ADT
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

Drawing No.: POD-00000187

Revision: A

Figure 6: TSSOP-24 Mechanical Dimensions

QFN-24



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10
e	0.50 BSC			0.50 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
115X11* MIL	2.45	2.50	2.55	2.45	2.50	2.55	V	X	W(V)GGD-8

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 7: QFN-24 Mechanical Dimensions

Ordering Information

Table 8: Ordering Information

Ordering Part Number	Package	Number of Channels	Operating Temperature Range	Package Method	Lead-Free
MxL82203I-AGA-R	TSSOP-24	16	–40°C to 85°C	Tape and Reel	Yes
MxL82203I-AQB-R	QFN-24	16	–40°C to 85°C	Tape and Reel	Yes

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