MxL82405

16-Bit SPI GPIO Expander with Integrated Level Shifters

Preliminary Data Sheet

General Description

The MxL82405 is an 16-bit GPIO expander with an SPI interface. After power-up, the MxL82405 has internal 100KΩ pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the MxL82405 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low, or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt behavior is configurable. It can be set to trigger on a rising edge, falling edge, or both edges. The interrupt condition is cleared either when the input returns to its original state or when the current input state is read.

The MxL82405 is available in 24-pin QFN.

Applications

- Personal digital assistants (PDA)
- Cellular phones/data devices
- Battery-operated devices
- Global Positioning System (GPS)
- Bluetooth

Features

- 1.62V to 5.5V operating voltage
- 16 General Purpose I/Os (GPIOs)
- Integrated level shifters
- Maximum stand-by current of 1μA at +1.8V
- SPI bus interface
  - SPI Clock frequency up to 26MHz
- Individually programmable inputs
  - Internal pull-up resistors
  - Polarity inversion
  - Individual interrupt enable
  - Rising edge and/or falling edge interrupt
  - Input filter
- Individually programmable outputs
  - Output level control
  - Output three-state control
- Open-drain active low interrupt output
- 3kV HBM ESD protection per *JESD22-A114F*
- 200mA latch-up performance per *JESD78B*

Revision History

Document No.	Release Date	Change Description
298DSR00	May 20, 2026	Initial preliminary release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supply Voltage	-	6	V
Supply Current	-	160	mA
Ground Current	-	200	mA
External Current Limit of each GPIO	-	25	mA
Total Current Limit for GPIO[15:8] and GPIO[7:0]	-	100	mA
Total Current Limit for GPIO[15:0]	-	200	mA
Total Supply Current sourced by all GPIOs	-	160	mA
Operating Temperature	–40	+85	°C
Storage Temperature	–65	+150	°C
Power Dissipation	-	200	mW

Electrical Characteristics

DC Electrical Characteristics

DC Electrical characteristics at V_{cc} = 1.62V to 5.5V, T_A = 40°C to +85°C, unless otherwise specified.

Table 2: DC Electrical Characteristics

Symbol	Parameter	Limits 1.8V ± 10% Min	Limits 1.8V ± 10% Max	Limits 2.5V ± 10% Min	Limits 2.5V ± 10% Max	Limits 3.3V ± 10% Min	Limits 3.3V ± 10% Max	Limits 5.0V ± 10% Min	Limits 5.0V ± 10% Max	Units	Conditions
V_{IL}	Input Low Voltage	–0.3	0.2	–0.3	0.5	–0.3	0.8	-	0.3×VCC	V	Note 1
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	0.7×VCC	5.5	0.7×VCC	-	V	Note 1
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	-	0.4	V V V	I_{OL} = 1.5mA I_{OL} = 4mA I_{OL} = 6mA Note 2 and Note 4
V_{OL}	Output Low Voltage	-	0.5	-	0.5		0.5	-	0.5	V	I_{OL} = 8mA Note 3
V_{OH}	Output High Voltage	1.4	-	1.8	-	2.0	-	2.0	-	V V V	I_{OL} = –0.2mA I_{OL} = –2mA I_{OL} = –4mA Note 2
V_{OH}	Output High Voltage	1.2	-	1.8	-	2.6	-	4.1	-	V	I_{OH} = –8mA Note 3
I_{IL}	Input Low Leakage Current	-	±10	-	±10	-	±10	-	±10	µA	-
I_{IH}	Input High Leakage Current	-	±10	-	±10	-	±10	-	±10	µA	-
C_{IN}	Input Pin Capacitance	-	5	-	5	-	5	-	5	pF	-
I_{CC}	Power Supply Current	-	0.5	-	1.0	-	2.0	-	4	µA	Note 5
I_{CC}	Power Supply Current	-	0.6	-	1.2	-	2.4	-	5	µA	Note 6
I_{CCS}	Standby Current	-	1	-	2	-	5	-	7	µA	Note 7
R_{GPIO}	GPIO Pull-up Resistance	60	140	60	140	60	140	60	140	kΩ	100kΩ ±40%
$R_{RESET\#}$	Reset# Pull-up Resistance	30	85	35	85	35	85	35	85	kΩ	60kΩ ±40%

Note: The V_{CC} comes from VCCP pin for the GPIOs and the VCC pin for the other signals

1. For SPI input signals (SI, SCK) AND GPIOs, A0, A1, and A2 signals.
2. For SPI output signal SO.
3. For GPIOs.
4. For IRQ# signal.
5. Test 1: SCL frequency is 10MHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.
6. Test 2: SCL frequency is 10MHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.
7. Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. SCL, and SI are at GND. CS# is at VCC. All GPIOs are configured as inputs. Outputs are left floating or in tri-state mode.

AC Electrical Characteristics

AC Electrical characteristics at V_{cc} = 1.62V to 5.5V, T_A = 40°C to +85°C, unless otherwise specified.

Table 3: AC Electrical Characteristics

Symbol	Parameter	Limits 1.8V±10%			Limits 2.5V±10%			Limits 3.3V±10%			Limits 5V±10%			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{SCL}	Operating Frequency	-	-	15	-	-	26	-	-	26	-	-	26	MHz	
T_{CSS}	CS# to SCL Setup Time	20	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{CSH}	CS# to SCL Hold Time	20	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{DO}	SCL Fall to SO Valid Time	-	-	30	-	-	17	-	-	17	-	-	17	ns	C_L = 30 pF
T_{DS}	SI to SCL Setup Time	20	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{DH}	SI to SCL Hold Time	20	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{CP}	SCL Period	66	-	-	38	-	-	38	-	-	38	-	-	ns	T_{CH} + T_{CL}
T_{CH}	SCL HIGH Time	35	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{CL}	SCL LOW Time	35	-	-	20	-	-	20	-	-	20	-	-	ns	
T_{CSW}	CS# HIGH Pulse Width	30	-	-	30	-	-	30	-	-	30	-	-	ns	
T_{D9}	SPI Output Data Valid Time	-	10	-	-	10	-	-	10	-	-	10	-	ns	
T_{D13}	SPI Input Pin Interrupt Clear	-	-	200	-	-	200	-	-	200	-	-	200	ns	

Timing Diagrams

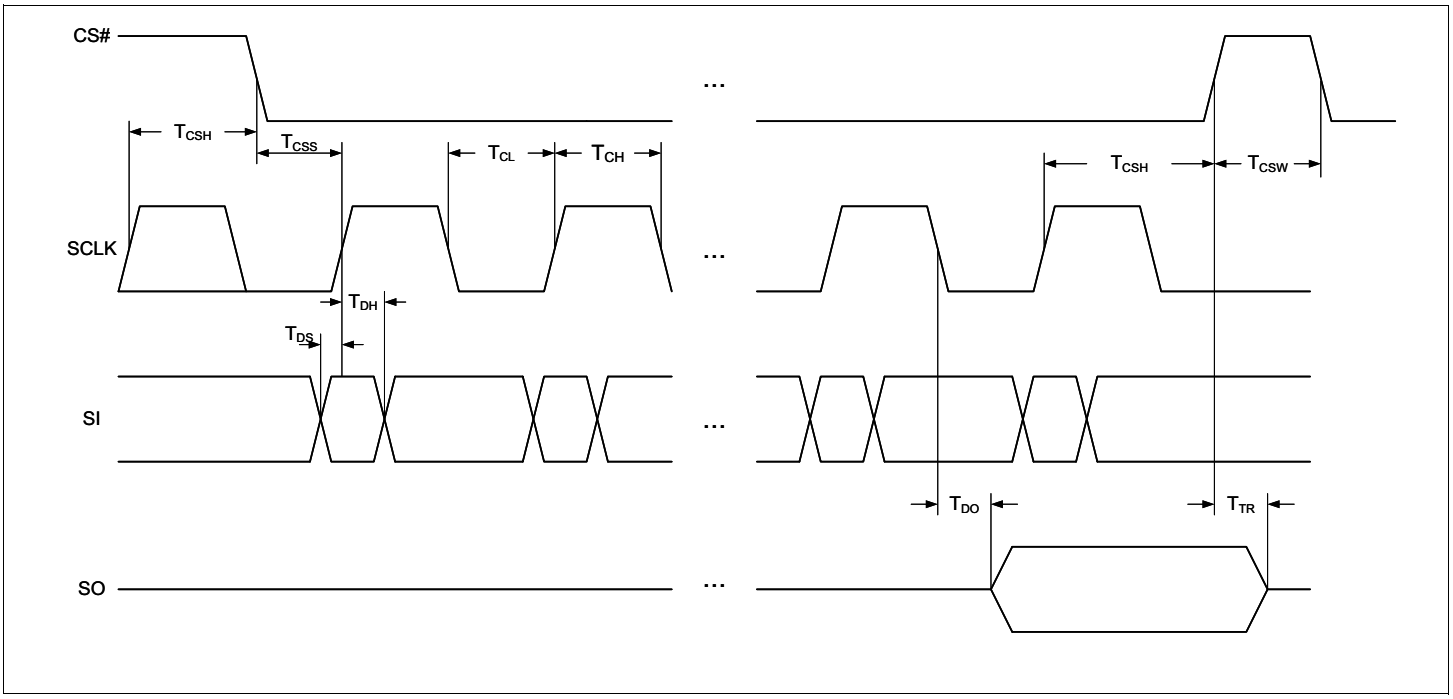


Figure 1: SPI-Bus Timing

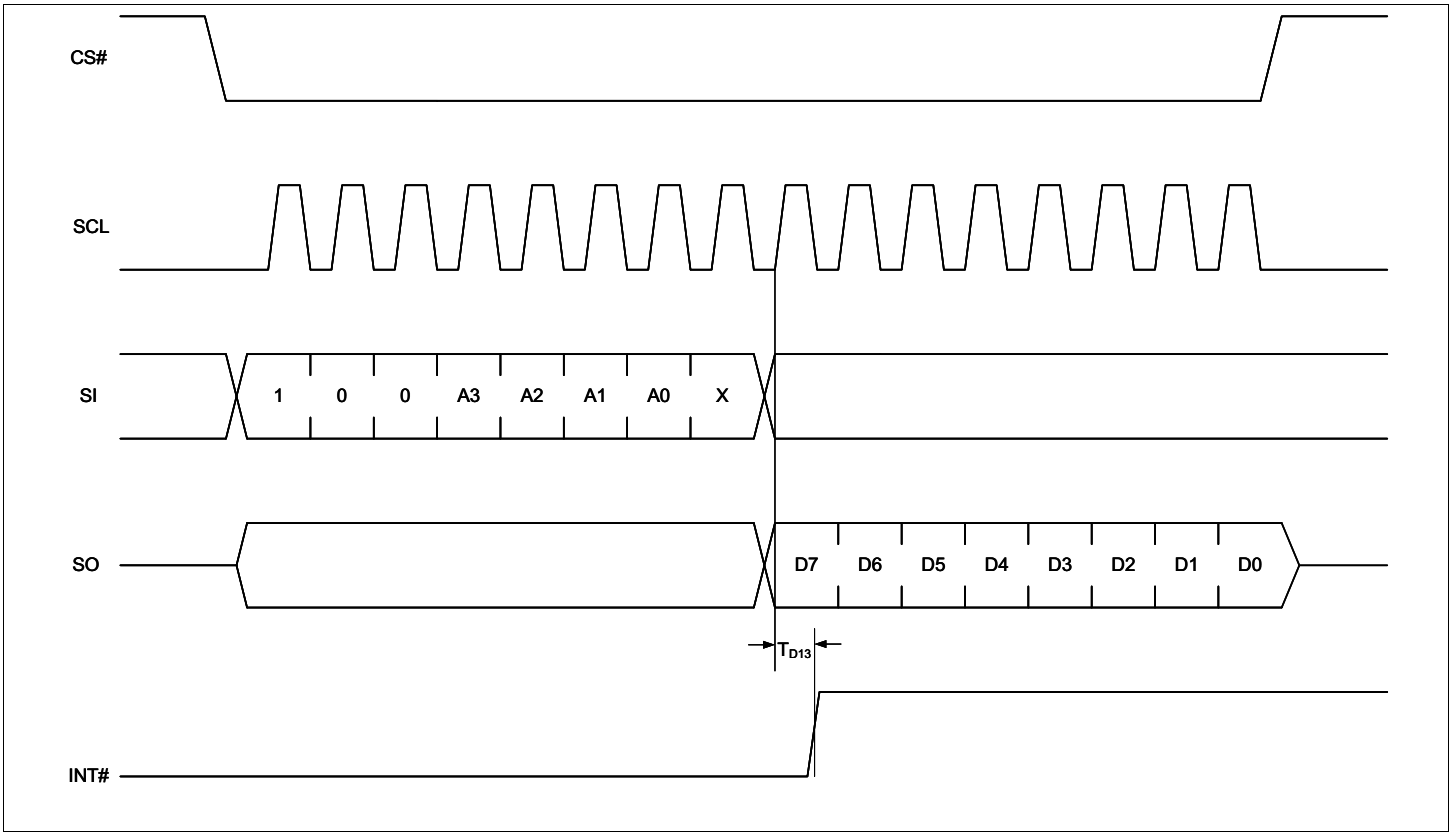


Figure 2: Read Input Port to Clear GPIO INT

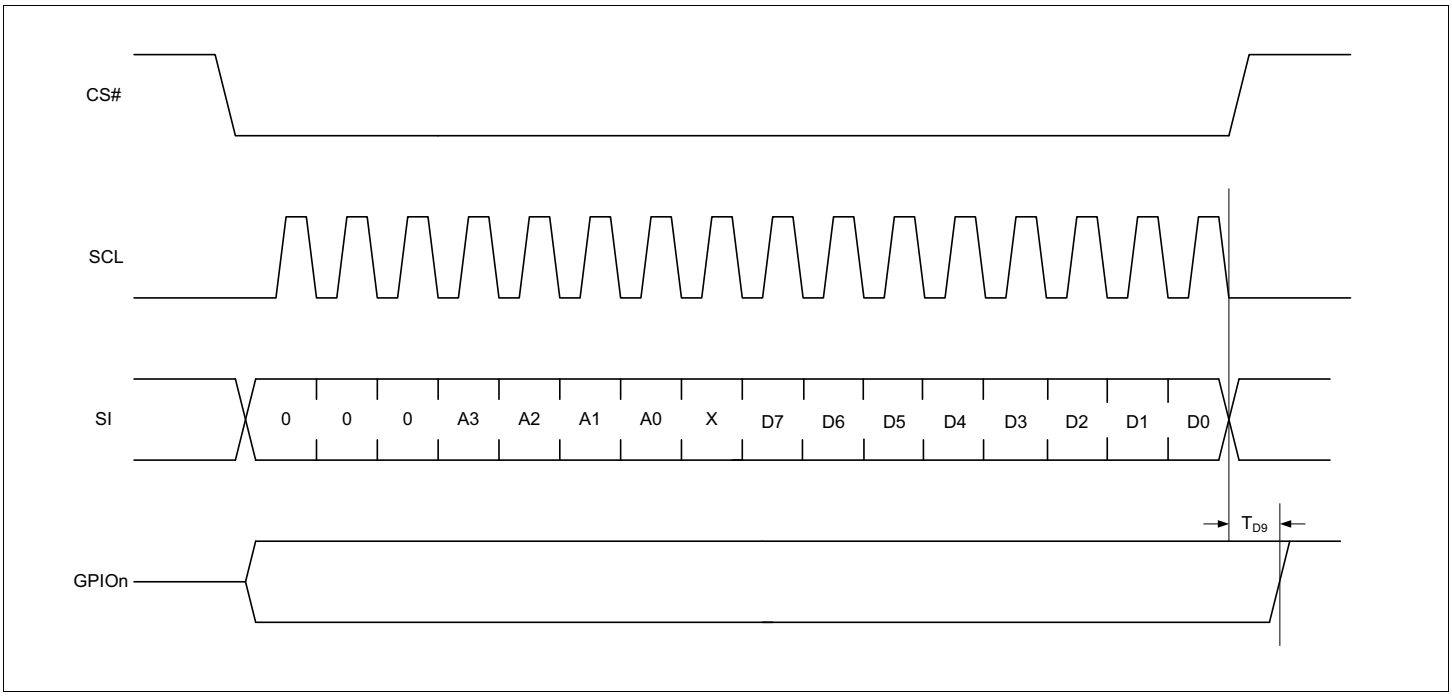


Figure 3: SPI Write out to GPIO Switch

Pin Information

Pin Configuration

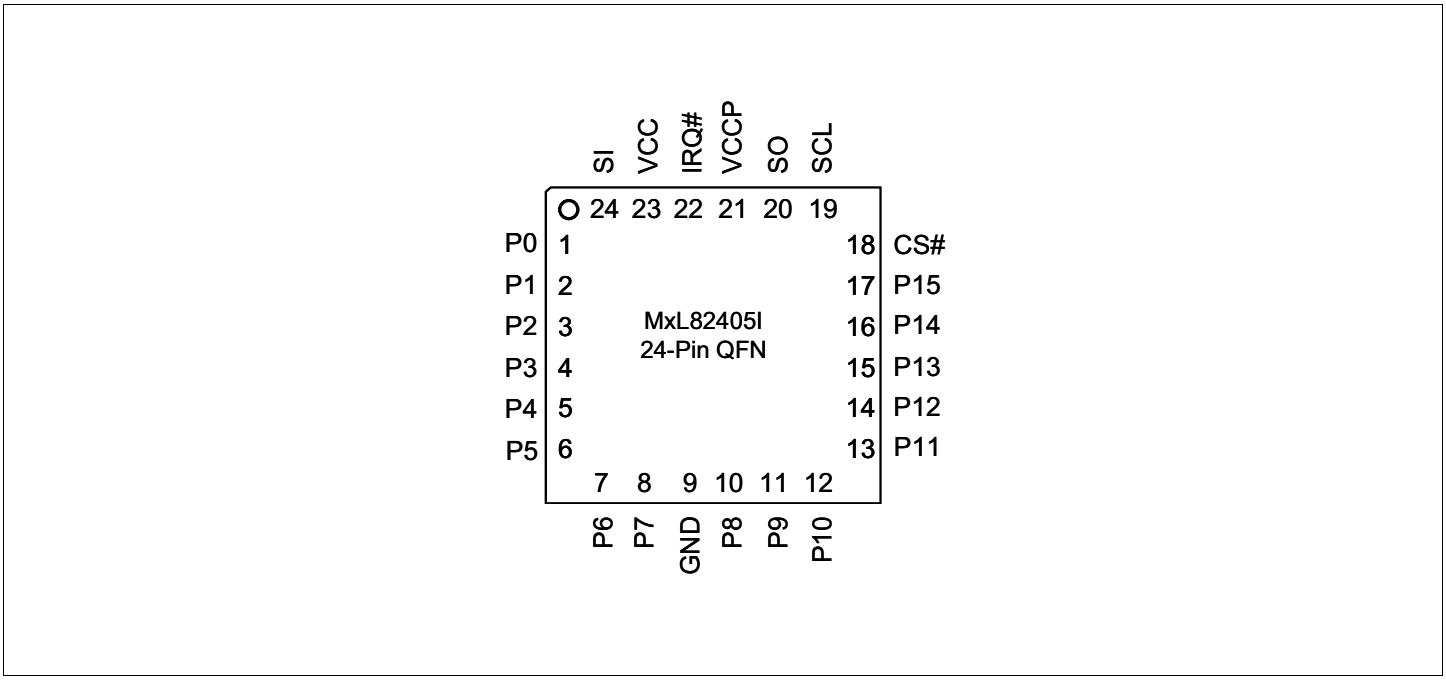


Figure 4: Pinout (Top View)

Pin Description

Table 4: Pin Description

Pin Name	QFN-24 PIN#	Type	Description
SPI Interface			
SO	20	O	SPI serial data output.
SCL	19	I	SPI bus serial input clock.
IRQ#	22	OD	Interrupt output (open-drain, active low).
CS#	18	I	SPI bus chip select.
SI	24	I	SPI serial data input.
GPIOs			
P0	1	I/O	General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up.
P1	2	I/O	
P2	3	I/O	
P3	4	I/O	
P4	5	I/O	
P5	6	I/O	
P6	7	I/O	
P7	8	I/O	

Table 4: Pin Description

Pin Name	QFN-24 PIN#	Type	Description
P8	10	I/O	General purpose I/O P8-P15. All GPIOs are configured as inputs upon power-up.
P9	11	I/O	
P10	12	I/O	
P11	13	I/O	
P12	14	I/O	
P13	15	I/O	
P14	16	I/O	
P15	17	I/O	
Ancillary Signals			
VCCP	21		1.62V to 5.5V VCC supply voltage for GPIOs.
VCC	23	Pwr	1.62V to 5.5V VCC supply voltage for SPI bus interface.
GND	9	Pwr	Power supply common, ground.
GND	Center Pad	Pwr	The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential.

Note: Pin type: I = Input, O = Output, I/O = Input/output, OD = Output Open Drain.

Block Diagram

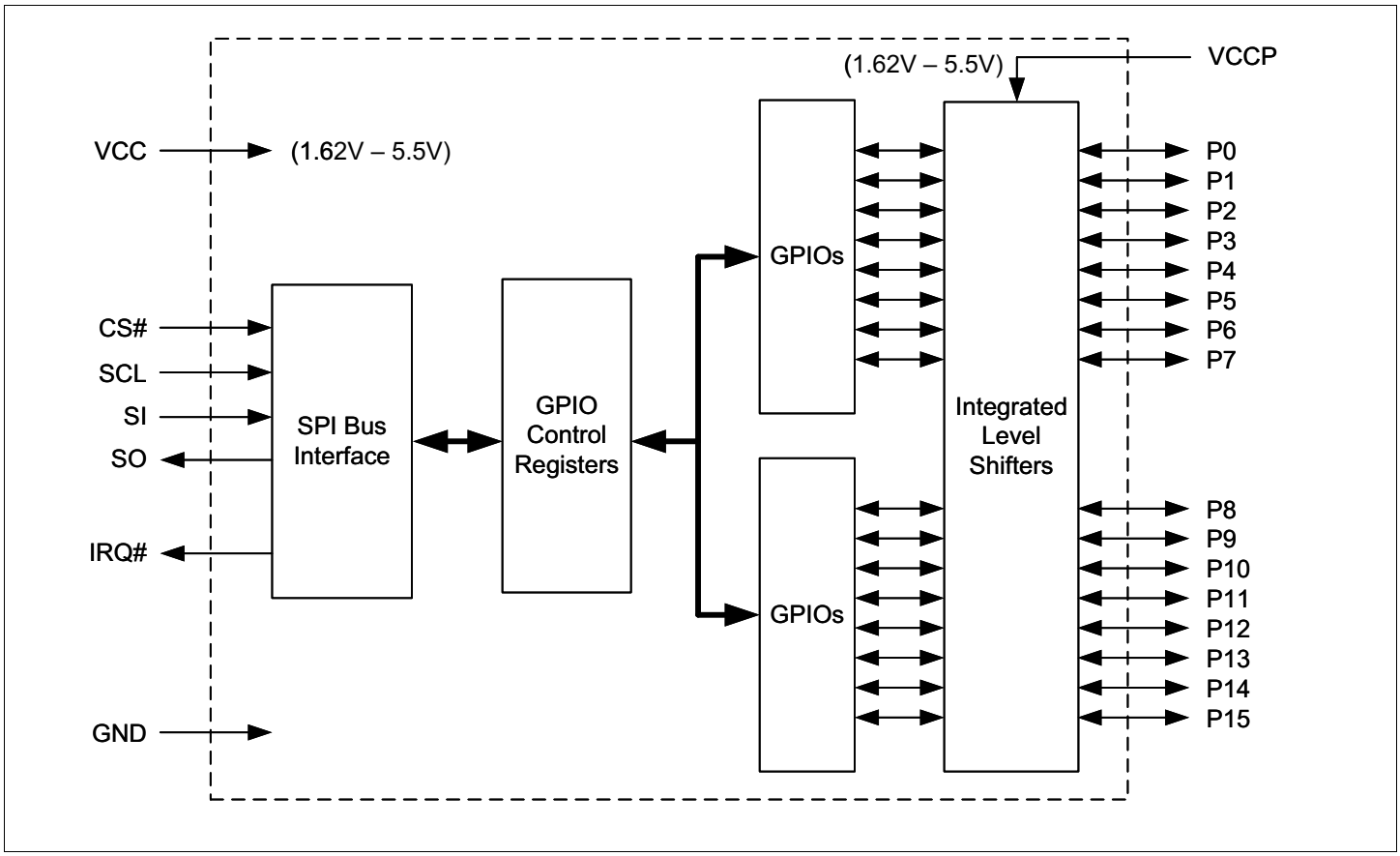


Figure 5: Functional Block Diagram

Functional Description

SPI Bus Interface

The SPI interface consists of four lines: serial clock (SCL), chip select (CS#), slave output (SO), and slave input (SI). The serial clock, slave output, and slave input can be as fast as 26MHz.To access the device in the SPI mode, the CS# signal is asserted by the SPI master, then the SPI master starts toggling the SCL signal with the appropriate transaction information. The first bit sent by the SPI master includes whether it is a read or write transaction and the register being accessed. See the following table.

Table 5: SPI Command Byte Format

Bit	Function
7	Read/Write# Logic 1 = Read Logic 0 = Write
6.1	Command Byte
0	Reserved

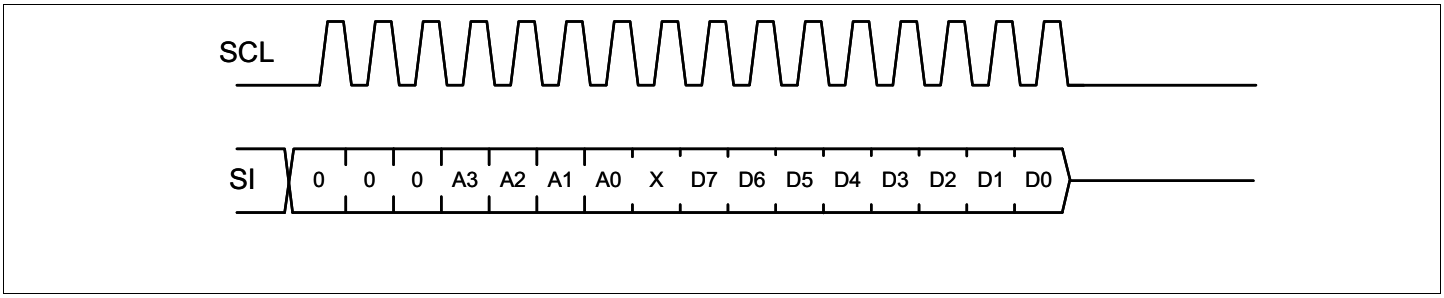


Figure 6: SPI Write

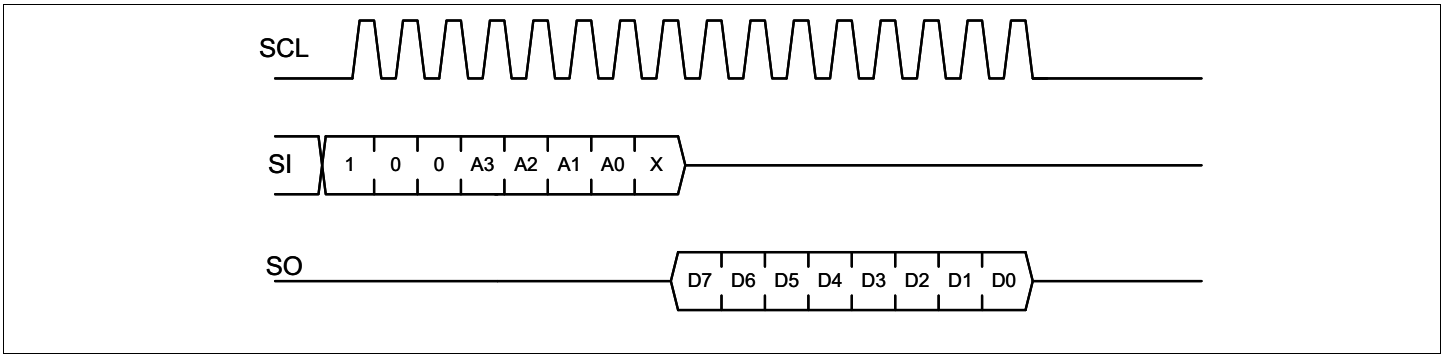


Figure 7: SPI Read

After the last read or write transaction, the SPI master sets the SCL signal back to its idle state (low).

SPI Command Byte

An SPI command byte is sent by the SPI master following the slave address. The command byte indicates the address offset of the register that will be accessed. The following table lists the command bytes for each register.

Table 6: SPI Command Byte (Register Address)

Command Byte	Register Name Description	Read/Write	Default Values
0x00	GSR1–GPIO State for P0-P7	Read-Only	0xXX
0x01	GSR2–GPIO State for P8-P15	Read-Only	0xXX
0x02	OCR1–Output Control for P0-P7	Read/Write	0xFF
0x03	OCR2–Output Control for P8-P15	Read/Write	0xFF
0x04	PIR1–Input Polarity Inversion for P0-P7	Read/Write	0x00
0x05	PIR2–Input Polarity Inversion for P8-P15	Read/Write	0x00
0x06	GCR1–GPIO Configuration for P0-P7	Read/Write	0xFF
0x07	GCR2–GPIO Configuration for P8-P15	Read/Write	0xFF
0x08	PUR1–Input Internal Pull-up Resistor Enable/Disable for P0-P7	Read/Write	0x00
0x09	PUR2–Input Internal Pull-up Resistor Enable/Disable for P8-P15	Read/Write	0x00
0x0A	IER1–Input Interrupt Enable for P0-P7	Read/Write	0x00
0x0B	IER2–Input Interrupt Enable for P8-P15	Read/Write	0x00
0x0C	TSCR1–Output Three-State Control for P0-P7	Read/Write	0x00
0x0D	TSCR2–Output Three-State Control for P8-P15	Read/Write	0x00
0x0E	ISR1–Input Interrupt Status for P0-P7	Read	0x00
0x0F	ISR2–Input Interrupt Status for P8-P15	Read	0x00
0x10	REIR1–Input Rising Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x11	REIR2–Input Rising Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x12	FEIR1–Input Falling Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x13	FEIR2–Input Falling Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x14	IFR1–Input Filter Enable/Disable for P0-P7	Read/Write	0xFF
0x15	IFR2–Input Filter Enable/Disable for P8-P15	Read/Write	0xFF

Interrupts

The following table lists the interrupt behavior of the different register settings for the MxL82405 device.

Table 7: Interrupt Generation and Clearing

GCR Bit	IER Bit	REIR Bit	FEIR Bit	IFR Bit	Interrupt Generated By	Interrupt Cleared By
1	0	X	X	X	No interrupts enabled (default).	N/A
1	1	0	0	0	A rising or falling edge on the input.	Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR)
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
1	1	1	0	0	A rising edge on the input.	Reading the GSR register.
				1	A rising edge on the input and remains high for more than 1075ns.	
1	1	0	1	0	A falling edge on the input.	Reading the GSR register.
				1	A falling edge on the input and remains low for more than 1075ns.	
1	1	1	1	0	A rising or falling edge on the input.	Reading the GSR register.
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
0	x	x	x	x	No interrupts in output mode.	N/A

Register Description

GPIO State Register 1 (GSR1)—Read Only

The status of P7–P0 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR register). Reading this register clears an input interrupt (For complete details, see Table 7 on page 11). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (that is, this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

GPIO State Register 2 (GSR2)—Read Only

The status of P15–P8 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR register). Reading this register clears an input interrupt (For complete details, see Table 7 on page 11). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (that is, this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Output Control Register 1 (OCR1)—Read/Write

When P7–P0 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Control Register 2 (OCR2)—Read/Write

When P15–P8 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Polarity Inversion Register 1 (PIR1)—Read/Write

When P7–P0 are defined as inputs, this register inverts the polarity of the input value read from the input port register. If the corresponding bit in this register is set to *1*, the value of this bit in the GSR register is the inverted value of the input pin. If the corresponding bit in this register is set to *0*, the value of this bit in the GSR register is the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Polarity Inversion Register 2 (PIR2)—Read/Write

When P15–P8 are defined as inputs, this register inverts the polarity of the input value read from the input port register. If the corresponding bit in this register is set to *1*, the value of this bit in the GSR register is the inverted value of the input pin. If the corresponding bit in this register is set to *0*, the value of this bit in the GSR register is the actual value of the input pin. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

GPIO Configuration Register 1 (GCR1)—Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to *0* enables the GPIOs as outputs. Setting these bits to *1* enables the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

GPIO Configuration Register 2 (GCR2)—Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to *0* enables the GPIOs as outputs. Setting these bits to *1* enables the GPIOs as inputs. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Internal Pull-up Enable/Disable Register 1 (PUR1)—Read/Write

This register enables/disables the internal pull-up resistors for an input. Upon power-up, the internal pull-up resistors are isabled by default. Writing a ’1’ to these bits will enable the internal pull-up resistors. Writing a ’0’ to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Internal Pull-up Enable/Disable Register 2 (PUR2)—Read/Write

This register enables/disables the internal pull-up resistors for an input. Upon power-up, the internal pull-up resistors are disabled by default. Writing a ’1’ to these bits will enable the internal pull-up resistors. Writing a ’0’ to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Interrupt Enable Register 1 (IER1)—Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a *1* to these bits enables the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. No interrupts are generated for outputs when GCR bit is *0*. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Enable Register 2 (IER2)—Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a *1* to these bits enables the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. No interrupts are generated for outputs when GCR bit is *0*. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Output Three-State Control Register 1 (TSCR1)—Read/Write

This register can enable/disable the three-state mode of an output. Writing a *1* to these bits enables the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Three-State Control Register 2 (TSCR2)—Read/Write

This register can enable/disable the three-state mode of an output. Writing a *1* to these bits enables the three-state mode for the corresponding output pins. he MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Interrupt Status Register 1 (ISR1)—Read Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Status Register 2 (ISR2) - Read-Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Rising Edge Interrupt Enable Register 1 (REIR1) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Rising Edge Interrupt Enable Register 2 (REIR2) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Falling Edge Interrupt Enable Register 1 (FEIR1) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the falling edge. Writing a *1* to these bits makes that input generate an interrupt on the rising edge only. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Falling Edge Interrupt Enable Register 2 (FEIR2) - Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the falling edge. Writing a *1* to these bits makes that input generate an interrupt on the rising edge only. For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Input Filter Enable Register 1 (IFR1) - Read/Write

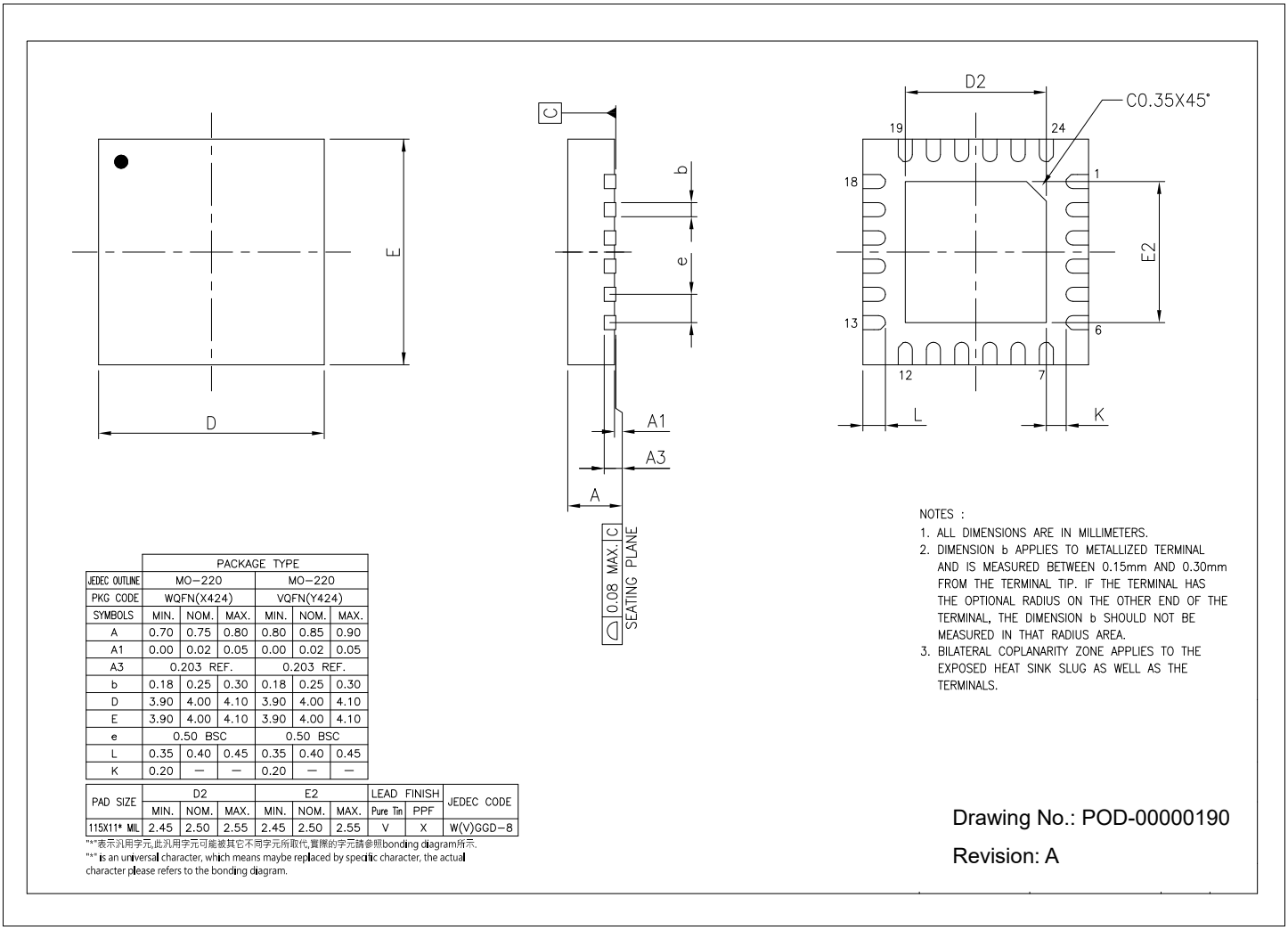
By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 225ns is filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a *0* to these bits disables the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, For complete details, see Table 7 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Filter Enable Register 2 (IFR2) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 225ns is filtered and is not generated an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a *0* to these bits disables the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, see Table 7 on page 11. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

Mechanical Dimensions

QFN-24



JEDEC OUTLINE	PACKAGE TYPE					
	MO−220			MO−220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10
e	0.50 BSC			0.50 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
115X11* MIL	2.45	2.50	2.55	2.45	2.50	2.55	V	X	W(V)GGD−8

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 8: QFN-24 Mechanical Dimensions

Ordering Information

Table 8: Ordering Information

Ordering PN	Package	Operating Temperature Range	Package Method	Lead-Free	Description
MXL82405I-AQB-R	QFNL/QFN-24	–40°C to 85°C	Tape and Reel	Yes	16-bit SPI GPIO Expander with level shift

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