GENERAL DESCRIPTION

The XR19L400 (L400) is a highly integrated device that combines a full-featured single channel Universal Asynchronous Receiver and Transmitter (UART) and RS-485 transceivers. The L400 is designed to operate with a single 3.3V or 5V power supply. The L400 is fully compliant with RS-485 Standards.

The L400 operates in four different modes: Active, Partial Sleep, Full Sleep and Power-Save. Each mode can be invoked via hardware or software. Upon power-up, the L400 is in the Active mode where the UART and RS-485 transceiver function normally. In the Partial Sleep mode, the internal crystal oscillator of the UART or charge pump of the RS-485 transceiver is turned off. In Full Sleep mode, both the crystal oscillator and the charge pump are turned off. While the UART is in the Sleep mode, the Power-Save mode isolates the core logic from the control signals (chip select, read/write strobes, address and data bus lines) to minimize the power consumption. The RS-485 receivers remain active in any of these four modes.

APPLICATIONS

- Battery-Powered Equipment
- Handheld and Mobile Devices
- Handheld Terminals
- Industrial Peripheral Interfaces
- Point-of-Sale (POS) Systems

FEATURES

- Meets true RS-485 standards at 3.3V or 5V operation
- Up to 8 Mbps data transmission rate
- 45us sleep mode exit (charge pump to full power)
- ESD protection for RS-485 I/O pins at
  - +/-15kV - Human Body Model
  - +/- 8kV - IEC 61000-4-2, Contact Discharge
  - +/- 15kV - IEC 61000-4-2, Air-Gap Discharge
- Software compatible with industry standard 16550 UART
- Intel/Motorola bus select
- Complete modem interface
- Sleep and Power-save modes to conserve battery power
- Wake-up interrupt upon exiting low power modes

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 1. BLOCK DIAGRAM

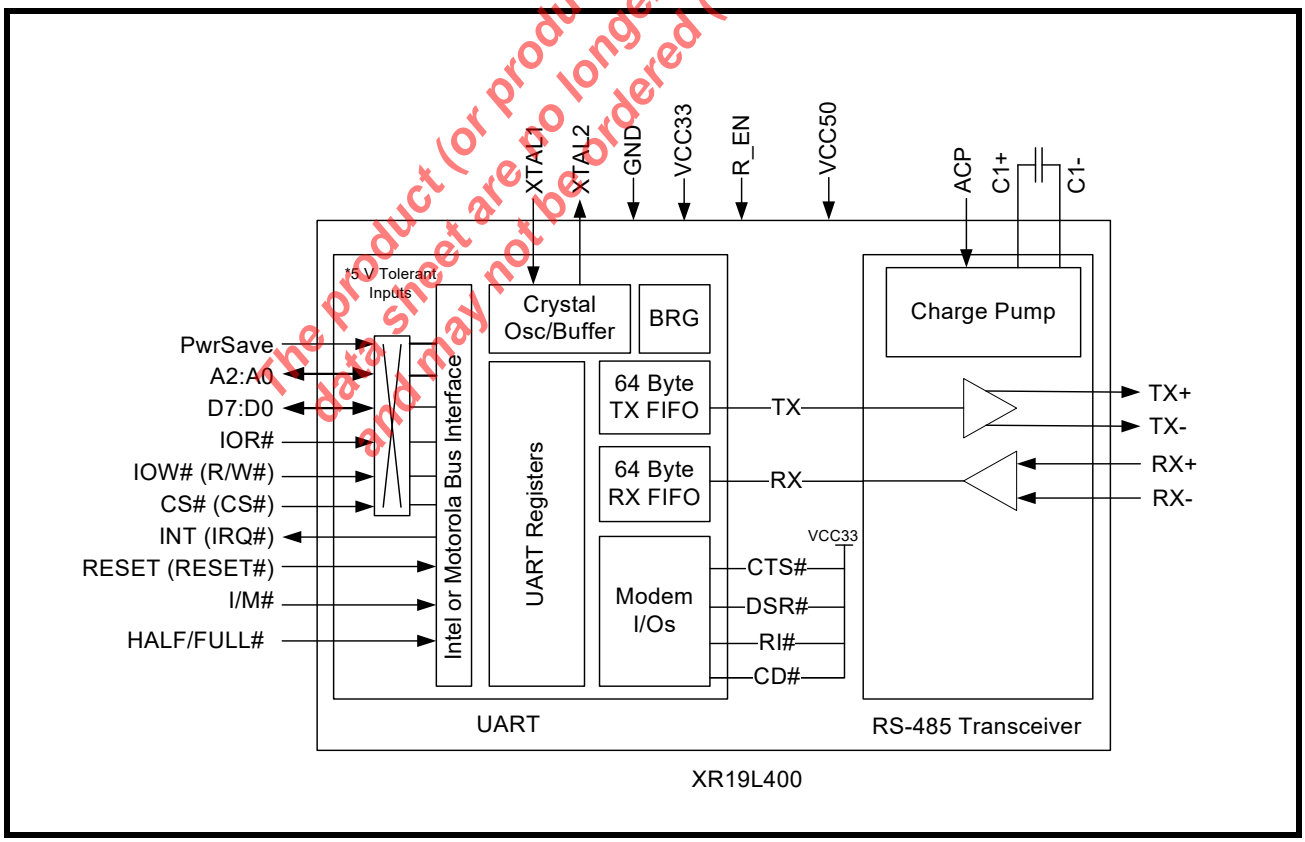
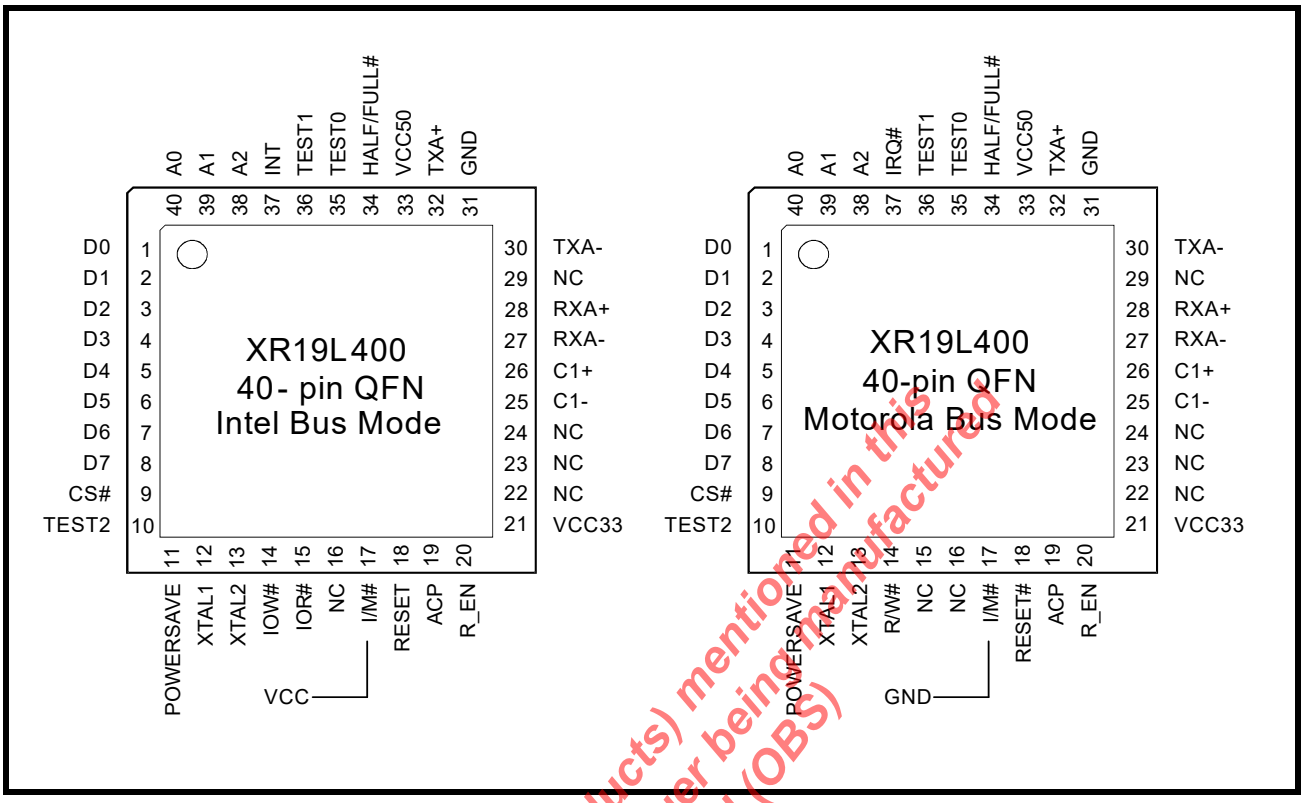


FIGURE 2. PIN OUT OF THE DEVICE



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ORDERING INFORMATION[1]

PART NUMBER	OPERATING TEMPERATURE RANGE	LEAD-FREE	PACKAGE	PACKAGING METHOD
XR19L400IL40TR-F	-40°C to +85°C	Yes[2]	40-pin QFN	Tape and Reel

NOTES:

1. *Refer to www.exar.com/XR19L400 for most up-to-date Ordering Information.*
2. *Visit www.exar.com for additional information on Environmental Rating.*

PIN DESCRIPTIONS

Pin Descriptions

NAME	40-QFN PIN#	TYPE	DESCRIPTION
DATA BUS INTERFACE (CMOS/TTL Voltage Levels)			
A2 A1 A0	38 39 40	I	Address bus lines [2:0]. These 3 address lines select one of the internal registers in the UART during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	8 7 6 5 4 3 2 1	I/O	Data bus lines [7:0] (bidirectional).
IOR# (NC)	15	I	When I/M# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active LOW). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When I/M# pin is LOW, the Motorola bus interface is selected and this input is not used.
IOW# (R/W#)	14	I	When I/M# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active LOW). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When I/M# pin is LOW, the Motorola bus interface is selected and this input becomes read (HIGH) and write (LOW) signal.
CS# (CS#)	9	I	This input is the chip select (active low) for the UART in both the Intel and Motorola bus modes.
INT (IRQ#)	37	O (OD)	When I/M# pin is HIGH, it selects Intel bus interface and this output become the active HIGH interrupt output. This output is enabled through the software setting of MCR[3]. This output is set to the active mode when MCR[3] is set to a logic 1, and set to the three state mode when MCR[3] is set to a logic 0. See MCR[3]. When I/M# pin is LOW, it selects Motorola bus interface and this output becomes the active LOW, open-drain interrupt output for both channels. An external pull-up resistor is required for proper operation. MCR[3] must be set to a logic 0 for proper operation of the interrupt.
SERIAL I/O INTERFACE (RS-485/RS-485 Voltage Levels)			
TX+ TX-	32 30	O	Differential UART Transmit Data.
RX+ RX-	28 27	I	Differential UART Receive Data.
ANCILLARY SIGNALS (CMOS/TTL Voltage Levels)			
HALF/ FULL#	34	I	Half-duplex or full-duplex mode select. This pin is sampled upon power-up. When HALF/FULL# is HIGH, half-duplex mode is enabled. When HALF/FULL# is LOW, full-duplex mode is enabled. After power-up, FCTR bit-3 can select between the half-duplex or full-duplex modes.
XTAL1	12	I	Crystal or external clock input.

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Pin Descriptions

NAME	40-QFN PIN#	TYPE	DESCRIPTION
XTAL2	13	O	Crystal or buffered clock output.
PwrSave	11	I	Power-Save (active high). This feature isolates the L400's data bus interface from the host preventing other bus activities that cause higher power drain during sleep mode.
ACP	19	I	Autosleep for Charge Pump (active HIGH). When the power supply is 3.3V, this pin shuts off the charge pump if the UART is already in sleep mode, i.e. the XTAL2 output is LOW. When the power supply is 5V, this pin should be connected to GND.
I/M#	17	I	Intel or Motorola Bus Select. When I/M# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When I/M# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.
RESET (RESET#)	18	I	When I/M# pin is HIGH for Intel bus interface, this input becomes RESET (active high). When I/M# pin is LOW for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs of the UART. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period.
C1- C1+	25 26	-	Charge pump capacitors. As shown in Figure 1, a 0.22 uF capacitor should be placed between these 2 pins.
R_EN	20	I	Regulator Enable. This pin regulates the 5V VCC down to 3.3V internally for the UART. When the supply voltage is 3.3V, connect R_EN to GND. When the supply voltage is 5V, connect R_EN to VCC.
TEST0 TEST1 TEST2	35 36 10	I I I	Factory Test Modes. For normal operation, these pins must be connected to GND.
VCC33	21	Pwr	3.3V power supply. When VCC33 is used, R_EN pin should be connected to GND. A 0.1 uF capacitor to GND is recommended on this power supply pin. If VCC33 is not used as the power supply pin, VCC33 should be left unconnected. See Figure 3. All CMOS/TTL input pins, except XTAL1, are 5V tolerant.
VCC50	33	Pwr	5.0V power supply. When VCC50 is used, R_EN pin should be connected to VCC. A 1uF capacitor to GND is recommended on the VCC50 power supply pin. The 1uF capacitor is recommended whether VCC33 or VCC50 is used as the power supply pin. See Figure 3. All CMOS/TTL input pins, except XTAL1, are 5V tolerant.
GND	31	Pwr	Power supply common, ground.
-	PAD	Pwr	The center pad on the backside of the QFN package is metallic and is not electrically connected to anything inside the device. It must be soldered on to the PCB and may be optionally connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
NC	16, 22, 23, 24, 29	-	No Connect. Note that in Motorola mode, the IOR# pin also becomes an NC pin.

NOTE: *Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain. For CMOS/TTL Voltage levels, 'LOW' indicates a voltage in the range 0V to VIL and 'HIGH" indicates a voltage in the range VIH to VCC.*

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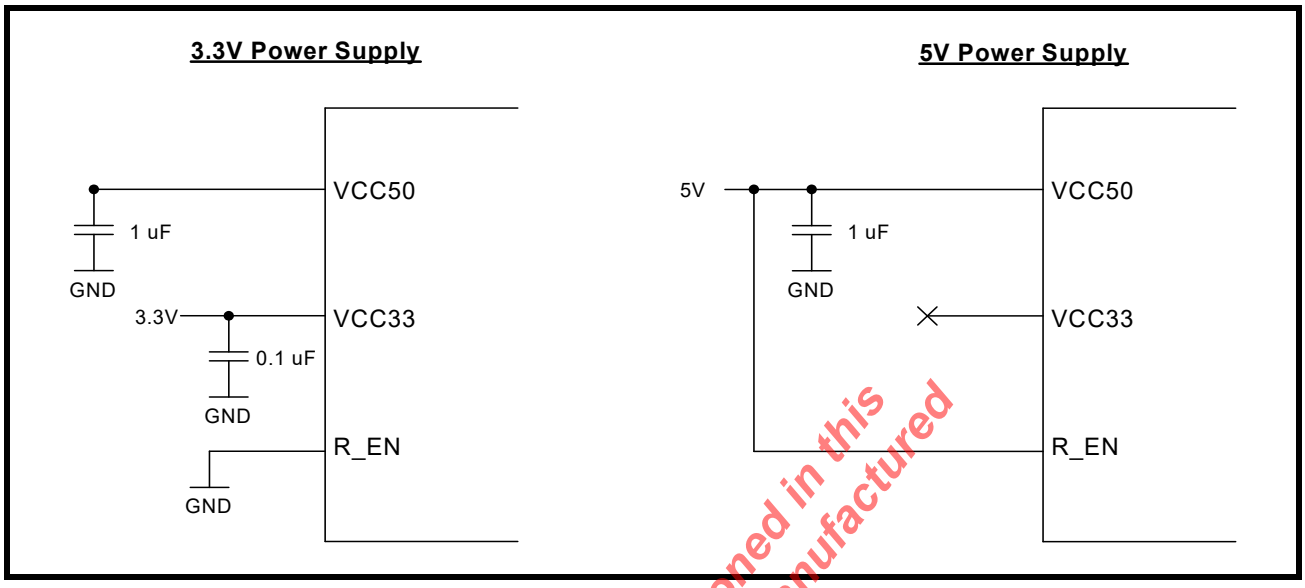
FIGURE 3. RECOMMENDED 3.3V OR 5V POWER SUPPLY CONNECTIONS



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1.0 PRODUCT DESCRIPTION

The XR19L400 consists of a single channel UART and RS-485 transceivers. It operates from a single +3.3V or 5V supply with data rates up to 8Mbps, while meeting all EIA/TIA-485 specifications. The configuration register set is 16550 UART compatible for control, status and data transfer. Also, the L400 has 64-bytes of transmit and receive FIFOs, automatic Xon/Xoff software flow control, transmit and receive FIFO trigger levels, and a programmable fractional baud rate generator with a prescaler of divide by 1 or 4. Additionally, the L400 includes the ACP pin which the user can shut down the charge pump for the RS-485 drivers (when operating at 3.3V). In the UART portion, the Power-Save feature isolates the databus interface to further reduce power consumption in the Sleep mode. The L400 is fabricated using an advanced CMOS process.

Enhanced Features

The L400 UART provides a solution that supports 64 bytes of transmit and receive FIFO. Increased performance is realized in the L400 by the transmit and receive FIFOs, FIFO trigger level controls and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the L400 provides the ACP and Power-Save modes that drastically reduces the power consumption when the device is not used. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Intel or Motorola Data Bus Interface

The L400 provides a host interface that supports Intel or Motorola microprocessor (CPU) data bus interface. The Intel bus compatible interface allows direct interconnect to Intel compatible type of CPUs using IOR#, IOW# and CS# inputs for data bus operation. The Motorola bus compatible interface instead uses the R/W# and CS# signals for data bus transactions. See pin description section for details on all the control signals. The Intel and Motorola bus interface selection is made through the pin, I/M#.

Data Rate

The L400 is capable of operation up to 8 Mbps data rate. The device can operate either with a crystal on pins XTAL1 and XTAL2, or external clock source on XTAL1 pin.

Internal Enhanced Register Sets

The L400 UART has a set of enhanced registers providing control and monitoring functions. Interrupt enable/disable and status, FIFO enable/disable, selectable TX and RX FIFO trigger levels, automatic hardware/software flow control enable/disable, programmable baud rates, modem interface controls and status, sleep mode and infrared mode are all standard features.

RS-485 Interface

The L400 includes RS-485 drivers/receivers for the interface. This feature eliminates the need for an external RS-485 transceiver. The RS-485 transceiver can be selected to operate in either the half-duplex or full-duplex mode upon power-up via the HALF/FULL# pin. The RS-485 drivers guarantee a data rate of up to 8 Mbps.

All RS-485 drivers and receivers are protected to ±15kV using the Human Body Model ground combination, ±8kV using IEC 61000-4-2 Contact Discharge, and ±15kV using IEC 61000-4-2 Air-Gap Discharge. For more information, send an e-mail to uarttechsupport@exar.com.

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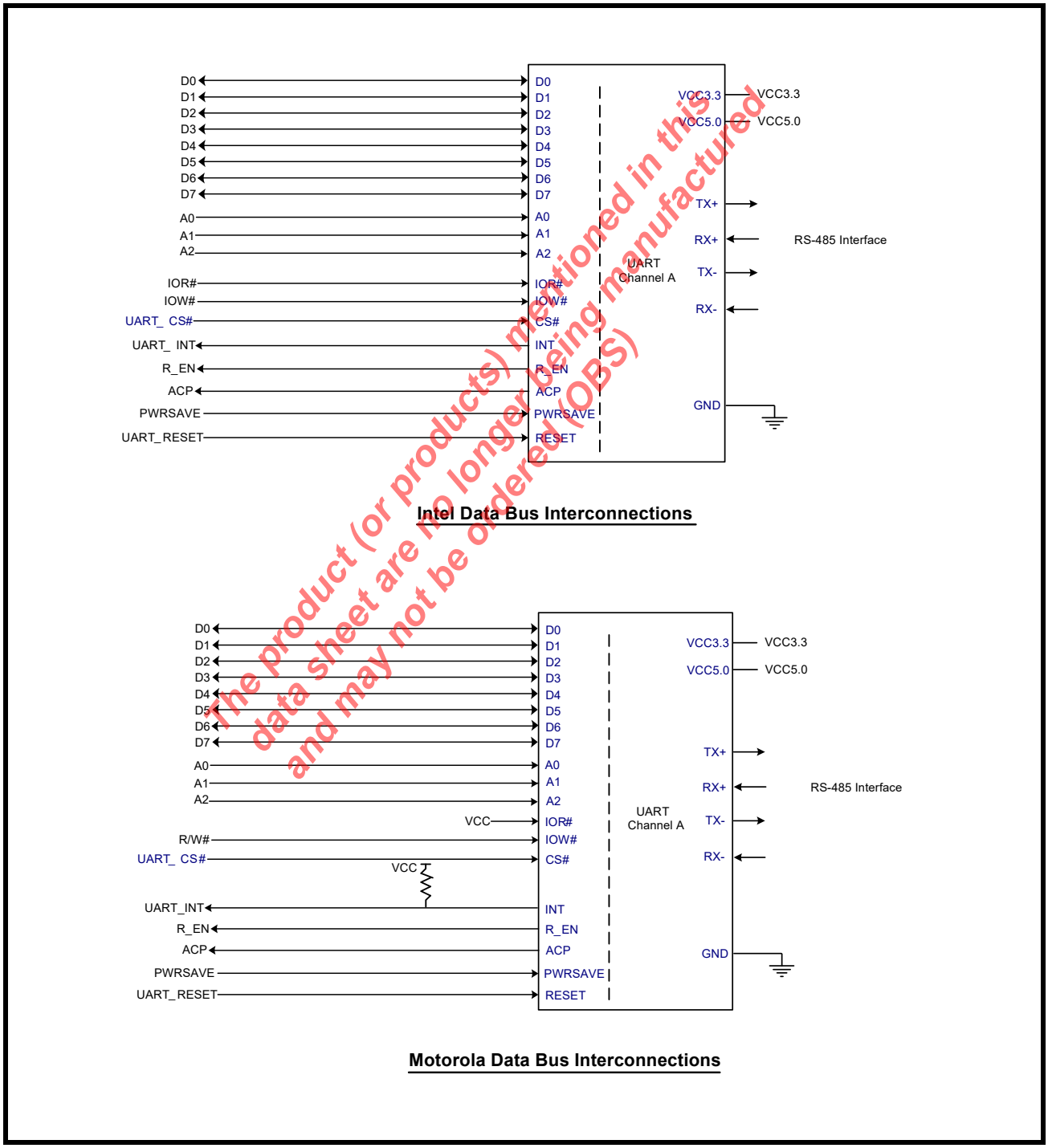
2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The L400 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# or R/W# inputs. A typical data bus interconnection for Intel and Motorola mode is shown in Figure 4.

FIGURE 4. XR19L400 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



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2.2 5-Volt Tolerant Inputs

The CMOS/TTL level inputs of the L400 can accept up to 5V inputs when operating at 3.3V. Note that the XTAL1 pin is not 5V tolerant when an external clock supply is used.

2.3 Device Hardware Reset

The RESET or RESET# input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 14). An active pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR19L400 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x01 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Channel Internal Registers

Each UART channel in the L400 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and an user accessible Scratchpad register (SPR).

Beyond the general 16C2550 features and capabilities, the L400 offers enhanced feature registers, namely, EFR, Xon/Xoff 1, Xon/Xoff 2, FCTR, TRG, EMSR and FC that provide Xon/Xoff software flow control, FIFO trigger level control and FIFO level counters. All the register functions are discussed in full detail later in "Section 3.0, UART Internal Registers" on page 20.

2.6 INT (IRQ#) Output

The interrupt output changes according to the operating mode and enhanced features setup. Table 1 and Table 2 below summarize the operating behavior for the transmitter and receiver in the Intel and Motorola modes. Also see Figures 18 through 21.

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TABLE 1: INT (IRQ#) PIN OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = one byte in THR 1 = THR empty	0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty
IRQ# Pin (I/M# = 0)	1 = one byte in THR 0 = THR empty	1 = FIFO above trigger level 0 = FIFO below trigger level or FIFO empty

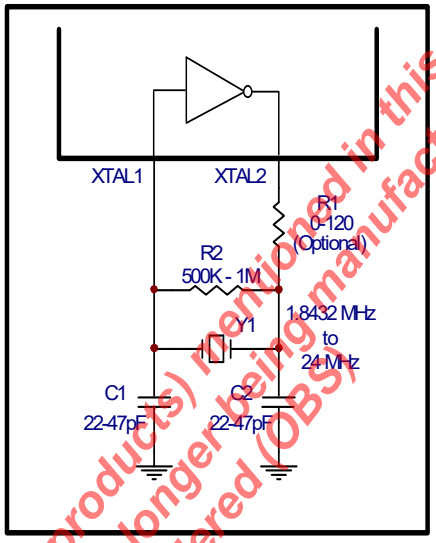
TABLE 2: INT (IRQ#) PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = no data 1 = 1 byte	0 = FIFO below trigger level 1 = FIFO above trigger level
IRQ# Pin (I/M# = 0)	1 = no data 0 = 1 byte	1 = FIFO below trigger level 0 = FIFO above trigger level

2.7 Crystal or External Clock Input

The L400 includes an on-chip oscillator (XTAL1 and XTAL2) to generate a clock when a crystal is connected between the XTAL1 and XTAL2 pins of the device. Alternatively, an external clock can be supplied through the XTAL1 pin. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock input and XTAL2 pin is the bufferred output which can be used as a clock signal for other devices in the system. Please note that the input XTAL1 is not 5V tolerant and therefore, the maximum voltage at the pin should be 3.3V when an external clock is supplied. For programming details, see "Programmable Baud Rate Generator."

FIGURE 5. TYPICAL CRYSTAL CONNECTIONS



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The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. When VCC = 5V, the on-chip oscillator can operate with a crystal whose frequency is not greater than 24 MHz. On the other hand, the L400 can accept an external clock of up to 64 MHz at XTAL1 pin which results in a maximum data rate of 8 Mbps. For further reading on the oscillator circuit please see DAN108 on EXAR's web site at **http://www.exar.com.**

2.8 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 3** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 3**. At 8X sampling rate, these data rates would double. Also, when using 8X sampling mode, please note that the bit-

time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), with 16X mode **EMSR[7] = 1**
Required Divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode **EMSR[7] = 0**

The closest divisor that is obtainable in the L400 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

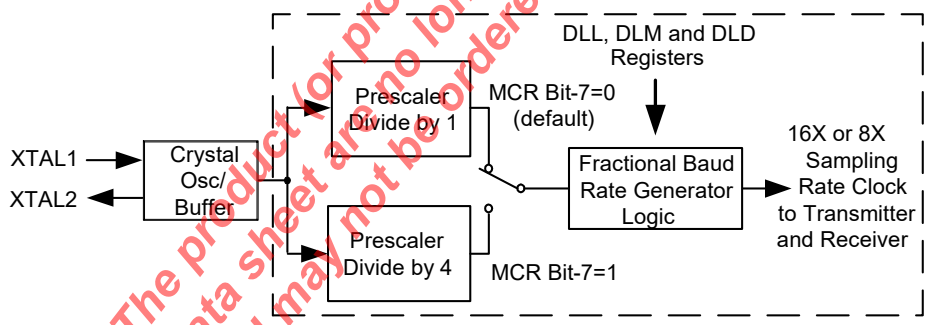
In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 6. BAUD RATE GENERATOR



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 3: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN L400	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

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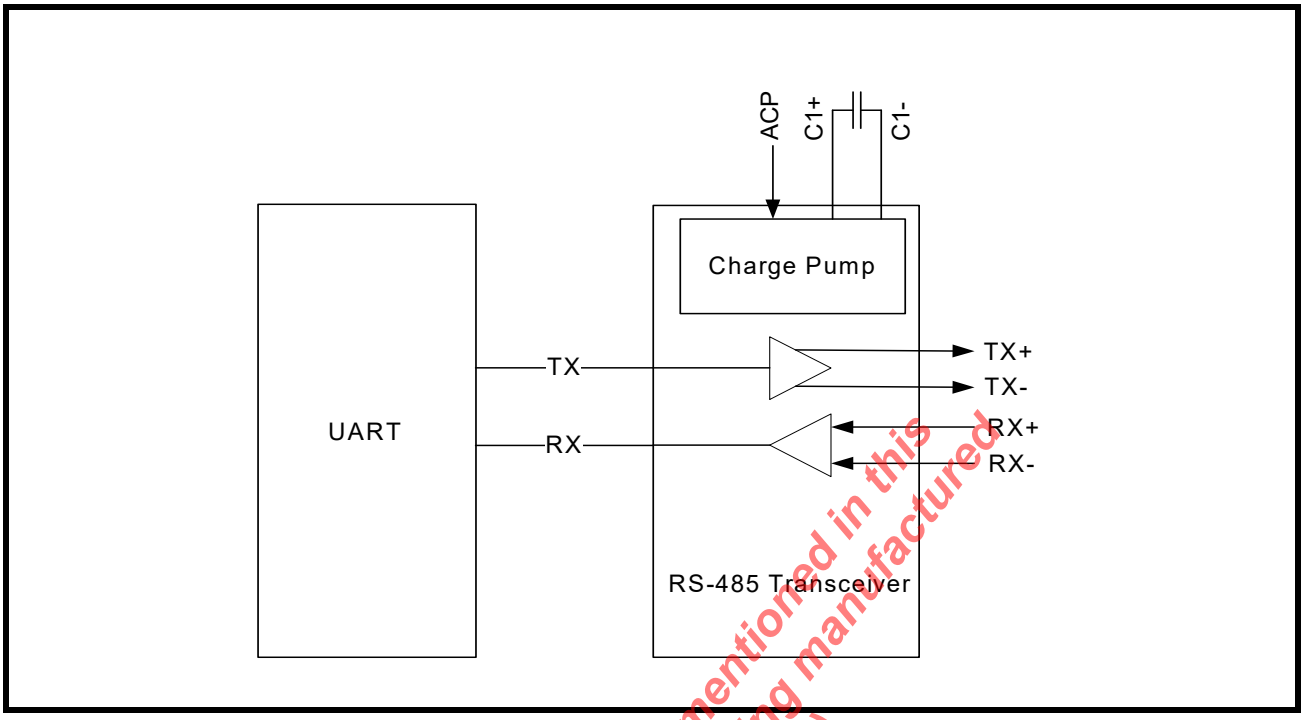
FIGURE 7. XR19L400 TRANSMITTER AND RECEIVER



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2.9 *Transmitter*

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X internal clock. A bit time is 16 (8) clock periods (see EMSR bit-7). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

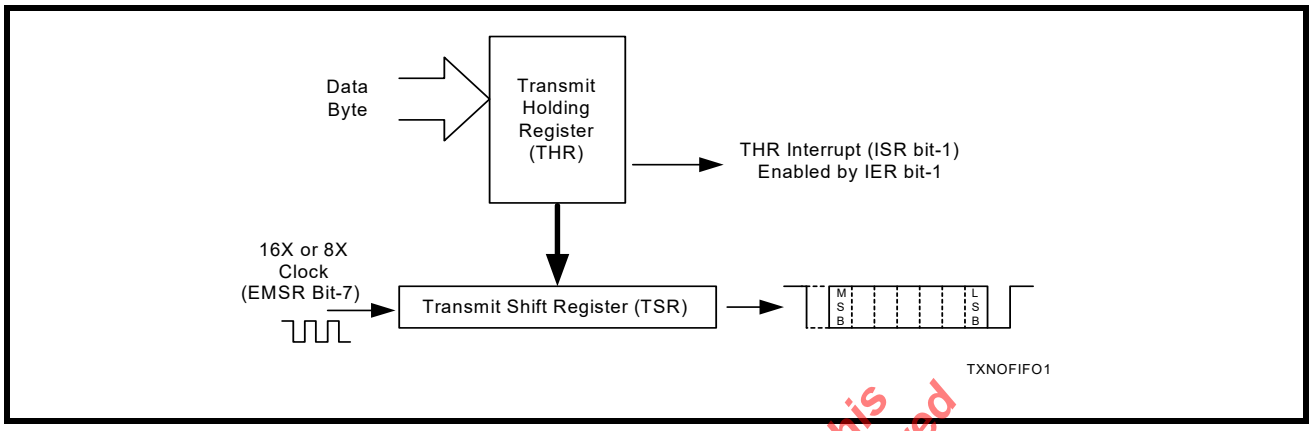
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

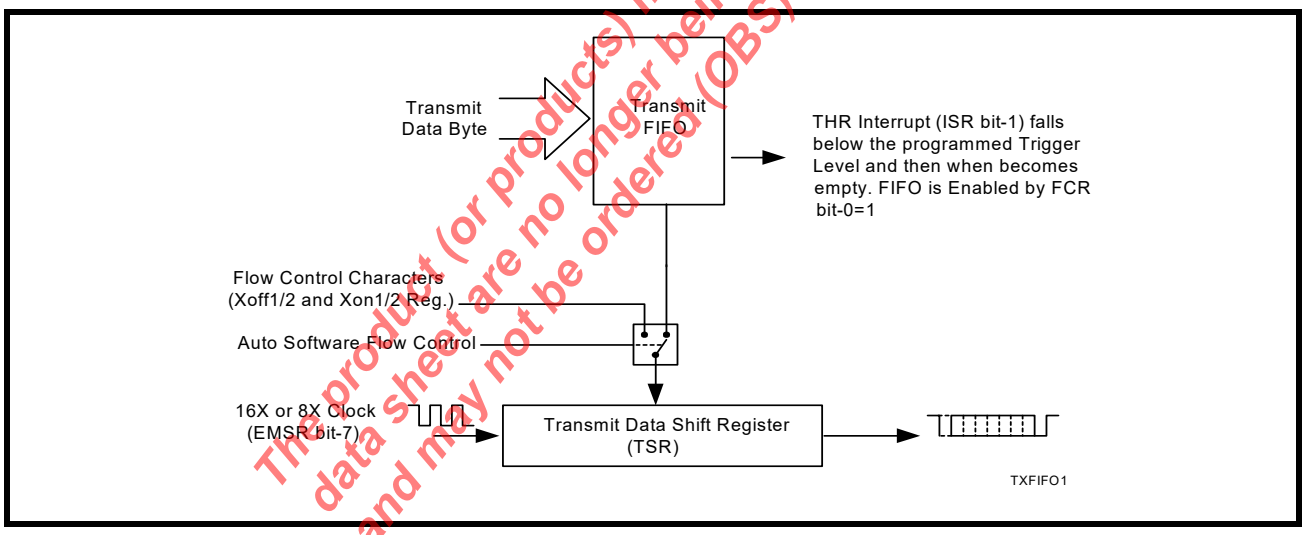
FIGURE 8. TRANSMITTER OPERATION IN NON-FIFO MODE



2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The Transmitter Empty Flag (LSR bit-6) is set when both the TSR and the FIFO become empty.

FIGURE 9. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



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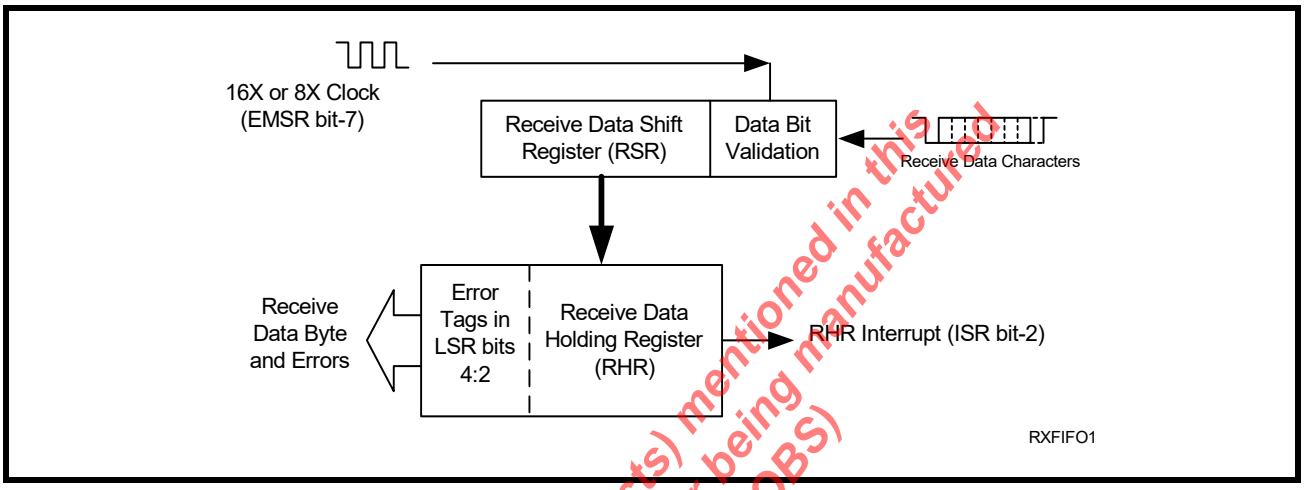
2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X clock (EMSR bit-7) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X clock rate. After 8 clocks (or 4 if 8X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 10. RECEIVER OPERATION IN NON-FIFO MODE



2.11 *Auto Xon/Xoff (Software) Flow Control*

When software flow control is enabled (See Table 13), the L400 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the L400 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the L400 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the L400 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 13) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the L400 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the L400 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The L400 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the L400 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the

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trigger level minus the hysteresis value (for Trigger Table D). These hysteresis values are shown in Table 11. Table 4 below explains this when Trigger Table-B (See Table 12) is selected.

TABLE 4: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 8-bit word length, no parity and 1 stop bit setting.*

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2.12 Sleep Mode, ACP Mode and Power-Save Feature with Wake-Up Interrupt

2.12.1 UART sleep mode (3.3V or 5V operation)

The UART portion in the L400 can enter sleep mode if all of these conditions are satisfied:

- no interrupts pending (ISR bit-0 = 1)
- the 16-bit divisor programmed in DLM and DLL registers is a non-zero value
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idle

The L400 stops its crystal oscillator to conserve power in this mode. The user can check the XTAL2 pin for no clock output as an indication that the device has entered the partial sleep mode.

The UART portion in the L400 resumes normal operation or active mode by any of the following:

- a receive data start bit transition on the RX inputs
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1' (in internal loopback mode)

If the sleep mode is enabled and the L400 is awakened by one of the conditions described above, an interrupt is issued by the L400 to signal to the CPU that it is awake. The lower nibble of the interrupt source register (ISR) will read a value of 0x1 for this interrupt and reading the ISR clears this interrupt. Since the same value (0x1) is also used to indicate no pending interrupt, users should exercise caution while using the sleep mode. The UART portion in the L400 will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the UART portion of the L400 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The UART portion of the L400 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.12.1.1 Receiving data in UART sleep mode

There is a start-up delay for the crystal oscillator after waking up from sleep mode, therefore the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. If an external oscillator is used, any data received will be transferred to/from the UART without any issues.

2.12.2 UART active, Charge pump of RS-485 transceiver shut down (3.3V operation only)

If the ACP pin is HIGH and the UART portion of the L400 is not in sleep mode, then the charge pump will automatically shut down to conserve power if the following conditions are true:

- no activity on the TX output signals
- modem inputs have been idle for approximately 30 seconds

When these conditions are satisfied, the L400 shuts down the charge pump and tri-states the RS-485 drivers to conserve power. In this mode, the RS-485 receivers are fully active and the internal registers of the L400 can be accessed. The time for the charge pump to resume normal operation after exiting the sleep mode is typically 45µs. It will wake up by any of the following:

- a receive data start bit transition on the RX input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a LOW to HIGH transition on any of the modem or general purpose serial inputs

Because the receivers are fully active when the charge pump is turned off, any data received will be transferred to/from the UART without any issues.

2.12.2.1 Transmitting data in ACP Mode

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Since it takes the charge pump typically 45µs to resume normal operation after ACP mode has been disabled. It is recommended that data not be transmitted until after this time.

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2.12.3 UART sleep, Charge pump of RS-485 transceiver shut down (3.3V operation only)

If the ACP pin is HIGH and the UART portion of the L400 is in sleep mode, then the charge pump will shut down immediately.

In this mode, the L400 shuts down the charge pump and tri-states the RS-485 drivers to conserve power. In this mode, the RS-485 receivers are fully active and the internal registers of the L400 can be accessed. The time for the charge pump to resume normal operation after exiting the sleep mode is typically 45µs. It will wake up by any of the following:

- a receive data start bit transition on the RX input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a LOW to HIGH transition on any of the modem or general purpose serial inputs

2.12.3.1 Receiving data in UART sleep mode

There is a start-up delay for the crystal oscillator after waking up from sleep mode, therefore the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. If an external oscillator is used, any data received will be transferred to/from the UART without any issues.

2.12.3.2 Transmitting data in ACP mode

Since it takes the charge pump typically 45µs to resume normal operation after ACP mode has been disabled. It is recommended that data not be transmitted until after this time.

2.12.4 Power-Save Feature

This mode is in addition to the sleep mode and in this mode, the core logic of the L400 is isolated from the CPU interface. If the address lines, data bus lines, IOW#, IOR# and CS# remain steady when the L400 is in full sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 37. However, if the input lines are floating or are toggling while the L400 is in sleep mode, the current can be up to 100 times more. If not using the Power-Save feature, an external buffer would be required to keep the address and data bus lines from toggling or floating to achieve the low current. But if the Power-Save feature is enabled (PwrSave pin connected to VCC), this will eliminate the need for an external buffer by internally isolating the address, data and control signals from other bus activities that could cause wasteful power drain (see **Figure 1**). The L400 enters Power-Save mode when this pin is connected to VCC, and the UART portion of the L400 is already in sleep mode.

Since Power-Save mode isolates the address, data and control signals, **the device will wake-up only by**:

- a receive data start bit transition, or
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1'

The L400 will return to the Power-Save mode automatically after a read to the MSR (to reset the modem inputs) and all interrupting conditions have been serviced and cleared. The L400 will stay in the Power-Save mode of operation until it is disabled by setting IER bit-4 to a logic 0 and/or the Power-Save pin is connected to GND.

If the L400 is awakened by any one of the above conditions, it issues an interrupt as soon as the oscillator circuit is up and running and the device is ready to transmit/receive. This interrupt has the same encoding (bit-0 of ISR register = 1) as "no interrupt pending" and will clear when the ISR register is read. This will show up in the ISR register only if no other interrupts are enabled.

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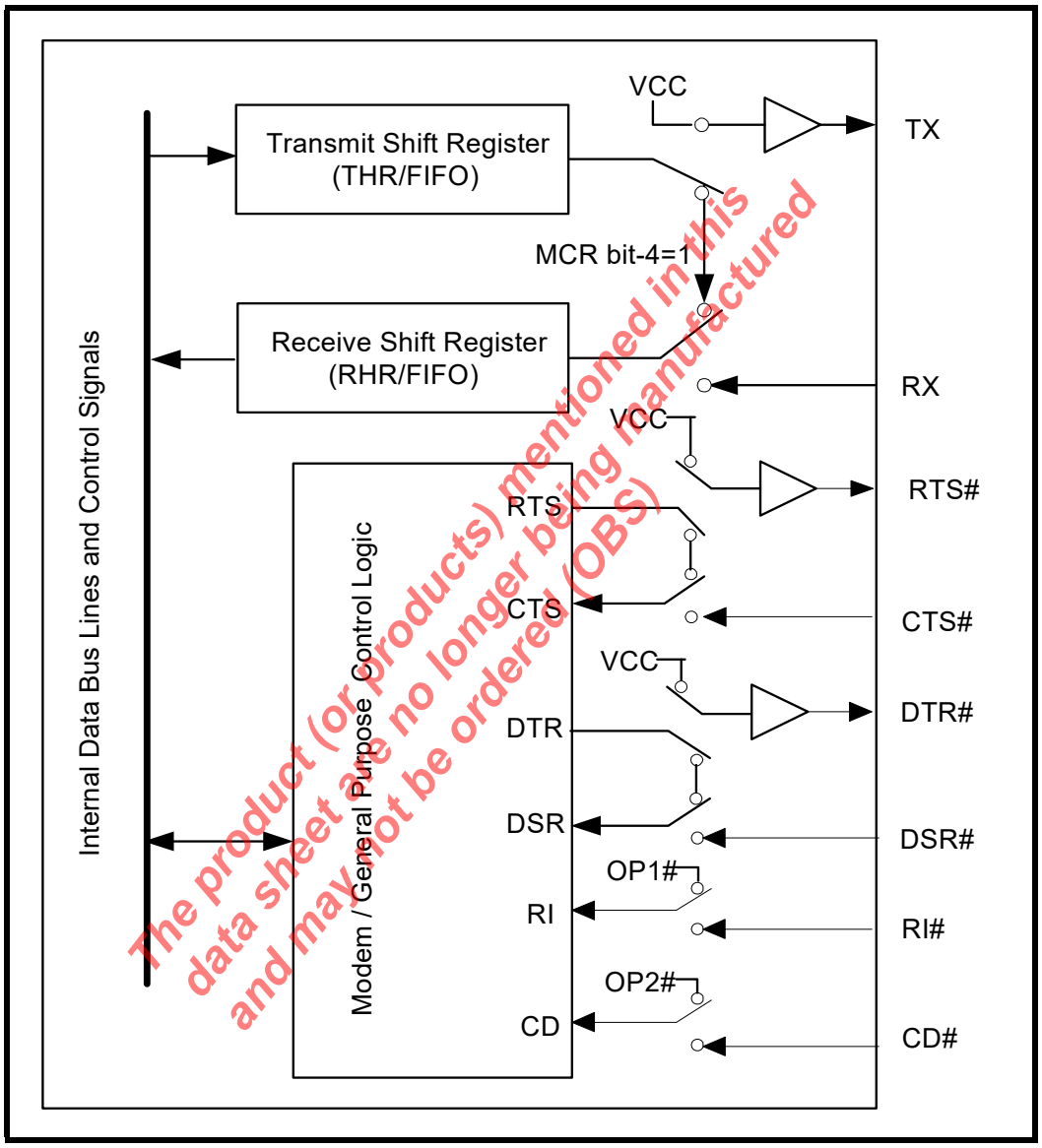
2.13 Internal Loopback

The L400 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 11 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending.

FIGURE 11. INTERNAL LOOP BACK



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3.0 UART INTERNAL REGISTERS

The L400 has a set of configuration registers selected by address lines A0, A1 and A2 with CS# asserted. The complete register set is shown on Table 5 and Table 6.

TABLE 5: UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	DLD - Divisor Fractional	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR ≠ 0xBF
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR ≠ 0xBF, FCTR[6] = 0
1 1 1	FLVL - RX/TX FIFO Level Counter Register	Read-only	LCR ≠ 0xBF, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
ENHANCED REGISTERS			
0 0 0	TRG - RX/TX FIFO Trigger Level Register FC - RX/TX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Register	Read/Write	
0 1 0	EFR - Enhanced Function Register	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

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TABLE 6: INTERNAL REGISTERS DESCRIPTIONS. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ Rsrvd	0/ Rsrvd	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR ≠ 0xBF
0 1 0	FCR	WR	RX FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	Rsrvd	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ Rsrvd	0/ XonAny	Internal Lopback Enable	OP2#/INT Output Enable	Rsrvd (OP1#)	RTS# Output Control	DTR# Output Control	LCR ≠ 0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR ≠ 0xBF FCTR[6]=0
1 1 1	EMSR	WR	16X Sam-pling Rate Mode	LSR Error Inter-rupt. Imd/Dly#	Auto RTS Hyst. bit-3	Auto RTS Hyst. bit-2	Rsrvd	Rsrvd	Rx/Tx FIFO Count	Rx/Tx FIFO Count	LCR ≠ 0xBF FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

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TABLE 6: INTERNAL REGISTERS DESCRIPTIONS. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	DLD	RD/WR	0	0	0	0	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF EFR[4] = 1
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	1	0	1	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Auto Half-Duplex Direction Control	Rsrvd	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Rsrvd	Rsrvd	Rsrvd	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], DLD	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

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4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 13.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 12.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR19L400 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO (default). Instead, LSR bits 2-4 can be programmed to generate an interrupt immediately, by setting EMSR bit-6 to a logic 1.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

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IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[7:6]: Reserved

For normal operation, these bits should remain at logic 0.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 7, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto half-duplex control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff is by detection of a Xoff character.
- Wake-up Indicator is when the UART comes out of sleep mode.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to ISR or when Xon character(s) is received.
- Wake-up Indicator is cleared by a read to the ISR register.

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TABLE 7: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff character)
-	0	0	0	0	0	1	None (default) or Wake-up Indicator

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition) or the device has come out of sleep mode.

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 7).

ISR[4]: Xoff Character Interrupt Status (requires EFR bit-4=1)

This bit is enabled when IER[5] = 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s).

ISR[5]: Reserved

For normal operation, this bit should remain a logic 0.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, and set the transmit/receive FIFO trigger levels.

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: Reserved

For normal operation, this bit should remain a logic 0.

FCR[5:4]: Transmit FIFO Trigger Select (requires EFR bit-4=1)

(logic 0 = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 8 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 8 shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (ODS).

TABLE 8: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

Trigger Table	FCTR Bit-5	FCTR Bit-4	FCR Bit-7	FCR Bit-6	FCR Bit-5	FCR bit-4	Receive Trigger Level	Transmit Trigger Level	Compatibility
Table-A	0	0			0	0		1 (default)	16C550, 16C2550, 16C2552, 16C554, 16C580
			0	0			1 (default)		
			0	1			4		
			1	0			8		
			1	1			14		
Table-B	0	1			0	0		16	16C650A
					0	1		8	
					1	0		24	
					1	1		30	
			0	0			8		
			0	1			16		
			1	0			24		
			1	1			28		

TABLE 8: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-5	FCTR BIT-4	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-C	1	0			0	0		8	16C654
					0	1		16	
					1	0		32	
					1	1		56	
			0	0			8		
			0	1			16		
			1	0			56		
			1	1			60		
Table-D	1	1	X	X	X	X	Programmable via TRG register. FCTR[7] = 0.	Programmable via TRG register. FCTR[7] = 1.	16L2752, 16C2850, 16C2852, 16C850, 16C854, 16C864

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 9 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR bit-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 9: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space", LOW state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", LOW, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL, DLM and DLD) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

DTR# is not available as an output pin on the L400, but it is available for use during internal loopback mode. In internal loopback mode, this bit is used to write the state of the DSR# interface signal.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Output

RTS# is not available as an output pin on the L400, but it is available for use during internal loopback mode. In internal loopback mode, this bit is used to write the state of the CTS# interface signal. If half-duplex mode is enabled via the Half/Full# pin or in is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. The RTS# pin can also be used for Auto RS485 Half-Duplex direction control enabled by FCTR bit-3. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# HIGH (default).
- Logic 1 = Force RTS# LOW.

MCR[2]: Reserved

OP1# is not available as an output pin on the L400. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: OP2# Output / INT Output Enable

This bit enables or disables the operation of INT, interrupt output. If INT output is not used, OP2# can be used as a general purpose output. Also, if 16/68# pin selects Motorola bus interface mode, this bit must be set to logic 0.

- Logic 0 = INT (A-B) outputs disabled (three state mode) and OP2# output set HIGH(default).
- Logic 1 = INT (A-B) outputs enabled (active mode) and OP2# output set LOW.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 11.

MCR[5]: Xon-Any Enable (requires EFR bit-4=1)

- Logic 0 = Disable Xon-Any function (default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO, unless the RX character is an Xon or Xoff character and the L400 is programmed to use the Xon/Xoff flow control.

MCR[6]: Reserved

For normal operation, this bit should remain a logic 0.

MCR[7]: Clock Prescaler Select (requires EFR bit-4=1)

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Error Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Error Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was LOW for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

MSR[0]: Delta CTS# Input Flag (Internal Loopback Mode Only)

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag (Internal Loopback Mode Only)

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag (Internal Loopback Mode Only)

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a LOW to HIGH, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag (Internal Loopback Mode Only)

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# is not available as an input pin on the L400, but it is available for use during internal loopback mode. This bit is equivalent to the RTS# bit in the MCR register.

MSR[5]: DSR Input Status

CTS# is not available as an input pin on the L400, but it is available for use during internal loopback mode. This bit is equivalent to the DTR# bit in the MCR register.

MSR[6]: RI Input Status

RI# is not available as an input pin on the L400, but it is available for use during internal loopback mode. This bit is equivalent to bit-2 in the MCR register.

MSR[7]: CD Input Status

CD# is not available as an input pin on the L400, but it is available for use during internal loopback mode. This bit is equivalent to bit-3 in the MCR register.

4.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.11 Enhanced Mode Select Register (EMSR)

This register replaces SPR (during a Write) and is accessible only when FCTR[6] = 1.

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

EMSR[1:0]: Receive/Transmit FIFO Level Count (Write-Only)

When Scratchpad Swap (FCTR[6]) is asserted, EMSR bits 1-0 controls what mode the FIFO Level Counter is operating in.

TABLE 10: SCRATCHPAD SWAP SELECTION

FCTR[6]	EMSR[1]	EMSR[0]	Scratchpad is
0	X	X	Scratchpad
1	X	0	RX FIFO Level Counter Mode
1	0	1	TX FIFO Level Counter Mode
1	1	1	Alternate RX/TX FIFO Counter Mode

During Alternate RX/TX FIFO Level Counter Mode, the first value read after EMSR bits 1-0 have been asserted will always be the RX FIFO Level Counter. The second value read will correspond with the TX FIFO Level Counter. The next value will be the RX FIFO Level Counter again, then the TX FIFO Level Counter and so on and so forth.

EMSR[3:2]: Reserved

For normal operation, these bits should remain a logic 0.

EMSR[5:4]: Extended RTS Hysteresis

TABLE 11: XON/XOFF HYSTERESIS

EMSR BIT-5	EMSR BIT-4	FCTR BIT-1	FCTR BIT-0	XON/XOFF HYSTERESIS (CHARACTERS)
0	0	0	0	0
0	0	0	1	±4
0	0	1	0	±6
0	0	1	1	±8
0	1	0	0	±8
0	1	0	1	±16
0	1	1	0	±24
0	1	1	1	±32
1	0	0	0	±40
1	0	0	1	±44
1	0	1	0	±48
1	0	1	1	±52
1	1	0	0	±12
1	1	0	1	±20
1	1	1	0	±28
1	1	1	1	±36

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EMSR[6]: LSR Interrupt Mode

- Logic 0 = LSR Interrupt Delayed (for 16C2550 compatibility, default). LSR bits 2, 3, and 4 will generate an interrupt when the character with the error is in the RHR.
- Logic 1 = LSR Interrupt Immediate. LSR bits 2, 3, and 4 will generate an interrupt as soon as the character is received into the FIFO.

EMSR[7]: 16X Sampling Rate Mode

Logic 0 = 8X Sampling Rate.

Logic 1 = 16X Sampling Rate (default).

4.12 FIFO Level Register (FLVL) - Read-Only

The FIFO Level Register replaces the Scratchpad Register (during a Read) when FCTR[6] = 1. Note that this is not identical to the FIFO Data Count Register which can be accessed when LCR = 0xBF.

FLVL[7:0]: FIFO Level Register

This register provides the FIFO counter level for the RX FIFO or the TX FIFO or both depending on EMSR[1:0]. See Table 10 for details.

4.13 Baud Rate Generator Registers (DLL, DLM and DLD) - Read/Write

These registers make-up the value of the baud rate divisor. The concatenation of the contents of DLM and DLL is a 16-bit value is then added to DLD/16 to achieve the fractional baud rate divisor. DLD must be enabled via EFR bit-4 before it can be accessed. **SEE"PROGRAMMABLE BAUD RATE GENERATOR WITH FRACTIONAL DIVISOR" ON PAGE 9.**

4.14 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x0A). Prior to reading this register, DLL and DLM should be set to 0x00 (DLD = 0xXX).

4.15 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00 (DLD = 0xXX).

4.16 Trigger Level Register (TRG) - Write-Only

User Programmable Transmit/Receive Trigger Level Register. If both the TX and RX trigger levels are used, the TX trigger levels must be set before the RX trigger levels.

TRG[7:0]: Trigger Level Register

These bits are used to program desired trigger levels when trigger Table-D is selected. FCTR bit-7 selects between programming the RX Trigger Level (a logic 0) and the TX Trigger Level (a logic 1).

4.17 RX/TX FIFO Level Count Register (FC) - Read-Only

This register is accessible when LCR = 0xBF. Note that this register is not identical to the FIFO Level Count Register which is located in the general register set when FCTR bit-6 = 1 (Scratchpad Register Swap). It is suggested to read the FIFO Level Count Register at the Scratchpad Register location when FCTR bit-6 = 1. See Table 10.

FC[7:0]: RX/TX FIFO Level Count

Receive/Transmit FIFO Level Count. Number of characters in Receiver FIFO (FCTR[7] = 0) or Transmitter FIFO (FCTR[7] = 1) can be read via this register. Reading this register is not recommended when transmitting or receiving data.

4.18 Feature Control Register (FCTR) - Read/Write

FCTR[2:0]: Reserved

For normal operation, these bits should remain a logic 0.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (ODS)

FCTR[3]: Auto Half-Duplex Direction Control

This bit overrides the HALF/FULL# pin to enable half-duplex mode or full-duplex mode.

- Logic 0 = Full-duplex mode. In this mode, the transmit interrupt is generated when the transmit holding register becomes empty and the transmit shift register is shifting data out.
- Logic 1 = Auto half-duplex mode. In this mode, the direction of the RS-485 transceiver is internally controlled by the RTS# signal. Also, the transmit interrupt generation is delayed until the transmitter shift register becomes empty.

FCTR[5:4]: Transmit/Receive Trigger Table Select

See Table 8 for more details.

TABLE 12: TRIGGER TABLE SELECT

FCTR BIT-5	FCTR BIT-4	TABLE
0	0	Table-A (TX/RX)
0	1	Table-B (TX/RX)
1	0	Table-C (TX/RX)
1	1	Table-D (TX/RX)

FCTR[6]: Scratchpad Swap

- Logic 0 = Scratch Pad register is selected as general read and write register. ST16C550 compatible mode.
- Logic 1 = FIFO Level Count register (Read-Only), Enhanced Mode Select Register (Write-Only). Number of characters in transmit or receive FIFO can be read via scratch pad register when this bit is set. Enhanced Mode Select Register is selected when it is written into.

FCTR[7]: Programmable Trigger Register Select

If using both programmable TX and RX trigger levels, TX trigger levels must be set before RX trigger levels.

- Logic 0 = Registers TRG and FC selected for RX.
- Logic 1 = Registers TRG and FC selected for TX.

4.19 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 13). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

TABLE 13: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[7:5]: Reserved

For normal operation, these bits should be at logic 0.

4.20 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 5.

TABLE 14: UART RESET CONDITIONS FOR CHANNEL A AND B

REGISTERS	RESET STATE
DLM, DLL	DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted.
DLD	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
EMSR	Bits 7-0 = 0x80
FLVL	Bits 7-0 = 0x00
TRG	Bits 7-0 = 0x00
FC	Bits 7-0 = 0x00
FCTR	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX+/TX-	RS-485 HIGH (Full-duplex mode)
INT (IRQ#)	Three-State Condition (16 mode) CMOS/TTL HIGH (68 mode)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	5.5 Volts
Voltage at Any Pin	GND-0.3 V to 5.5 V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (40-QFN)	theta-ja = 40°C/W, theta-jc = 13°C/W

ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA= -40° TO +85°C (INDUSTRIAL GRADE), VCC= 3.3 or 5V ± 10%

SYMBOL	PARAMETER	CONDITIONS	3.3V LIMITS MIN	3.3V LIMITS MAX	5.0V LIMITS MIN	5.0V LIMITS MAX	UNITS
DC CHARACTERISTICS							
ICC	Supply Current, Normal Mode	60 ohm load		40		20	mA
ISLP/IPWS	Supply Current, Sleep Mode/Power-Save Mode	60 ohm load, ACP mode disabled (ACP mode applies to 3.3V only)		10		15	mA
ISLP/IPWS	Supply Current, Sleep Mode/Power-Save Mode	60 ohm load, ACP mode enabled (ACP mode applies to 3.3V only)		5		-	mA
OSCILLATOR INPUT (X1)							
VILCK	Clock Input Low Level		-0.3	0.6	-0.5	0.6	V
VIHCK	Clock Input High Level		2.4	VCC	3.0	VCC	V
LOGIC INPUTS/OUTPUTS (D[0:7], A[0:2], IOR#, IOW#/R/W#, CS#, INT/IRQ#, RST#/RST, I/M#, PWRSAVE, ACP, R_EN							
VIL	Input Low Voltage		-0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage		2.0	5.5	2.0	5.5	V
VOL	Output Low Voltage			0.4		0.4	V
VOH	Output High Voltage		2.0		2.0		V
IIL	Input Low Leakage Current			+/-10		+/-10	uA
IHL	Input High Leakage Current			+/-10		+/-10	uA
RS-485 INPUTS (RX+, RX-)							
	Input Voltage Range		-7	+12	-7	+12	V
RS-485 OUTPUTS (TX+, TX-)							
VOD	Differential Driver Output	RL = 60 ohm	+2		+2		V
VOC	Driver Common-Mode Ouput Voltage	RL = 60 ohm		+3		+3	V
ILKGR	Output Leakage Current			+/-20		+/-20	uA

The product(or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=-40° TO +85°C, VCC=3.3 OR 5V ± 10%, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3		LIMITS 5.0		UNIT
		MIN	MAX	MIN	MAX	
-	Crystal Frequency		24		24	MHz
OSC	External Clock Frequency		64		64	MHz
CLK	External Clock Low/High Time	30		30		ns
T_{AS}	Address Setup Time (16 Mode)	0		0		ns
T_{AH}	Address Hold Time (16 Mode)	0		0		ns
T_{CS}	Chip Select Width (16 Mode)	65		65		ns
T_{RD}	IOR# Strobe Width (16 Mode)	65		65		ns
T_{DY}	Read Cycle Delay (16 Mode)	65		65		ns
T_{RDV}	Data Access Time (16 Mode)		60		60	ns
T_{DD}	Data Disable Time (16 Mode)	0	15	0	15	ns
T_{WR}	IOW# Strobe Width (16 Mode)	65		65		ns
T_{DY}	Write Cycle Delay (16 Mode)	65		65		ns
T_{DS}	Data Setup Time (16 Mode)	10		10		ns
T_{DH}	Data Hold Time (16 Mode)	5		5		ns
T_{ADS}	Address Setup (68 Mode)	0		0		ns
T_{ADH}	Address Hold (68 Mode)	0		0		ns
T_{RWS}	R/W# Setup to CS# (68 Mode)	0		0		ns
T_{RDA}	Read Data Access (68 mode)		60		60	ns
T_{RDH}	Read Data Disable Time (68 mode)	0	15	0	15	ns
T_{WDS}	Write Data Setup (68 mode)	10		10		ns
T_{WDH}	Write Data Hold (68 Mode)	5		5		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted (68 Mode)	5		5		ns
T_{CSL}	CS# Width (68 Mode)	65		65		ns
T_{CSD}	CS# Cycle Delay (68 Mode)	65		65		ns
T_{WDO}	Delay From IOW# To Output		50		50	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		50		50	ns

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=-40° TO +85°C, VCC=3.3 OR 5V ± 10%, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3 MIN	LIMITS 3.3 MAX	LIMITS 5.0 MIN	LIMITS 5.0 MAX	UNIT
T_{SI}	Delay From Stop To Interrupt		50		50	ns
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		50		50	ns
T_{RST}	Reset Pulse Width	40		40		ns
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-
Bclk	Baud Clock	16X or 8X of data rate				Hz

FIGURE 12. CLOCK TIMING

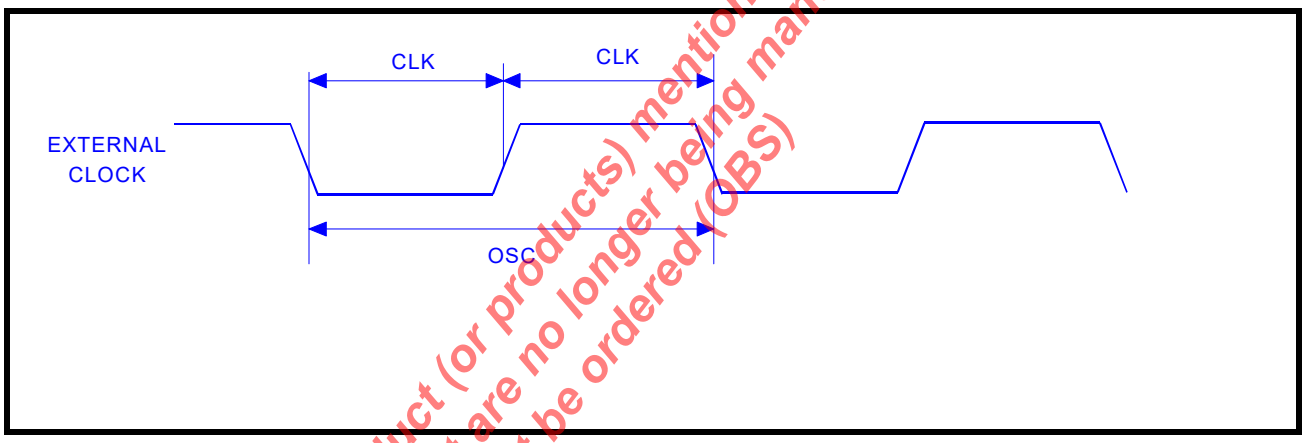

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FIGURE 13. MODEM INPUT/OUTPUT TIMING

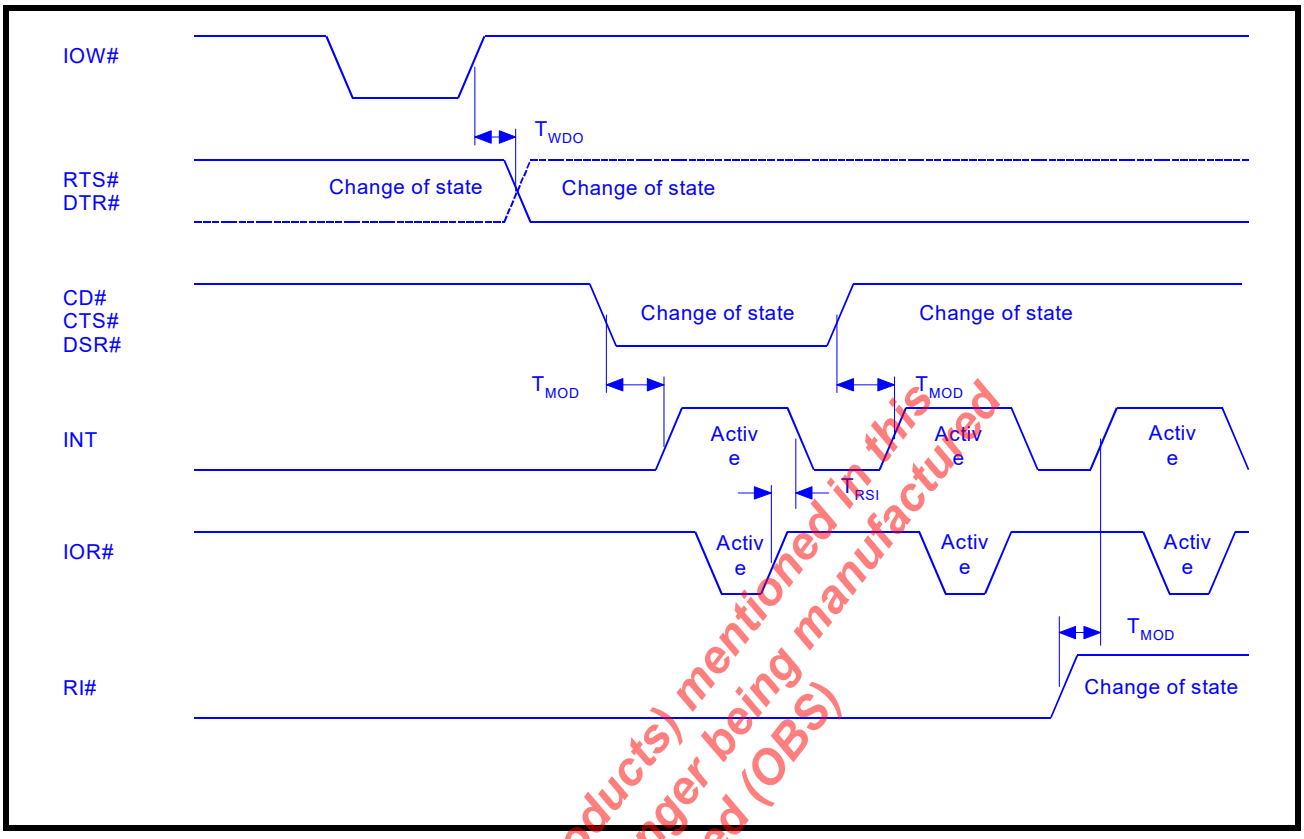

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FIGURE 14. 16 MODE (INTEL) DATA BUS READ TIMING

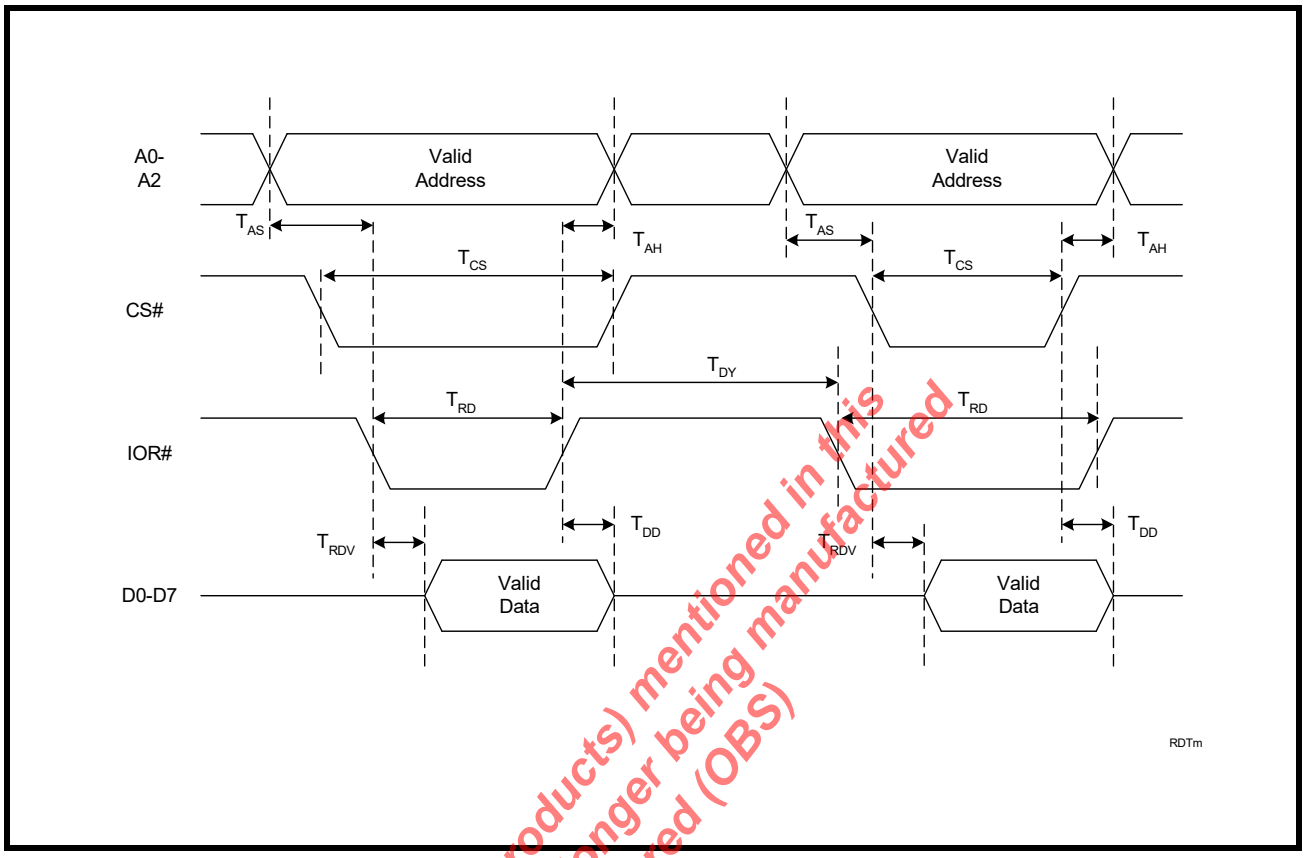

FIGURE 15. 16 MODE (INTEL) DATA BUS WRITE TIMING

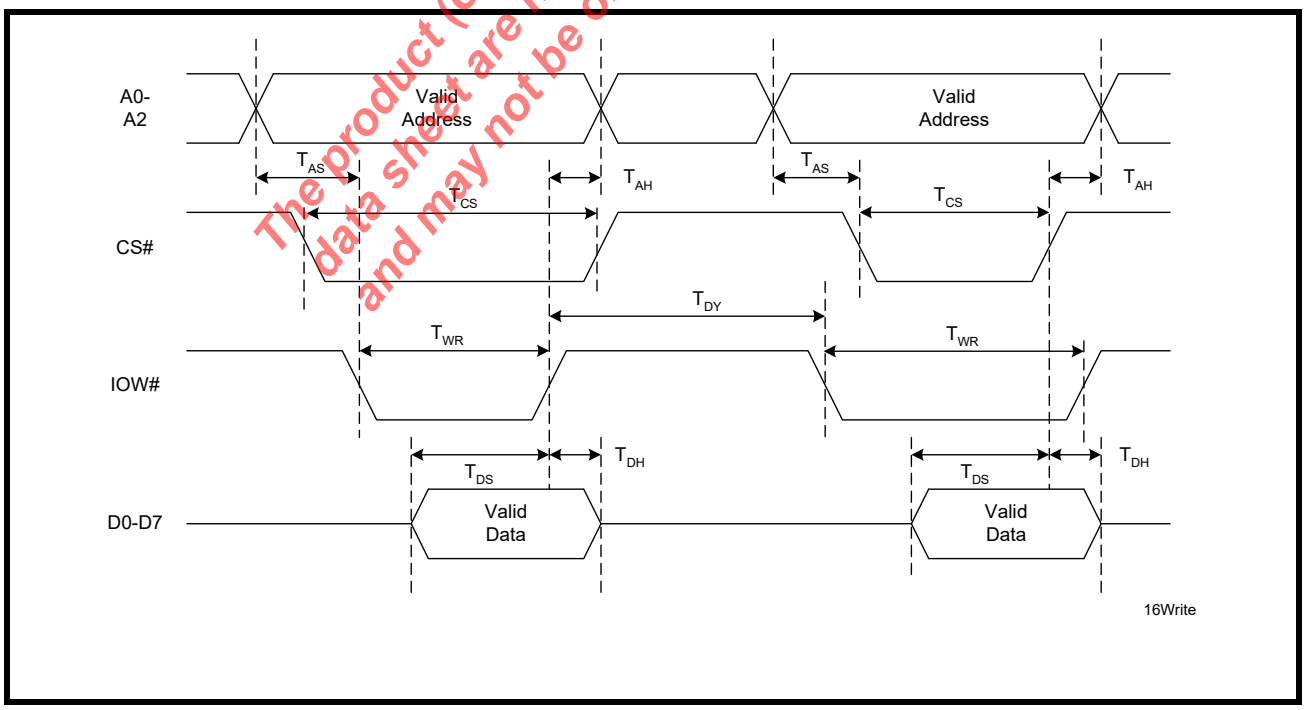

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FIGURE 16. 68 MODE (MOTOROLA) DATA BUS READ TIMING

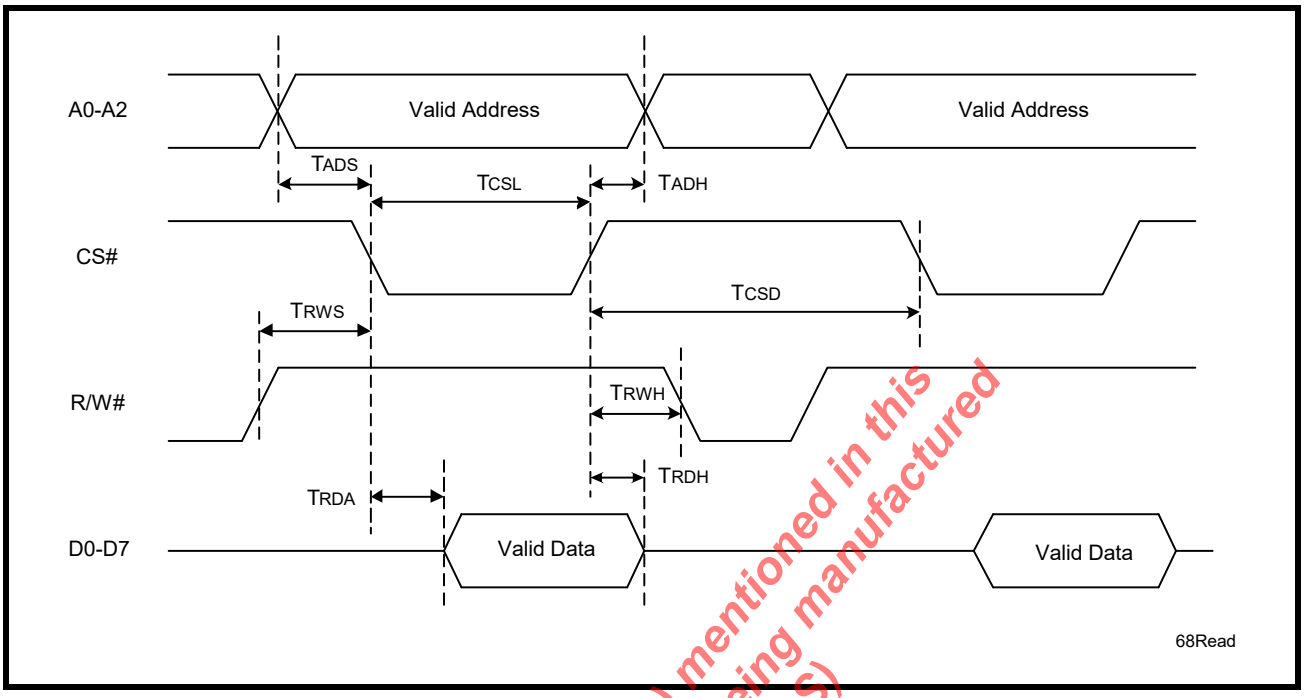
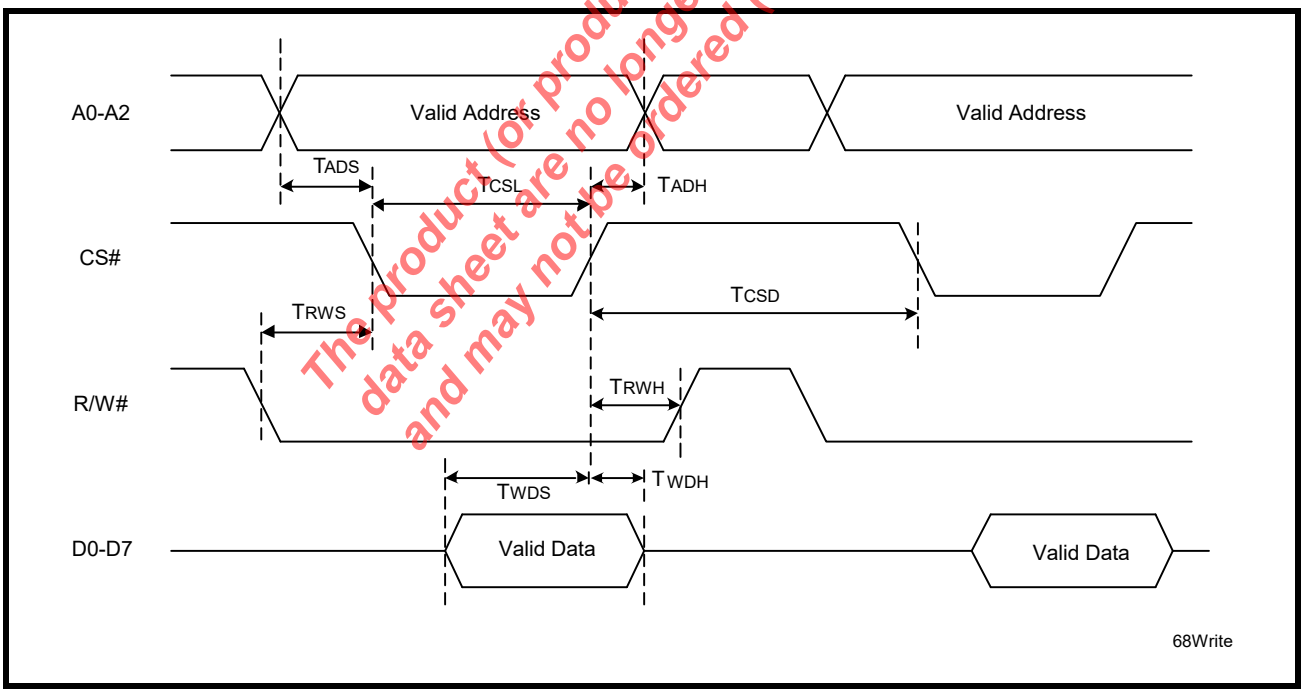


FIGURE 17. 68 MODE (MOTOROLA) DATA BUS WRITE TIMING



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 18. RECEIVE READY INTERRUPT TIMING [NON-FIFO MODE]

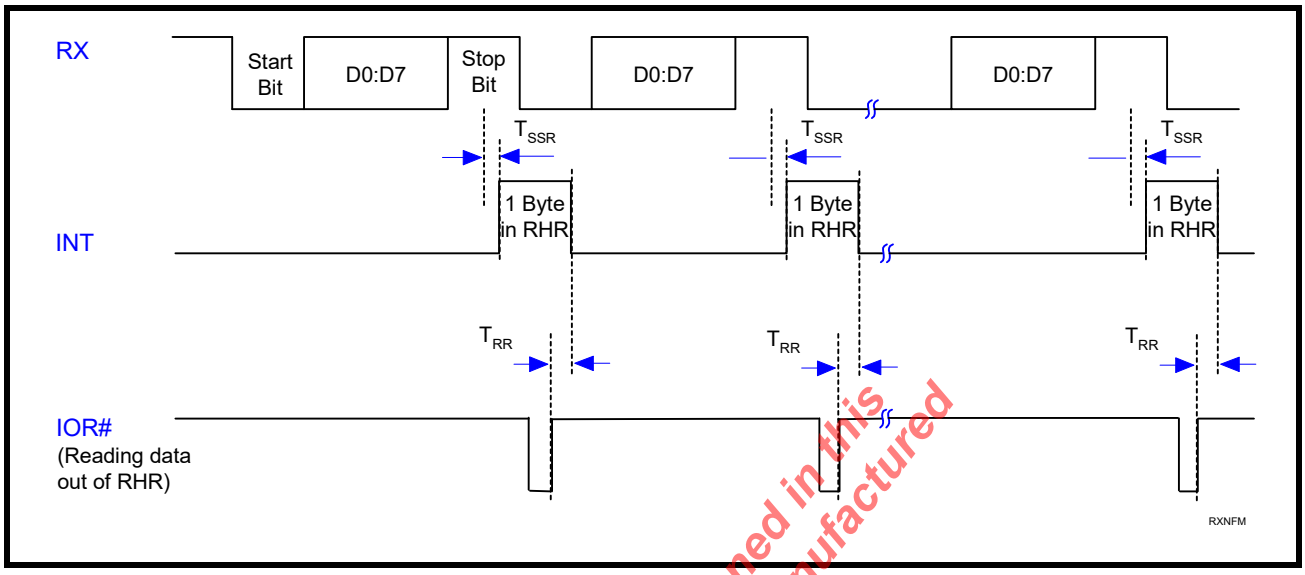


FIGURE 19. TRANSMIT READY INTERRUPT TIMING [NON-FIFO MODE]

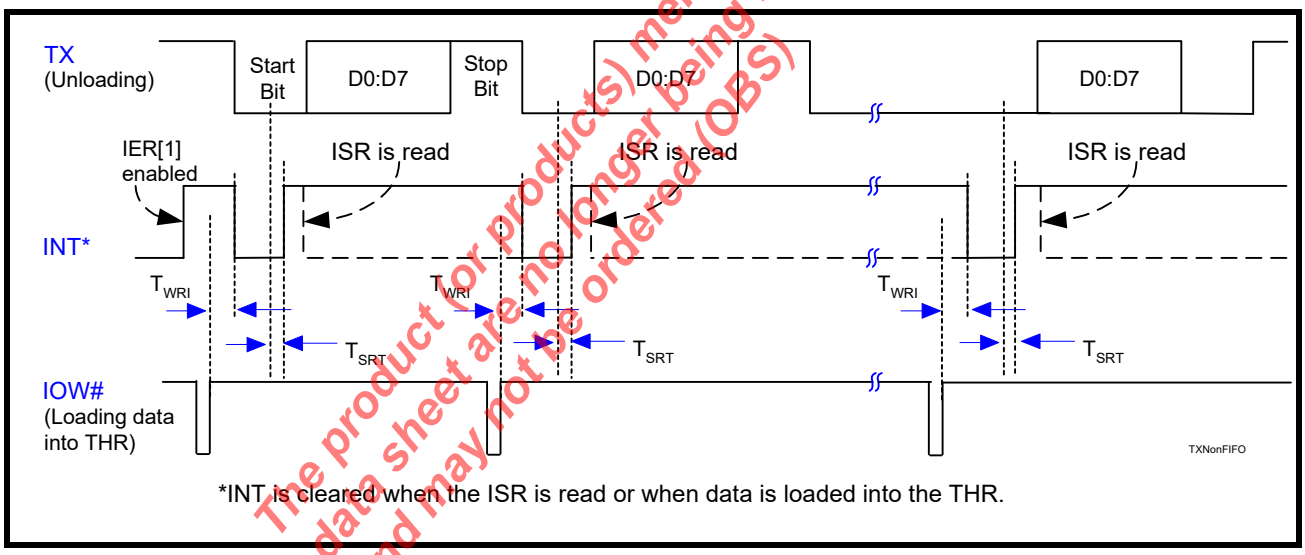


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FIGURE 20. RECEIVE READY INTERRUPT TIMING [FIFO MODE]

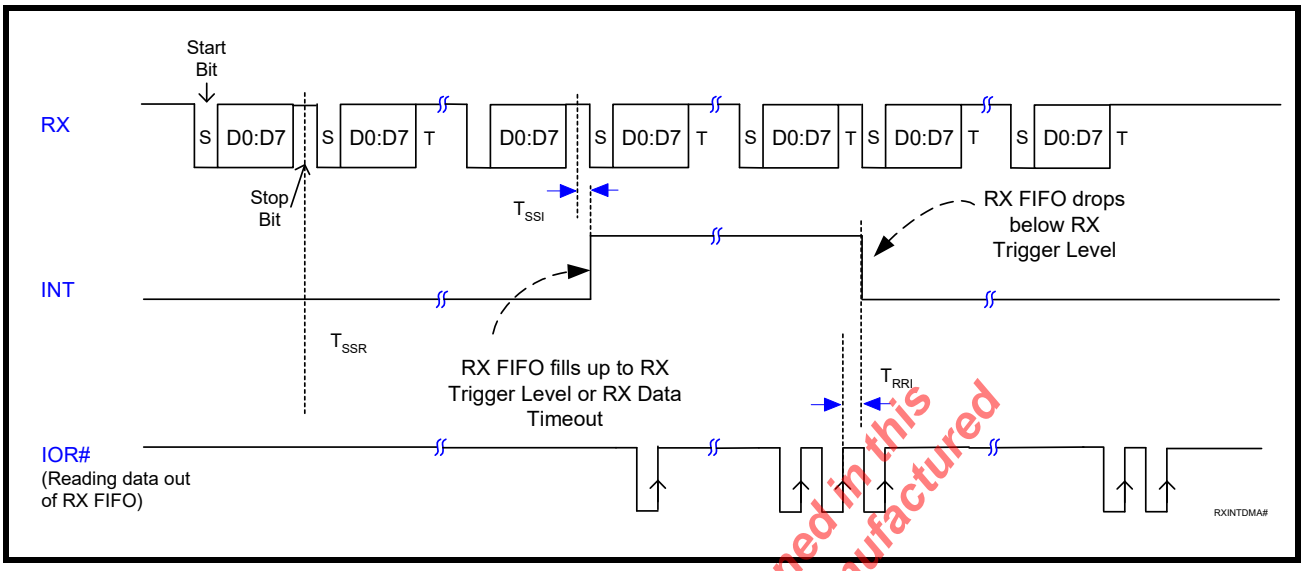
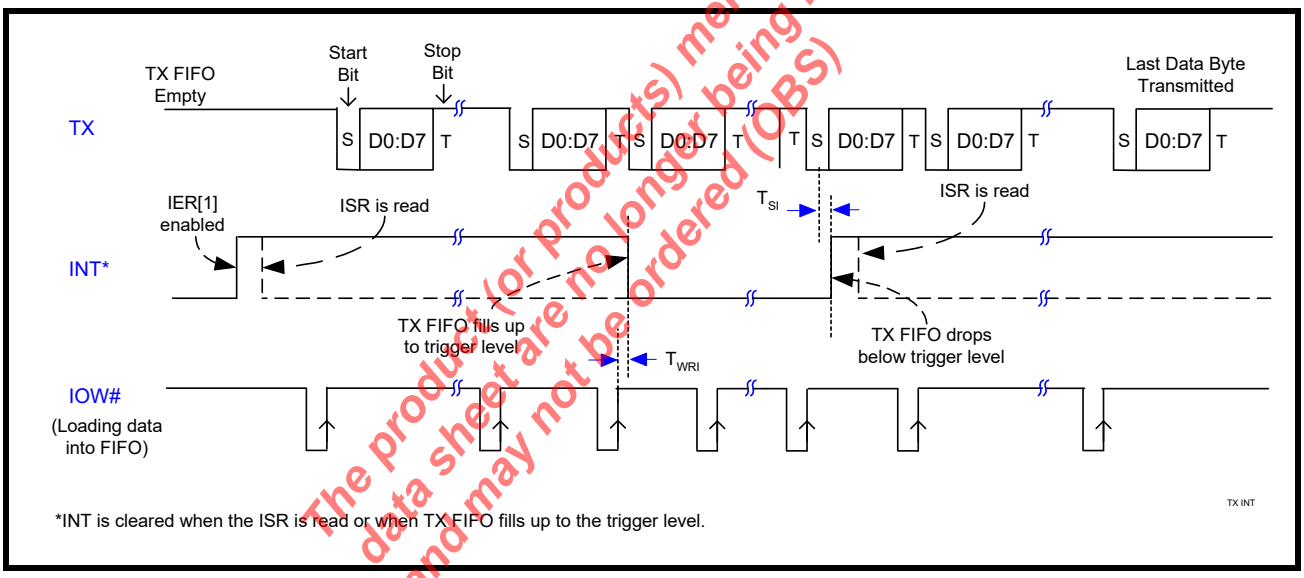


FIGURE 21. TRANSMIT READY INTERRUPT TIMING [FIFO MODE]



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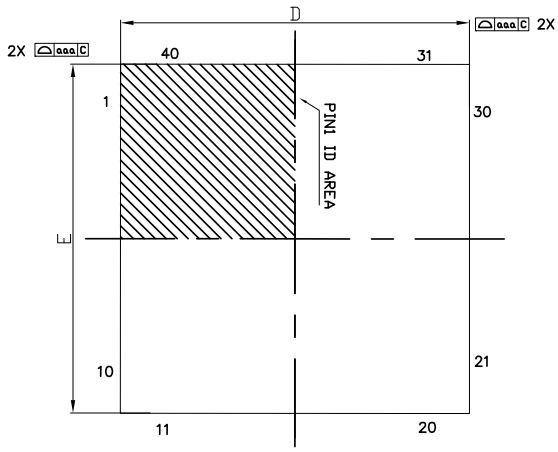
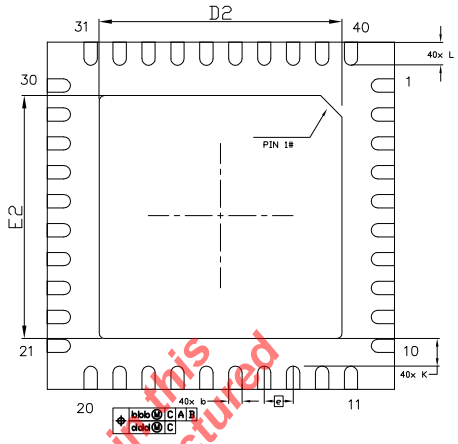
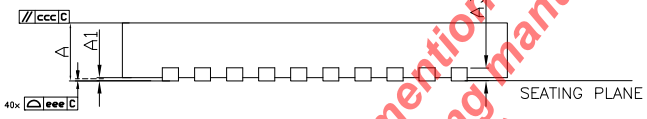
MECHANICAL DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIMENSION TABLE				
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20Ref	---	
b	0.20	0.25	0.30	
D		6.00 BSC		
E		6.00 BSC		
e		0.50 BSC		
D2	4.50	4.65	4.80	
E2	4.50	4.65	4.80	
L	0.35	0.40	0.45	
K	0.20	–	–	
aaa		0.15		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		40		

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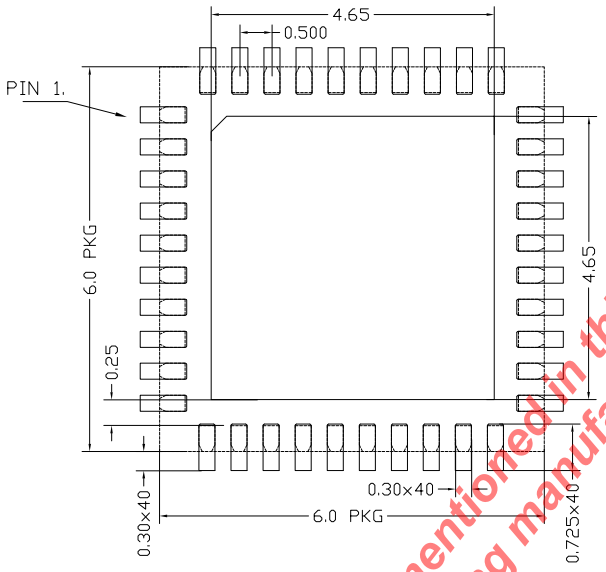
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

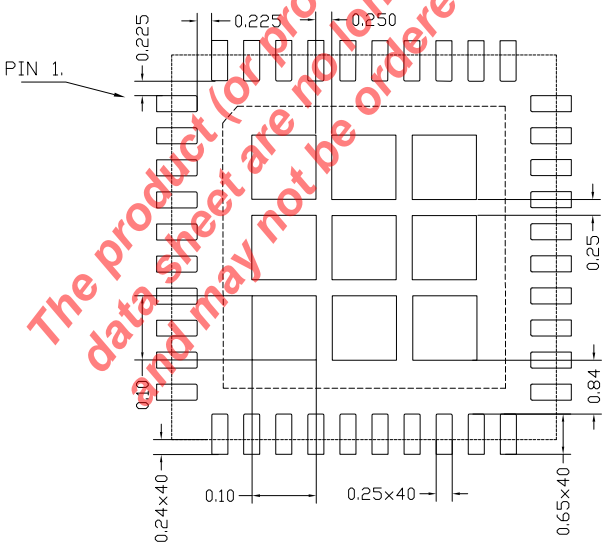
Drawing No.: POD-00000041

Revision: B.2

RECOMMENDED LAND PATTERN AND STENCIL



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000041

Revision: B.2

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REVISION HISTORY

DATE	REVISION	DESCRIPTION
April 2007	P1.0.0	Preliminary Datasheet
June 2007	P1.0.1	Updated pinout.
July 2007	1.0.0	Final Datasheet. Updated DC Electrical characteristics.
October 2007	1.0.1	Updated maximum crystal frequency and external clock frequency in AC Electrical Characteristics.
December 2007	1.0.2	Removed references to the special character detect since that feature is not available in this device.
July 2009	1.0.3	Clarified VCC33 and VCC50 pin descriptions.
April 2018	1.0.4	Update to MaxLinear logo. Update format and Ordering Information.

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