

# DATA COMMUNICATIONS APPLICATION NOTE DAN160

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## MIGRATING FROM THE XR16C2850 TO THE XR16L2750

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#### 1.0 INTRODUCTION

This application note describes the changes necessary and what to consider when migrating from the XR16C2850 to the XR16L2750.

#### 1.1 HARDWARE DIFFERENCES

- The XR16C2850 and XR16L2750 are both available in the 44-pin PLCC and 48-pin TQFP packages. The XR16C2850 is also available in the 40-pin PDIP package but the XR16L2750 is not.
- The XR16C2850 can operate at 3.3 or 5 V only. The XR16L2750 can operate from 2.25 V up to 5.5 V. Also, the XR16L2750 has 5 V tolerant inputs while operating at 3.3 V whereas the XR16C2850 does not.
- The maximum crystal oscillator frequency for the XR16C2850 is 8 MHz at 3.3 V while it is a maximum of 20 MHz for the XR16L2750. The crystal oscillator frequency at 5 V and external clock frequencies are the same and the XR16L2750 has the additional specifications for operating at 2.5 V.
- In the 44-pin PLCC package, the XR16C2850 and XR16L2750 have identical pinouts so they are fully pin-to-pin compatible.
- In the 48-pin TQFP package, the XR16C2850 has 3 additional pins that are not available in the XR16L2750 but the XR16L2750 can still be a direct drop-in. The following table lists the additional pins of the XR16C2850 and how the same functionality of these pins can be implemented in the XR16L2750.

48-TQFP **HARDWARE** XR16C2850 XR16L2750 PIN **CHANGES COMMENTS** PIN NAME PIN NAME NUMBER REQUIRED CLK8/16 24 N.C. None CLK8/16 pin functionality can be selected via EMSR bit-7. CLKSEL N.C. 25 None CLKSEL pin functionality can be selected via MCR bit-7. 37 HDCNTL# N.C. None HDCNTL# pin functionality can be selected via EMSR bit-3.

TABLE 1: PIN DIFFERENCES BETWEEN THE XR16C2850 AND XR16L2750

## 1.2 FIRMWARE DIFFERENCES

The internal registers of the XR16C2850 and XR16L2750 are identical except for a few registers:

- FIFO Control Register (FCR)
  - Bit-0 enables the FIFO for both the XR16C2850 and XR16L2750, but the FIFO sizes are different. The TX and RX FIFOs are 128 bytes deep for the XR16C2850 and are 64 bytes deep for the XR16L2750.
- Enhanced Mode Select Register (EMSR)
  - Bit-7 is not used in the XR16C2850 but it is used in the XR16L2750 to select the 16X or 8X sampling rate. Bit-7 is asserted for 16X sampling (default) and de-asserted for 8X sampling.
  - Bit-6 is not used in the XR16C2850 but it is used in the XR16L2750 to select whether the LSR Interrupt is
    generated immediately when there is a data error in the FIFO or delayed until the data byte with an error is
    being read out of the FIFO.
  - Bit-3 is not used in the XR16C2850 but it is used in the XR16L2750 to invert the polarity of the RS485 halfduplex direction control output signal (RTS#) if necessary.
- Device Identification (DVID) register has a value of 0x12 for the XR16C2850 and 0x0A for the XR16L2750.



### 1.3 REPLACING THE XR16C2850 WITH THE XR16L2750

You can directly replace the XR16C2850 with the XR16L2750 in the 44-pin PLCC and 48-pin TQFP packages. If using the XR16C2850 in the 40-pin PDIP package, then hardware changes will be required since the XR16L2750 is not available in that package.

If using the 8X data sampling rate, BRG prescaler, or RS485 Half-Duplex Control, the software will need to be updated since these functionality control are only implemented in the register bits in the XR16L2750 rather than the hardware pins as available in the XR16C2850. Also, the XR16L2750 has a few additional features such as selecting the LSR interrupt mode and inverting the RS485 polarity that may require some software changes.

In a nutshell, the XR16C2850 and XR16L2750 are very similar devices but with different FIFO sizes and there are a few additional features in the XR16L2750.

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