Data Sheet

COMLINEAR® CLC1008, CLC2008

0.5mA, Low Cost, 2.5 to 5.5V, 75MHz Rail-to-Rail Amplifiers

FEATURES

- 505µA supply current
- 75MHz bandwidth
- Input voltage range with 5V supply: -0.3V to 3.8V
- Output voltage range with 5V supply: 0.07V to 4.86V
- 50V/µs slew rate
- 12nV/√Hz input voltage noise
- 15mA linear output current
- Fully specified at 2.7V and 5V supplies
- Replaces AD8031 in $V_S \leq 5$ applications

APPLICATIONS

- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Signal conditioning
- Medical Equipment
- Portable medical instrumentation

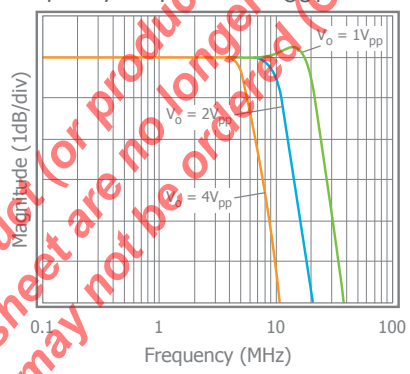
General Description

The COMLINEAR CLC1008 (single) and CLC2008 (dual) offer superior dynamic performance with 75MHz small signal bandwidth and 50V/µs slew rate. These amplifiers use only 505µA of supply current and are designed to operate from a supply range of 2.5V to 5.5V (±1.25 to ±2.75).The combination of low power, high output current drive, and rail-to-rail performance make the CLC1008 and CLC2008 well suited for battery-powered communication/ computing systems.

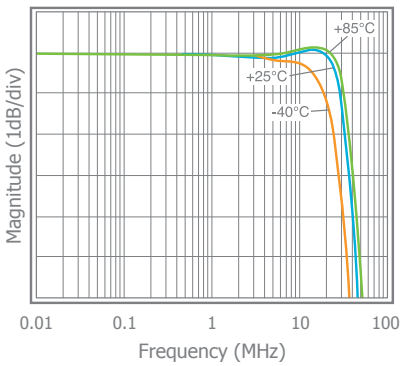
The combination of low cost and high performance make the CLC1008 and CLC2008 suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, and color copiers.

Typical Performance Examples

Frequency Response vs. V_{OUT}



Frequency Response vs. Temperature



Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1008IST5X	SOT23-5	Yes	Yes	-40°C to +85°C	Reel
CLC2008ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

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48720 Kato Road, Fremont CA 94538, USA

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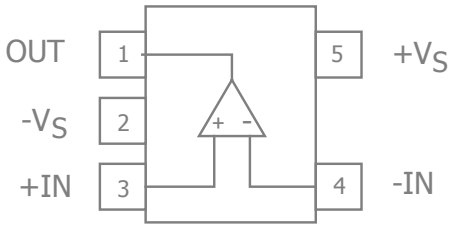
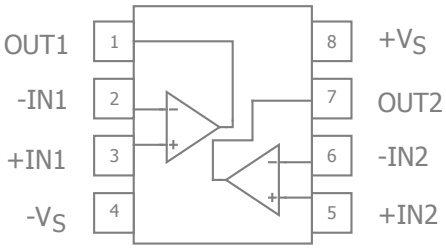
CLC1008 Pin Configuration



CLC1008 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

CLC2008 Pin Configuration



CLC2008 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	6	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V
Continuous Output Current	-30	30	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		5.5	V

Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.05V_{pp} , R_f = 0		65		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} < 0.2V_{pp}		30		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		12		MHz
GBWP	Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		28		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%)		7.5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		60		ns
OS	Overshoot	V_{OUT} = 1V step		10		%
SR	Slew Rate	2V step, G = -1		40		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		-67		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		-72		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		65		dB
e_n	Input Voltage Noise	> 10kHz		12		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			0		mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current			1.2		µA
dI_b	Average Drift			3.5		nA/°C
I_{OS}	Input Offset Current			30		nA
PSRR	Power Supply Rejection Ratio (1)	DC	60	66		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		98		dB
I_S	Supply Current	per channel		470		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		9		MΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_S - 1.5		74		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to V_S / 2		0.09 to 2.53		V
		R_L = 10kΩ to V_S / 2		0.05 to 2.6		V
I_{OUT}	Output Current			±15		mA
I_{SC}	Short Circuit Output Current			±30		mA

Notes:

1. 100% tested at 25°C

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.05V_{pp} , R_f = 0		75		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} < 0.2V_{pp}		35		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		15		MHz
GBWP	Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		33		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%)		6		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		60		ns
OS	Overshoot	V_{OUT} = 1V step		12		%
SR	Slew Rate	2V step, G = -1		50		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		-64		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		-62		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		60		dB
e_n	Input Voltage Noise	> 10kHz		12		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage (1)		-5	-1	5	mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current (1)		-3.5	1.2	3.5	µA
dI_b	Average Drift			3.5		nA/°C
I_{OS}	Input Offset Current (1)			30	350	nA
PSRR	Power Supply Rejection Ratio (1)	DC	60	66		dB
A_{OL}	Open-Loop Gain (1)	V_{OUT} = V_S / 2	65	80		dB
I_S	Supply Current (1)	per channel		505	620	µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		9		MΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio (1)	DC, V_{CM} = 0V to V_S - 1.5	65	74		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to V_S / 2 (1)	0.2 to 4.65	0.13 to 4.73		V
		R_L = 10kΩ to V_S / 2		0.08 to 4.84		V
I_{OUT}	Output Current			±15		mA
I_{SC}	Short Circuit Output Current			±30		mA

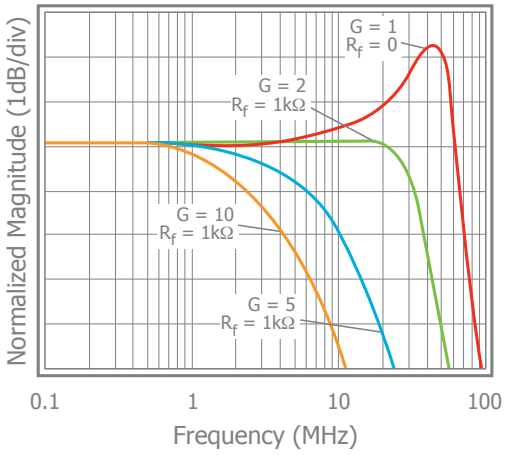
Notes:

1. 100% tested at 25°C

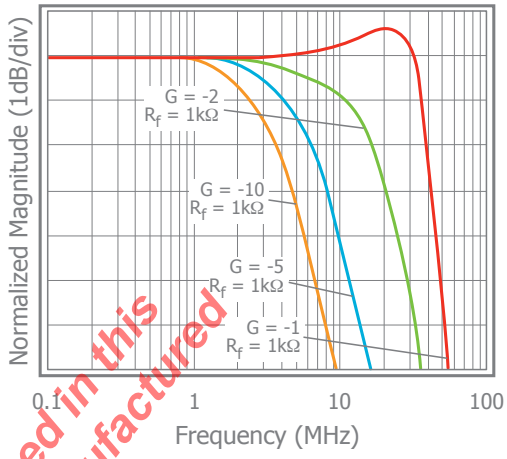
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

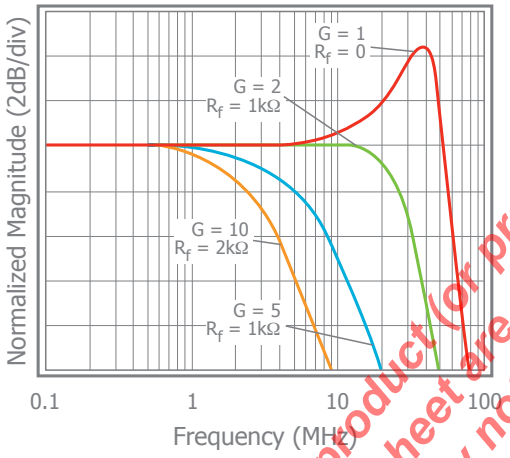
Non-Inverting Frequency Response at V_S = 5V



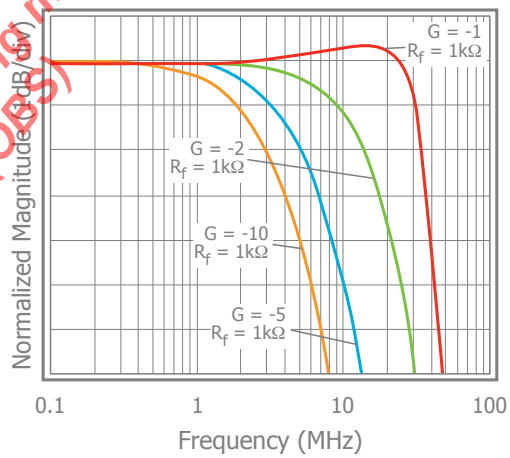
Inverting Frequency Response at V_S = 5V



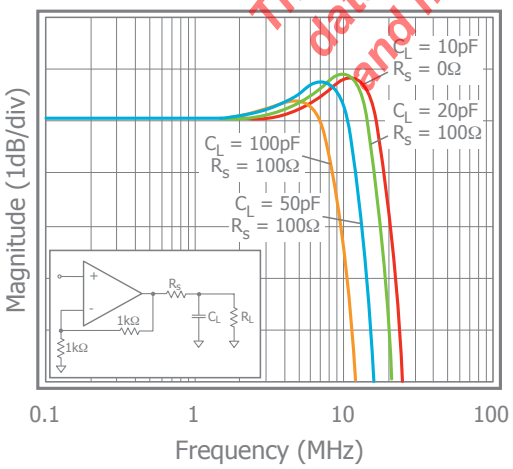
Non-Inverting Frequency Response



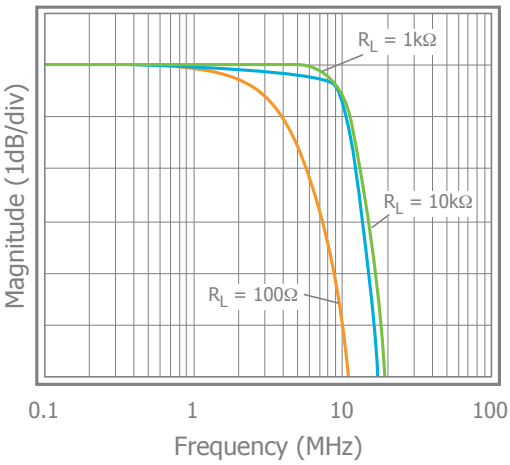
Inverting Frequency Response



Frequency Response vs. C_L



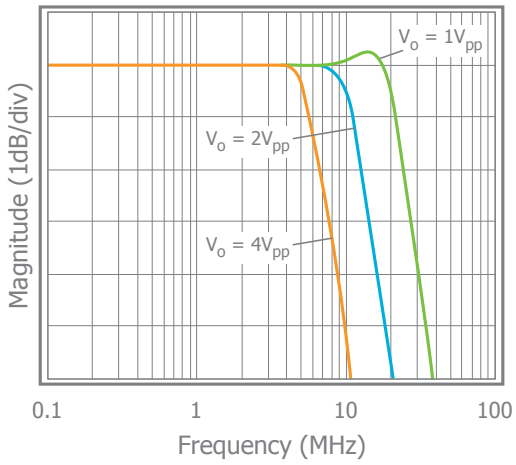
Frequency Response vs. R_L



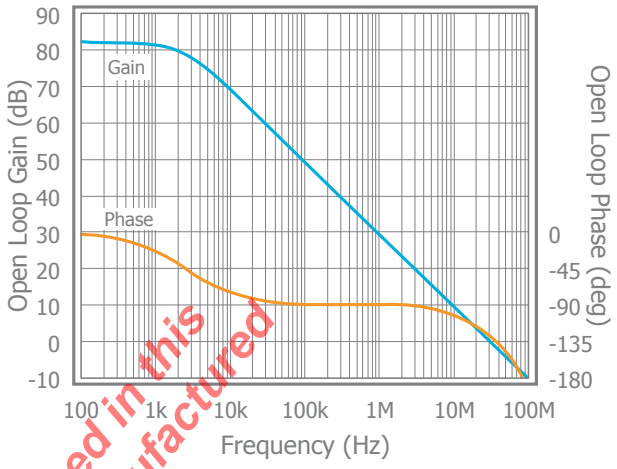
Typical Performance Characteristics

T_A = 25°C, V_s = +5V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

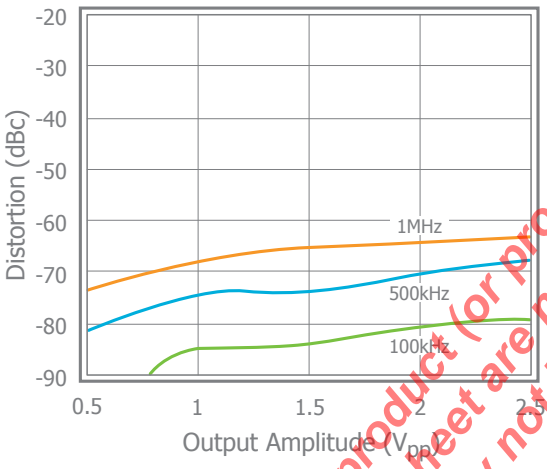
Frequency Response vs. V_{OUT}



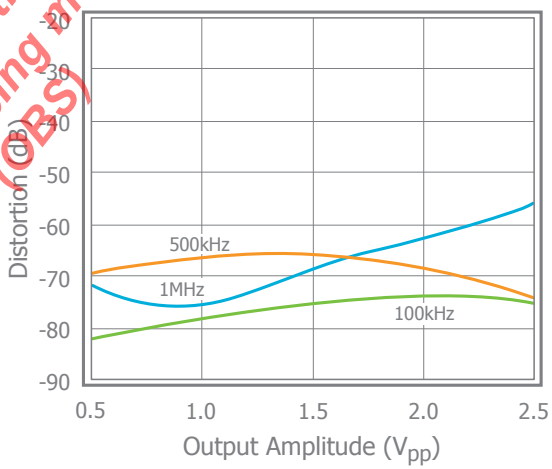
Open Loop Gain & Phase vs. Frequency



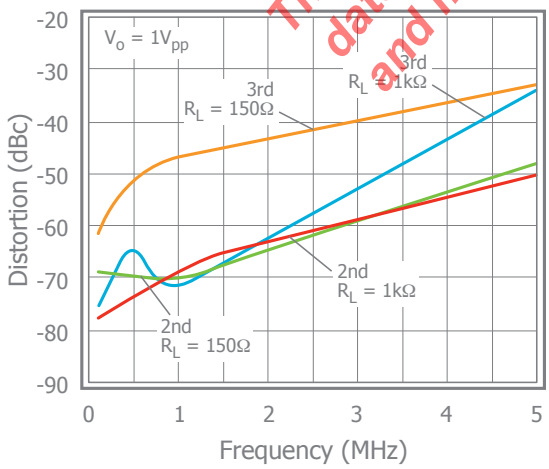
2nd Harmonic Distortion vs. V_{OUT}



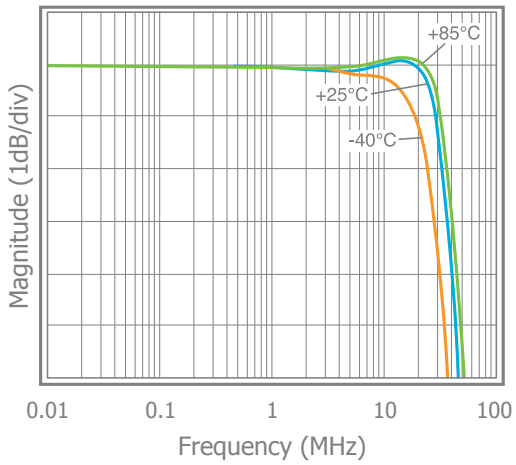
3rd Harmonic Distortion vs. V_{OUT}



2nd & 3rd Harmonic Distortion



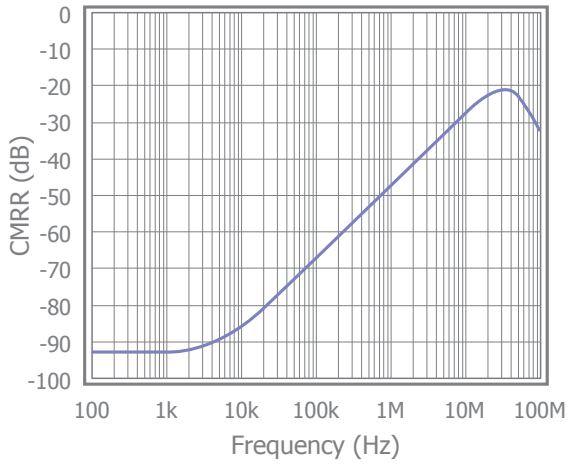
Frequency Response vs. Temperature



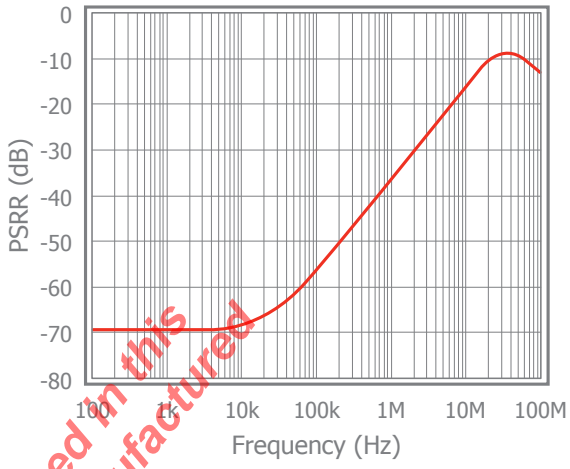
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

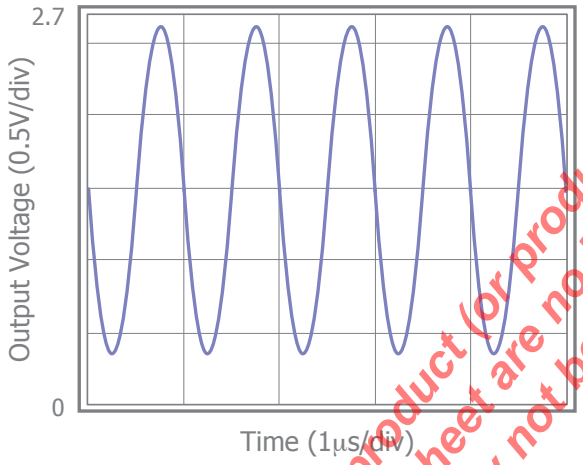
CMRR



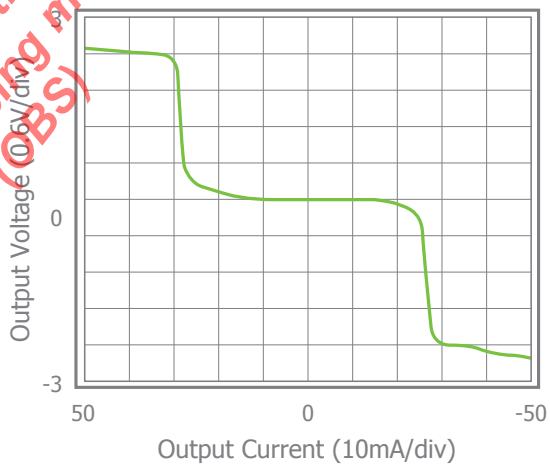
PSRR



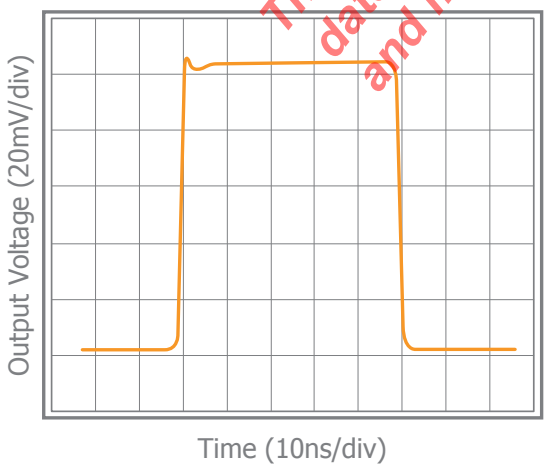
Output Swing



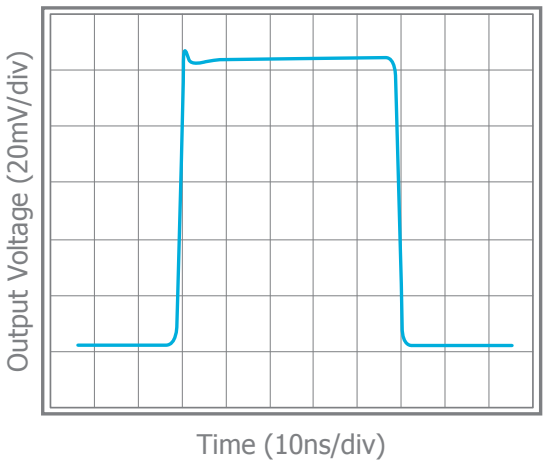
Output Voltage vs. Output Current



Small Signal Pulse Response



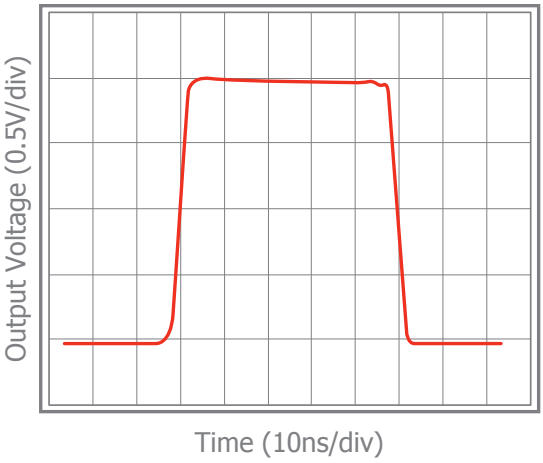
Small Signal Pulse Response at V_S = 5V



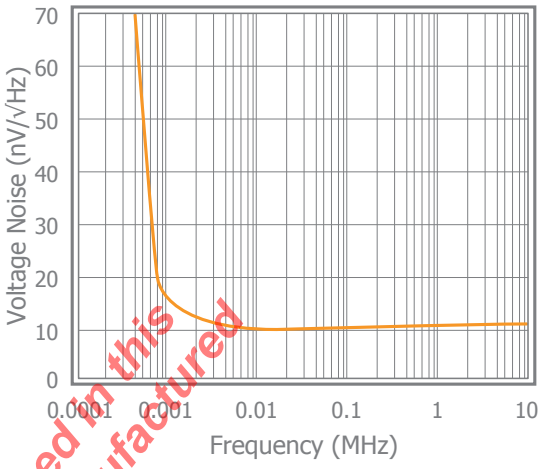
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =1kΩ, R_L = 1kΩ to V_S/2, G = 2; unless otherwise noted.

Large Signal Pulse Response at V_S = 5V



Input Voltage Noise



Application Information

General Description

The CLC1008 family are a single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process. The CLC1008 offers 75MHz unity gain bandwidth, 50V/µs slew rate, and only 505µA supply current. It features a rail-to-rail output stage and is unity gain stable.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applicaitons.

The common mode input range extends to 300mV below ground in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

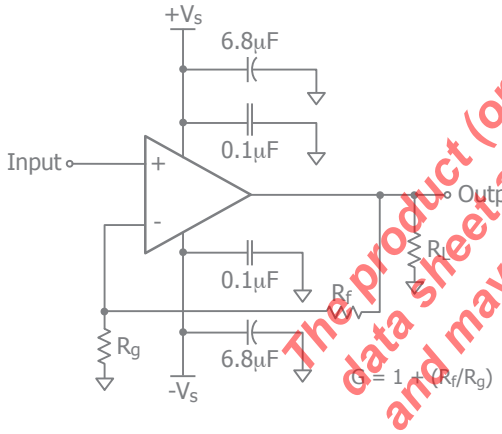


Figure 1. Typical Non-Inverting Gain Circuit

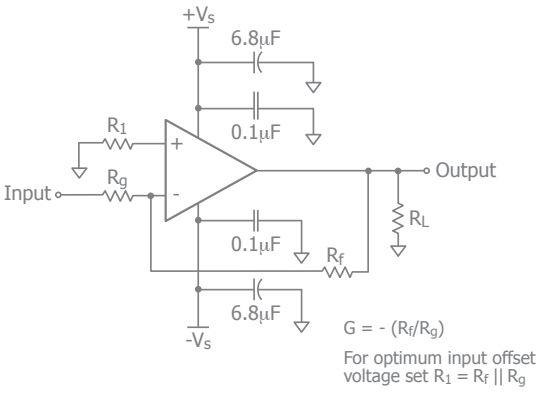


Figure 2. Typical Inverting Gain Circuit

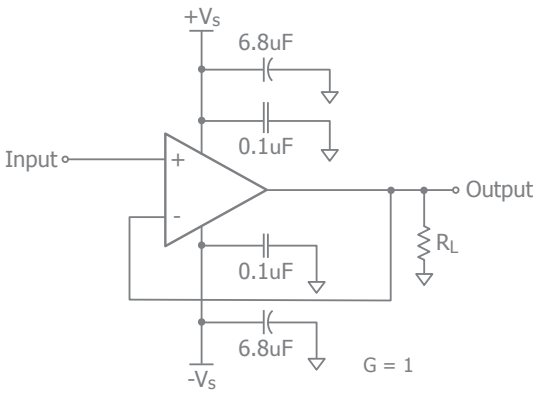


Figure 3. Unity Gain Circuit

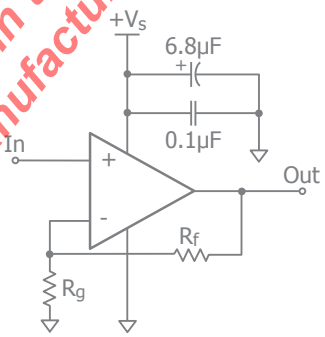


Figure 4. Single Supply Non-Inverting Gain Circuit

For optimum response at a gain of +2, a feedback resistor of 1kΩ is recommended. Figure 5 illustrates the CLC1008 frequency response with both 1kΩ and 2kΩ feedback resistors.

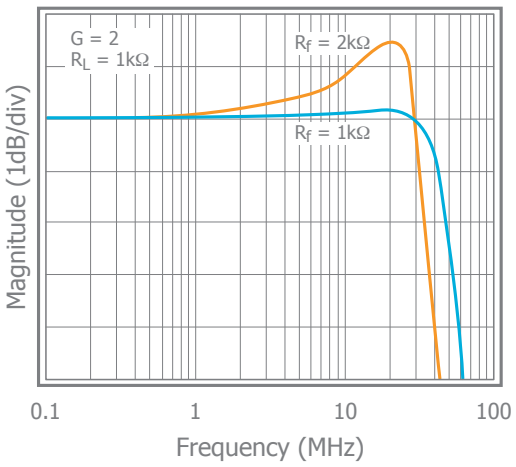


Figure 5. Frequency Response vs. R_f

Power Dissipation

Power dissipation should not be a factor when operating under the stated 1k ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC1008 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

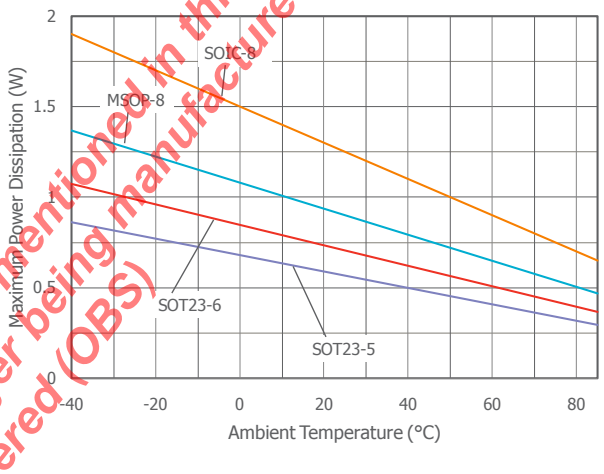


Figure 6. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 7.

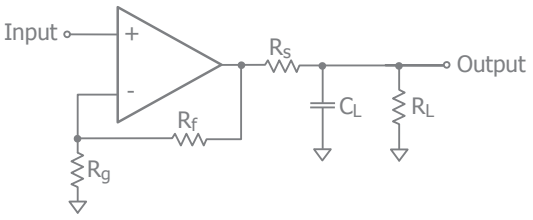


Figure 7. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in

approximately <1dB peaking in the frequency response. The Frequency Response vs. C_L plot, on page 4, illustrates the response of the CLCx008.

C_L (pF)	R_S (Ω)	-3dB BW (kHz)
10pF	0	22
20pF	100	19
50pF	100	12
100pF	100	10.2

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1008 and CLC2008 will typically recover in less than 20ns from an overdrive condition. Figure 8 shows the CLC1008 in an overdriven condition.

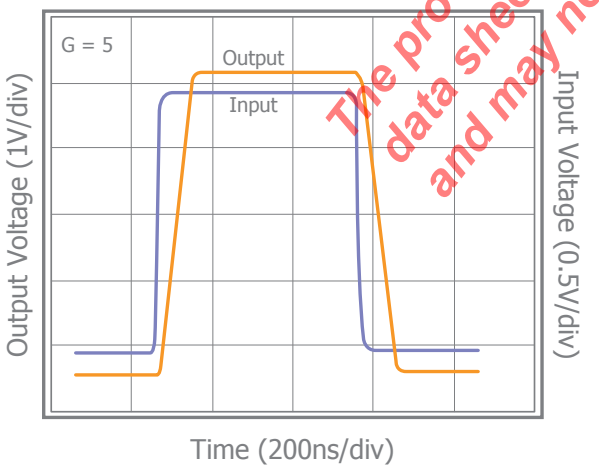


Figure 8. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1008 in SOT23
CEB003	CLC1008 in SOIC
CEB006	CLC2008 in SOIC
CEB010	CLC2008 in MSOP

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

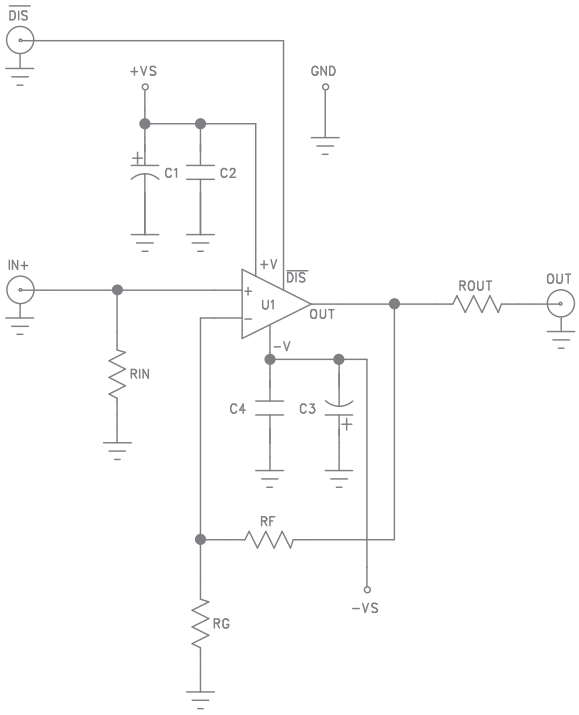


Figure 8. CEB002 & CEB003 Schematic

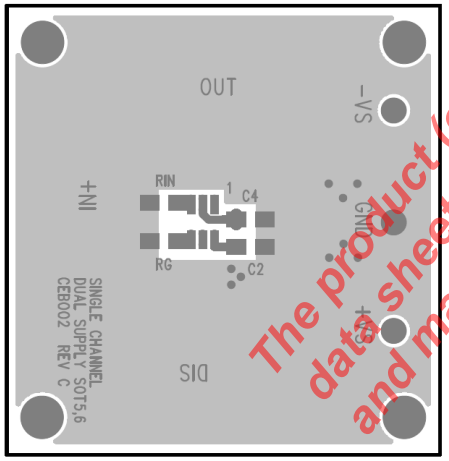


Figure 9. CEB002 Top View

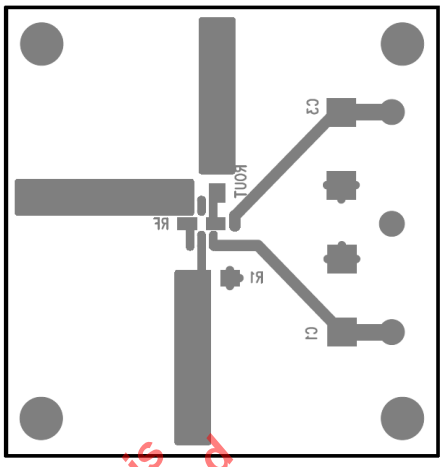


Figure 10. CEB002 Bottom View

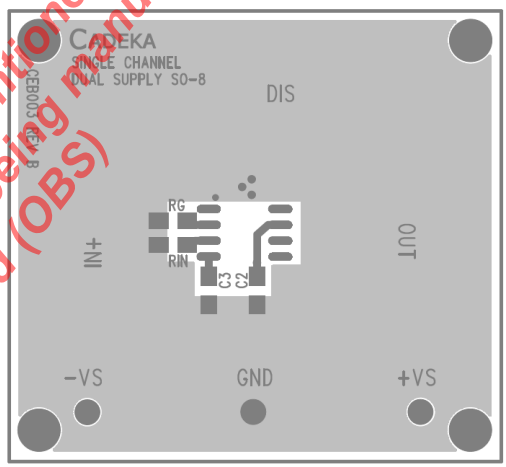


Figure 11. CEB003 Top View

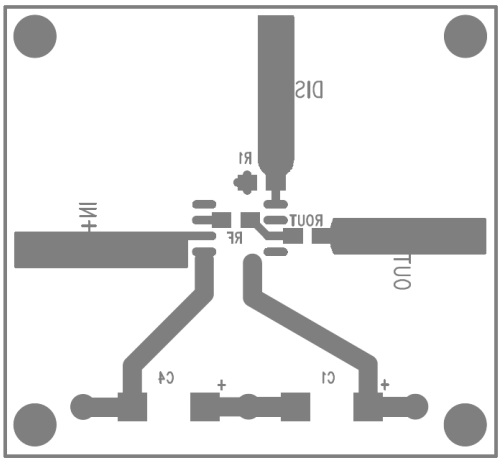


Figure 12. CEB003 Bottom View

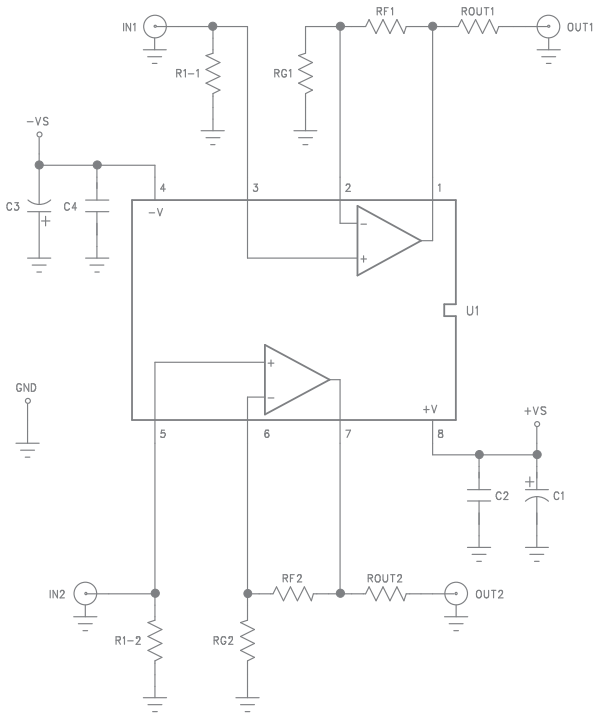


Figure 11. CEB006 & CEB010 Schematic

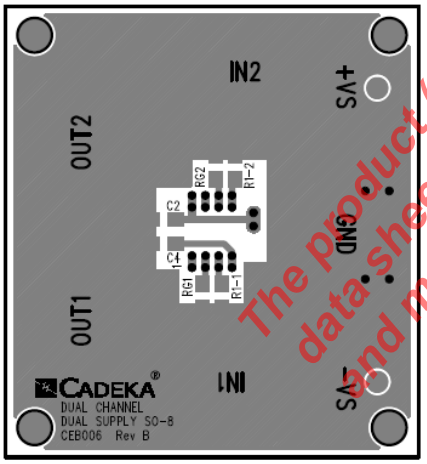


Figure 12. CEB006 Top View

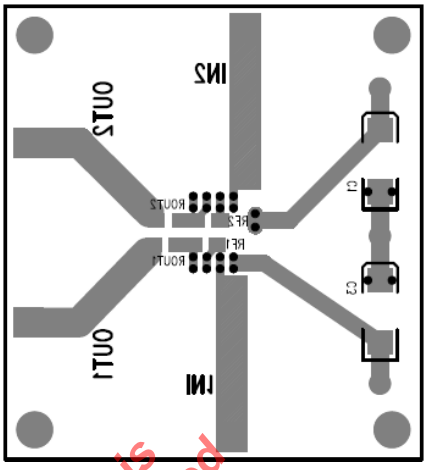


Figure 13. CEB006 Bottom View

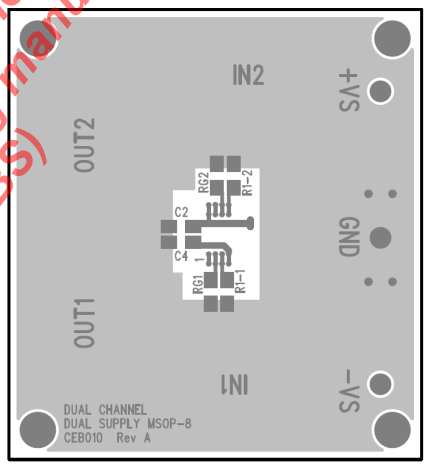


Figure 15. CEB010 Top View

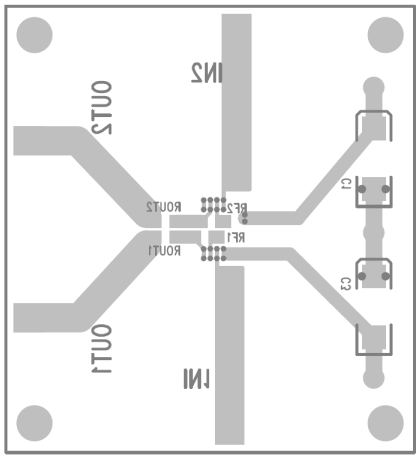
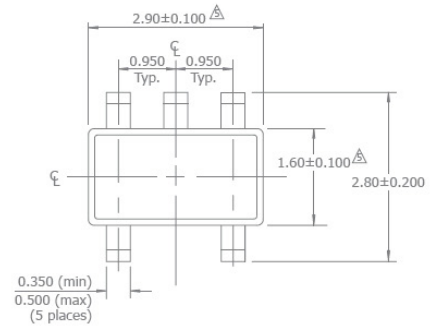


Figure 16. CEB010 Bottom View

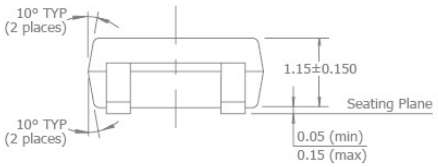
Mechanical Dimensions

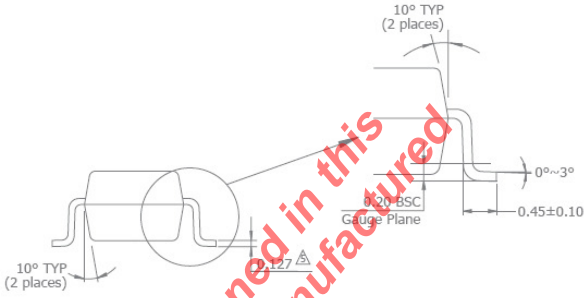
SOT23-5 Package



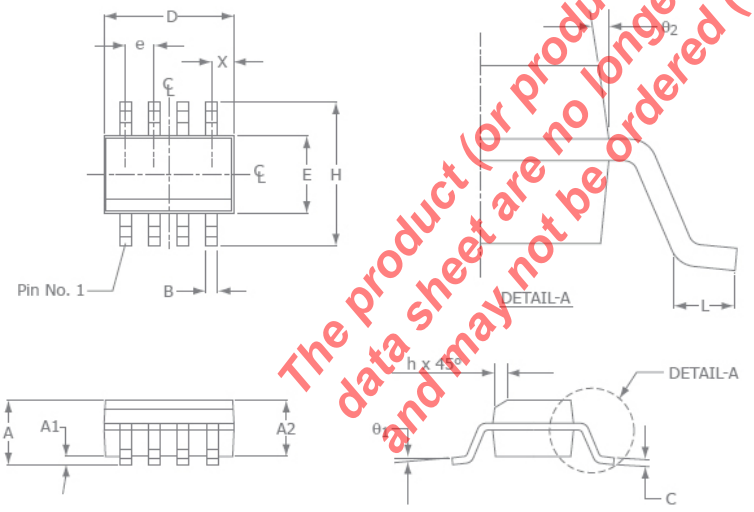
NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.
5. Dimension are exclusive of mold flash and gate burr.
6. Dimension are exclusive of solder plating.





SOIC-8



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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