A New Direction in Mixed-Signal

CLC1020

General Purpose, Rail to Rail Output Amplifier

Rail to Rail Amplifiers

FEATURES

- 127µA supply current
- 2.1MHz gain bandwidth
- Input voltage range with 5V supply: -0.4V to 4.3V
- Output voltage range with 5V supply: 0.01V to 4.99V
- 2.7V/µs slew rate
- 0.7pA bias current
- 0.1mV input offset voltage
- No crossover distortion
- Fully specified at 2.7V and 5V supplies
- Pb-free TSOT-5

APPLICATIONS

- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Medical Equipment
- Portable medical instrumentation

General Description

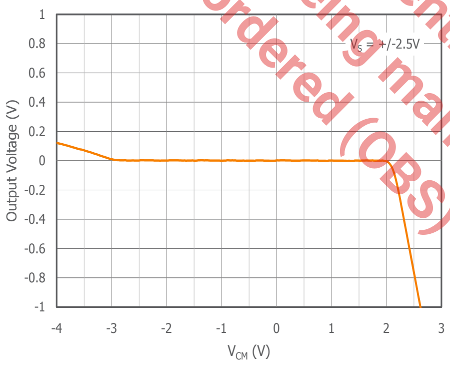
The COMLINEAR CLC1020 is a single channel, high-performance, voltage feedback amplifier. The CLC1020 provides 2.1MHz gain bandwidth product and 2.7V/µs slew rate making it well suited for high-performance battery powered-systems. This COMLINEAR high-performance amplifier also offers low input offset voltage and low bias current.

The COMLINEAR CLC1020 consumes only 127µA supply current and is designed to operate from a supply range of 2.7V to 5.5V (±1.35 to ±2.75). The input voltage range extends 400mV below the negative rail and 700mV below the positive rail. The CLC1020 amplifier operates over the extended temperature range of -40°C to +125°C.

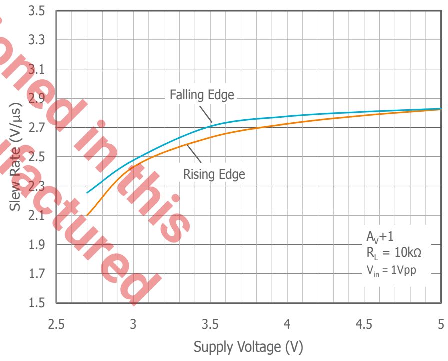
The CLC1020 is packaged in the space saving TSOT-5 package. The TSOT-5 package is pin compatible with the SOT23-5 package.

Typical Performance Examples

Vout vs. Vcm



Slew Rate vs. Supply Voltage

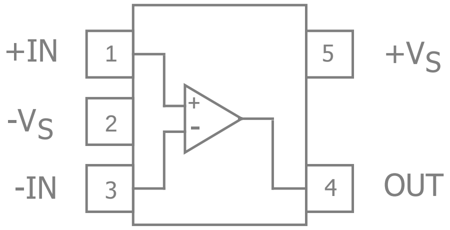


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1020IST5X	TSOT-5	Yes	Yes	-40°C to +125°C	Reel

Moisture sensitivity level for all parts is MSL-1.

CLC1020 Pin Configuration



CLC1020 Pin Assignments

Pin No.	Pin Name	Description
1	+IN	Output
2	$-V_S$	Negative supply
3	-IN	Positive input
4	OUT	Negative input
5	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the “Absolute Maximum Ratings”. The device should not be operated at these “absolute” limits. Adhere to the “Recommended Operating Conditions” for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage		7	V
Input Voltage Range	-V_S-0.4V	+V_S	V
Continuous Output Current	Output is protected against momentary short circuit		

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead TSOT		221		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	TSOT-5
Human Body Model (HBM)	2kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+125	°C
Supply Voltage Range	2.7		5.5	V

Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = 10kΩ, R_L=10kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	Gain Bandwidth Product	V_{OUT}=0.2V_{pp}, C_L = 200 pF, R_L = 10kΩ, G=11		2		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.2V_{pp} , R_L = 10kΩ, G=1		1.6		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.2V_{pp}, R_L = 10kΩ, G=2		836		kHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}, R_L = 10kΩ, G=2		540		kHz
G_m	Gain Margin	G=1		22		dB
Φ_m	Phase Margin	G=1		82		°
Time Domain Response						
t_R , t_S	Rise and Fall Time	V_{OUT} = 2V step, R_L = 10kΩ		840		ns
t_S	Settling Time to 0.1%	V_{OUT} =2V_{pp}, R_L = 10kΩ		1.6		µs
OS	Overshoot	V_{OUT}=2V_{pp}, R_L = 10kΩ		5.5		%
SR	Slew Rate	V_{OUT}=2V_{pp}, R_L = 10kΩ		2.3		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 10kΩ		-61		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 10kΩ		-70		dBc
THD	Total Harmonic Distortion	2V_{pp}, 10kHz, G=1, R_L = 10kΩ		0.094		%
e_n	Input Voltage Noise	f=100Hz		54		nV/√Hz
		f=1kHz		30		nV/√Hz
		f=10kHz		17		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			0.53		mV
dV_{IO}	Average Drift			2.1		µV/°C
I_b	Input Bias Current			0.5		pA
I_{os}	Input Offset Current			0.1		pA
PSRR	Power Supply Rejection Ratio	DC		73		dB
I_S	Supply Current			111		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting Input		29		GΩ
C_{IN}	Input Capacitance	Non-inverting		2.4		pF
CMIR	Common Mode Input Range	For V_{CM}≤50dB		-0.4 to 2.0		V
CMRR	Common Mode Rejection Ratio	DC , V_{cm}=0V to 1.7V		70.5		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ		0.02 to 2.63		V
		R_L = 10kΩ		0.01 to 2.68		V
I_{SC}	Short-Circuit Output Current	Sourcing, V_{OUT} = 0V, G=1		18		mA
		Sinking, V_{OUT} = 2.7V, G=1		58		mA

Notes:

1. 100% tested at 25°C

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = 10kΩ, R_L=10kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	Gain Bandwidth Product	V_{OUT}=0.2V_{pp}, C_L = 200pF, R_L = 10kΩ, G=11		2.1		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.2V_{pp} , R_L = 10kΩ, G=1		1.8		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.2$V_{pp,}$ R_L = 10kΩ, G=2		907		kHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2$V_{pp,}$ R_L = 10kΩ, G=2		576		Hz
G_m	Gain Margin	G=1		18		dB
Φ_m	Phase Margin	G=1		90		°
Time Domain Response						
t_R , t_S	Rise and Fall Time	V_{OUT} =2V step, R_L = 10kΩ		670		ns
t_S	Settling Time to 0.1%	V_{OUT} =2V_{pp}, R_L = 10kΩ		1.6		µs
OS	Overshoot	V_{OUT}=2V_{pp}, R_L = 10kΩ		5.9		%
SR	Slew Rate	V_{OUT}=4V_{pp}, R_L = 10kΩ		2.7		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT}=2V_{pp}, 10kHz, R_L = 10kΩ		-67		dBc
HD3	3rd Harmonic Distortion	V_{OUT}=2V_{pp}, 10kHz, R_L = 10kΩ		-68		dBc
THD	Total Harmonic Distortion	V_{OUT}=2V_{pp}, 10kHz, R_L = 10kΩ		0.057		%
e_n	Input Voltage Noise	f=100Hz		57		nV/√Hz
		f=1kHz		30		nV/√Hz
		f=100kHz		18		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage(1)			0.1	6	mV
dV_{IO}	Average Drift			1.1		µV/°C
I_b	Input Bias Current			0.7	250	pA
I_{os}	Input Offset Current			0.1		pA
PSRR	Power Supply Rejection Ratio (1)	DC	60	73		dB
A_{OL}	Open-Loop Gain (1)	V_{OUT} = V_S / 2	70	122		dB
I_S	Supply Current (1)			127	170	µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting Input		40		GΩ
C_{IN}	Input Capacitance	Non-inverting Input		2.2		pF
CMIR	Common Mode Input Range	For V_{CM}≤50dB	-0.3	-0.4 to 4.3	4.2	V
CMRR	Common Mode Rejection Ratio (1)	DC , V_{cm}= 0V to 4V	60	67		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ	4.93	4.96 to 0.02	0.04	V
		R_L = 10kΩ (1)	4.97	4.99 to 0.01	0.02	V
I_{SC}	Short-Circuit Output Current	Sourcing, V_{OUT} = 0V, G=1	30	69		mA
		Sinking, V_{OUT} = 5V, G=1	80	150		mA

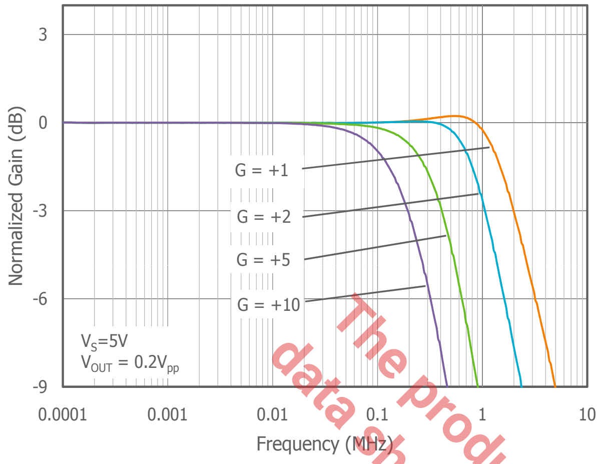
Notes:

1. 100% tested at 25°C

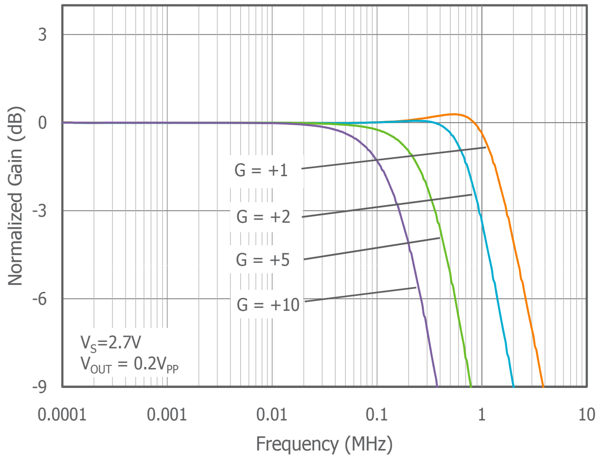
Typical Performance Characteristics - Continued

$T_A = 25°C$, $V_S = +5V$, $R_f = R_g = 10k\Omega$, $R_L = 10k\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

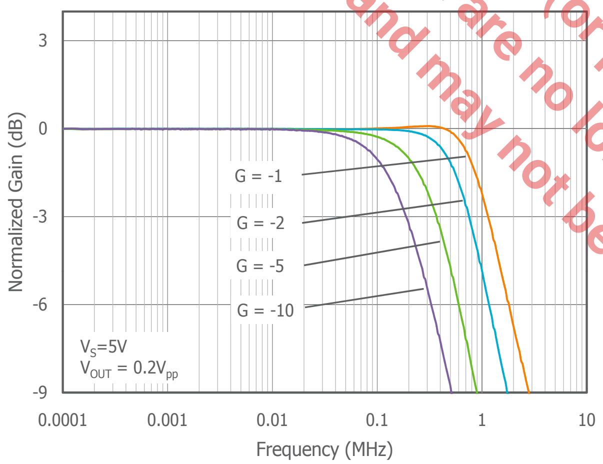
Non-Inverting Freq. Resp. +5V



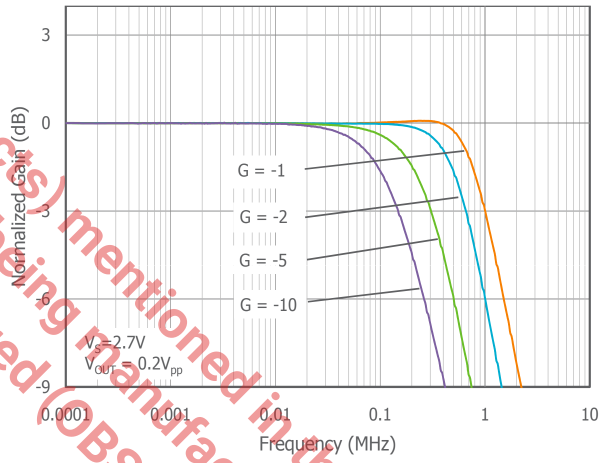
Non-Inverting Freq. Resp. +2.7V



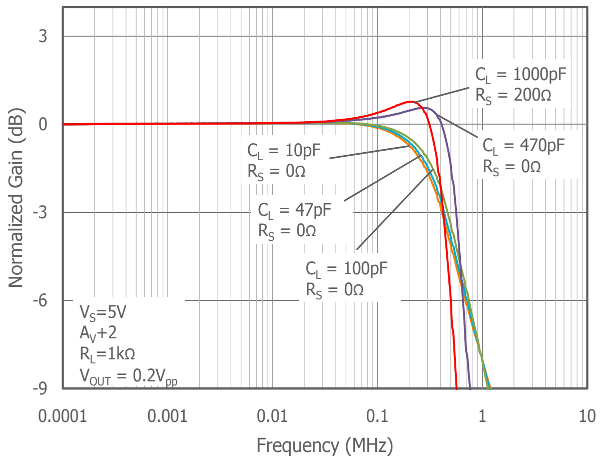
Inverting Freq. Resp. +5V



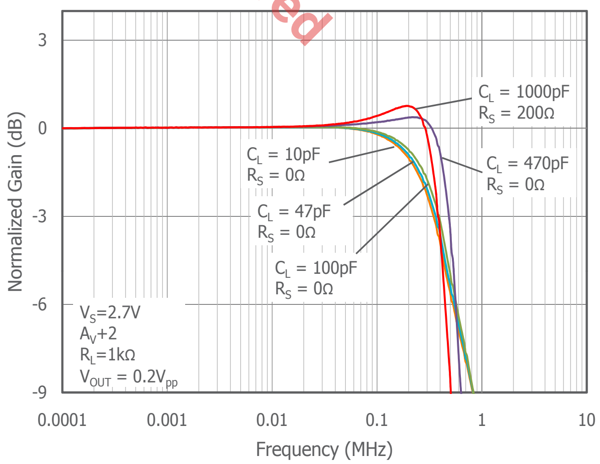
Inverting Freq. Resp. +2.7V



Freq. Resp. vs. C_L R_L=1kΩ +5V

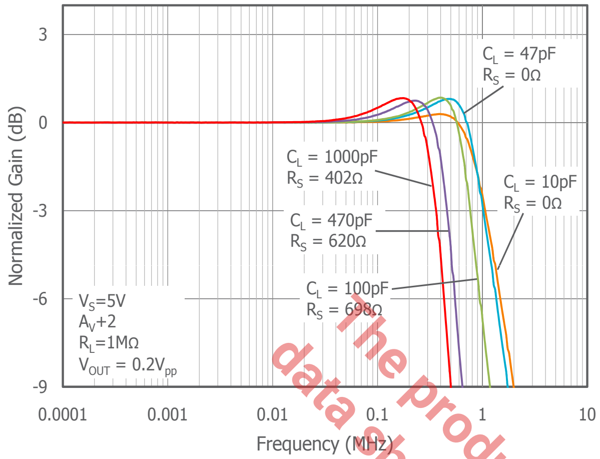


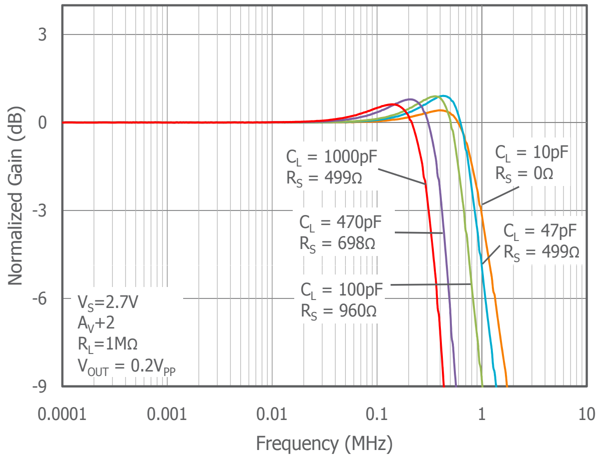
Freq. Resp. vs. C_L R_L=1kΩ +2.7V

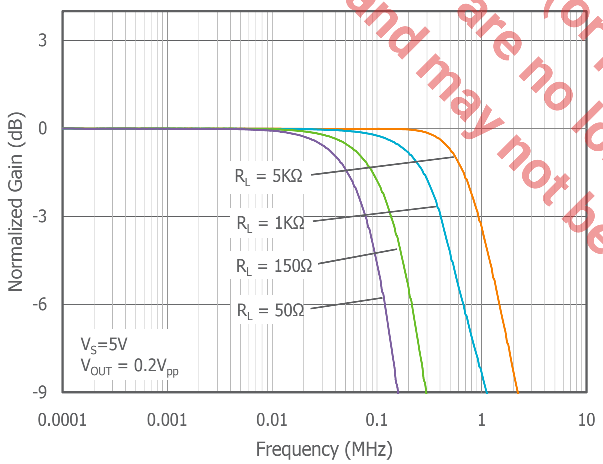


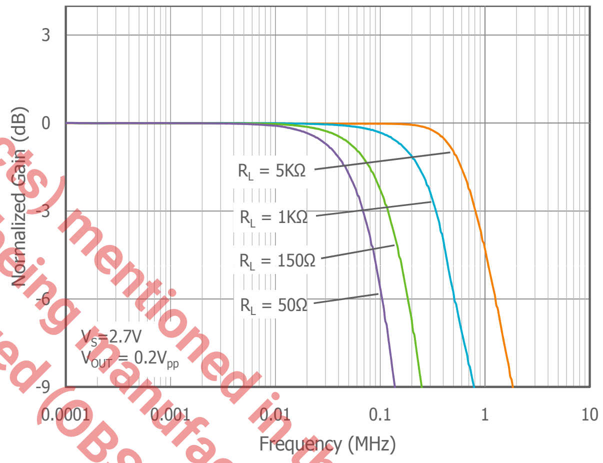
Typical Performance Characteristics - Continued

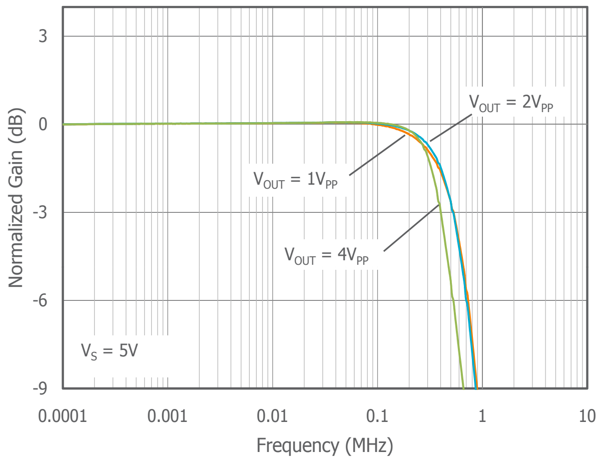
T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to $V_S/2$, G = 2; unless otherwise noted.

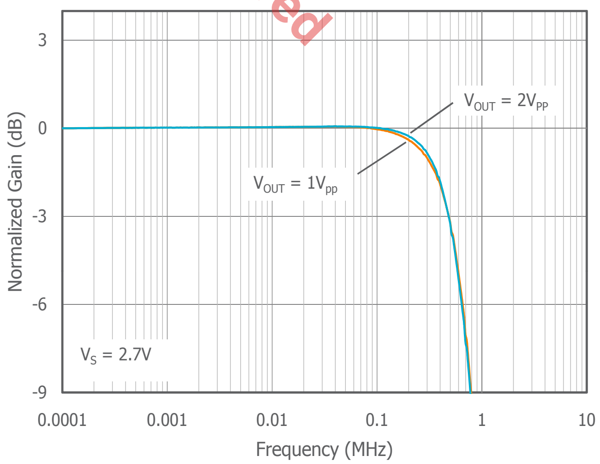








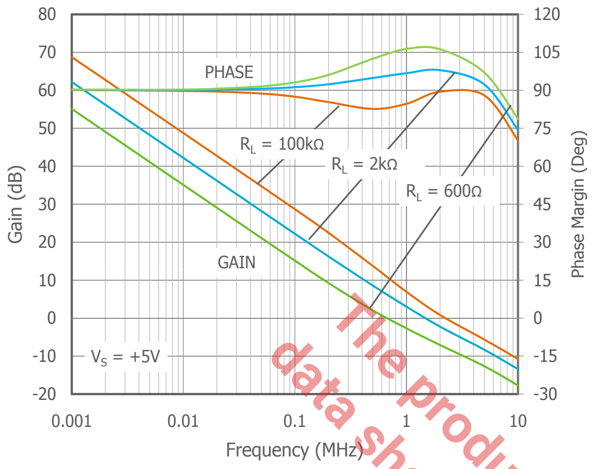




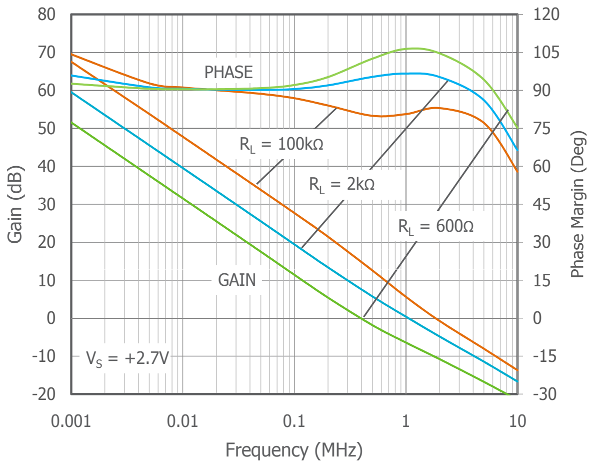
Typical Performance Characteristics - Continued

$T_A = 25°C$, $V_S = +5V$, $R_f = R_g = 10k\Omega$, $R_L = 10k\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

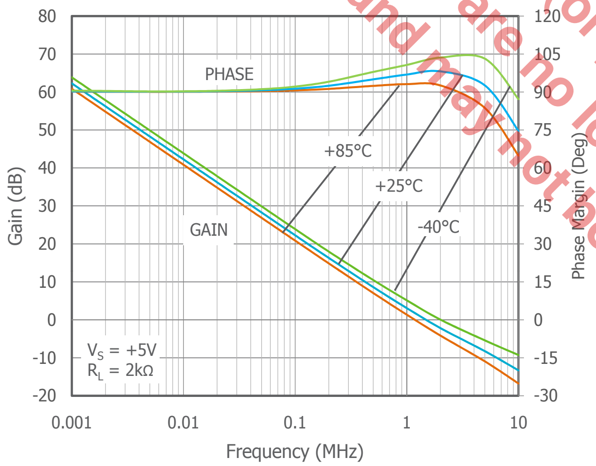
Open Loop Gain & Phase vs. Freq. +5V



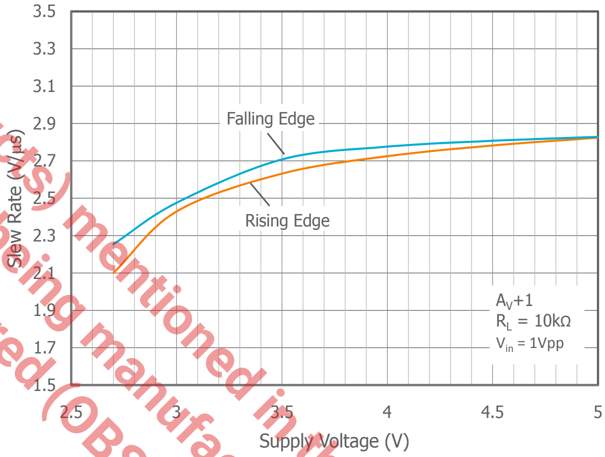
Open Loop Gain & Phase vs. Freq. +2.7V



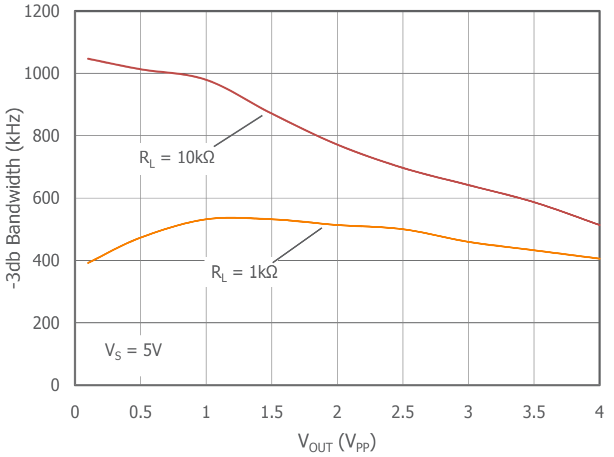
Open Loop Gain & Phase vs. Temp +5V



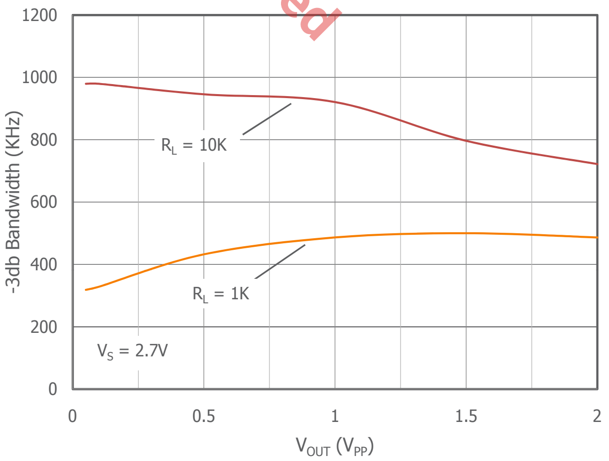
Slew Rate vs. Supply Voltage



-3db BW vs Output Amplitude +5V



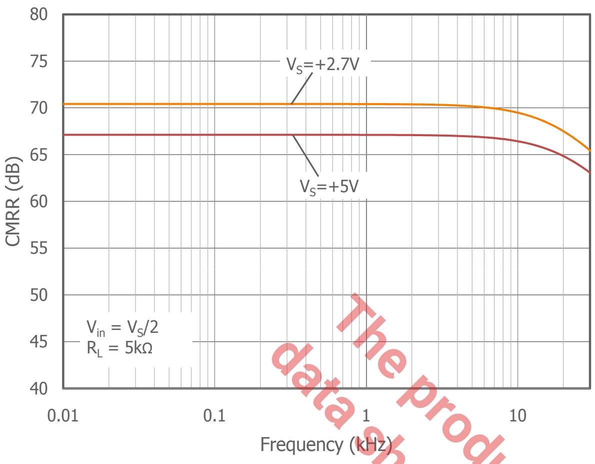
-3db BW vs Output Amplitude +2.7V



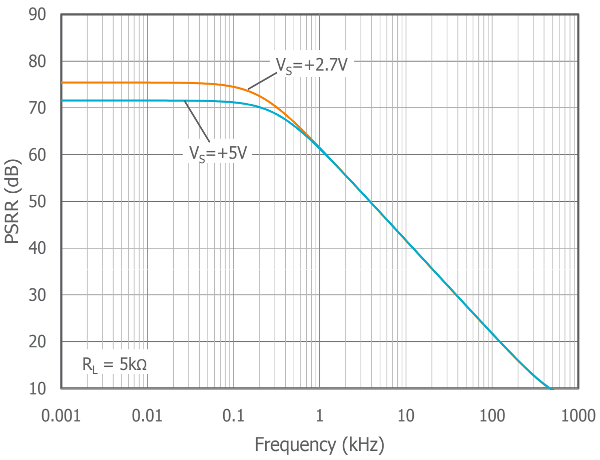
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

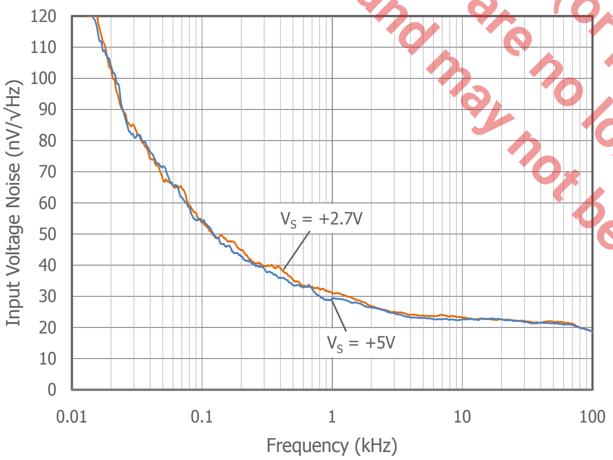
CMRR vs. Freq.



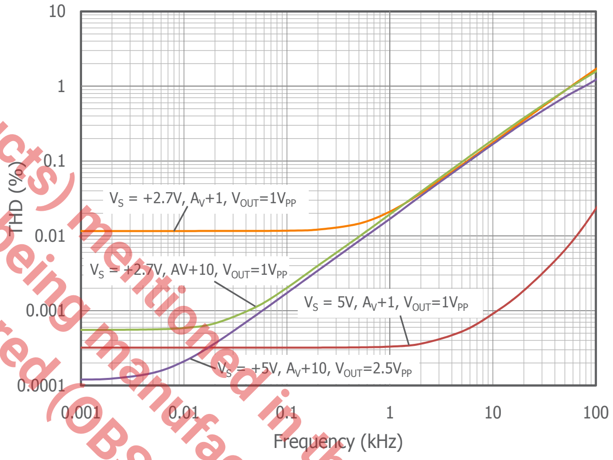
PSRR vs. Freq.



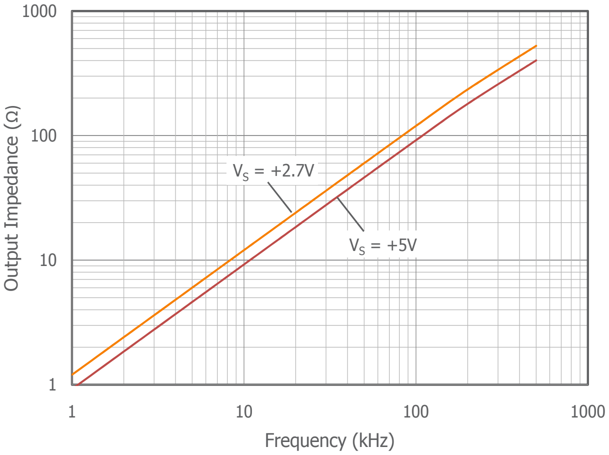
Input Voltage Noise vs. Freq.



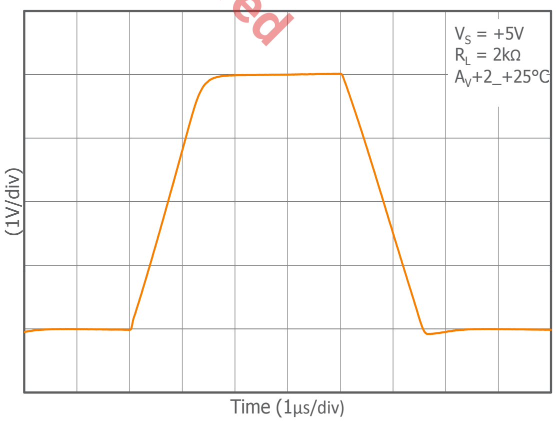
THD vs. Freq.



Output Impedance vs. Freq.



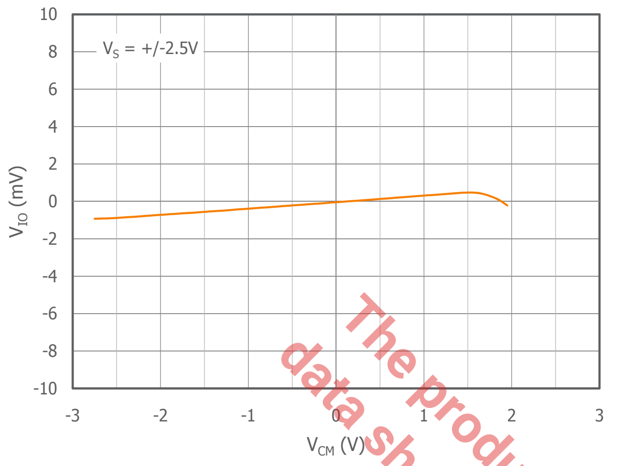
Large Signal Pulse Response



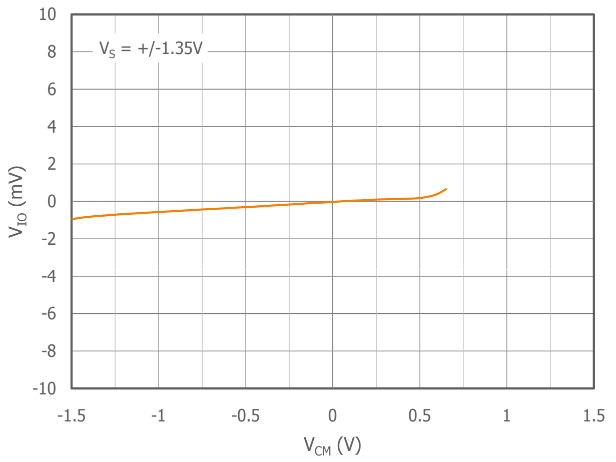
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

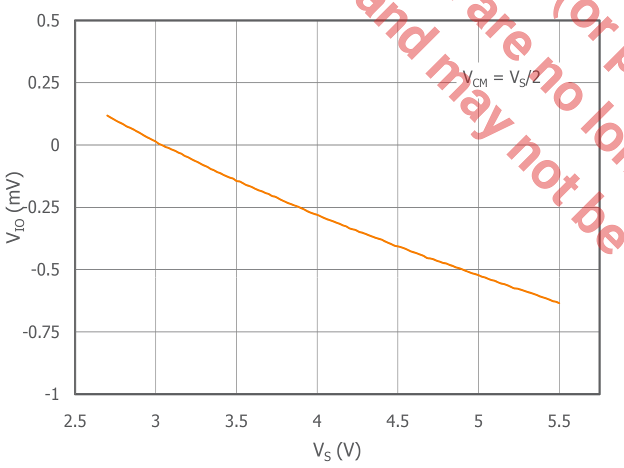
V_{IO} vs. CMR +5V



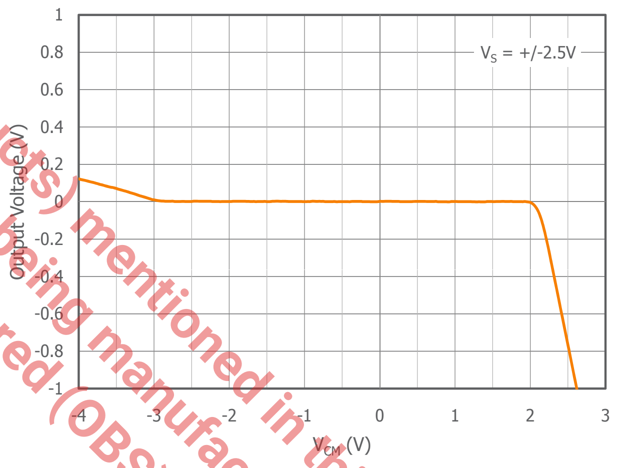
V_{IO} vs. CMR 2.7V



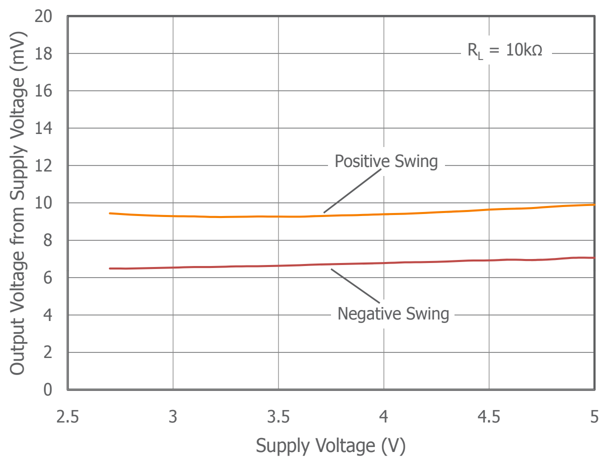
V_{IO} vs. Supply Voltage



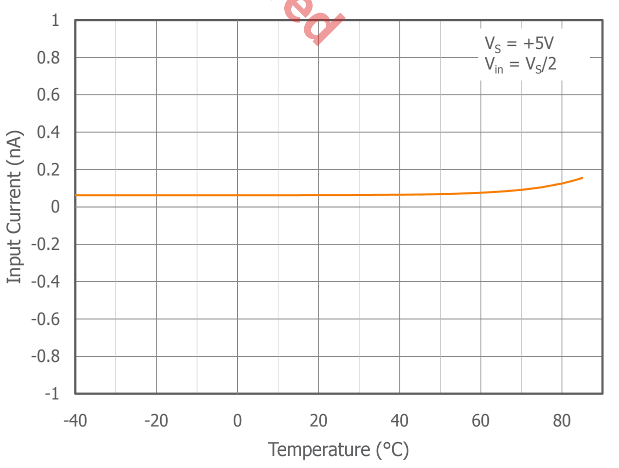
V_{OUT} vs. V_{CM} +5V



Output Swing vs. Supply Voltage



Input Current vs. Temperature



Application Information

General Description

The CLC1020 is a single supply, general purpose, voltage-feedback amplifier fabricated on a CMOS process. The CLC1020 offers 2.1MHz gain bandwidth product, 2.7V/µs slew rate, and only 127µA supply current. It features a rail to rail output stage and is unity gain stable.

The common mode input range extends to 400mV below ground and to 700mV below Vs. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time. Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications

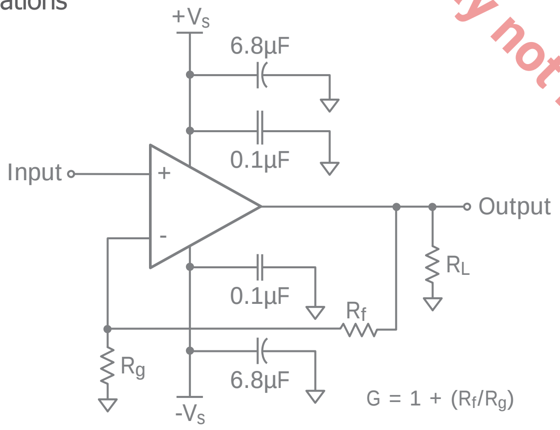
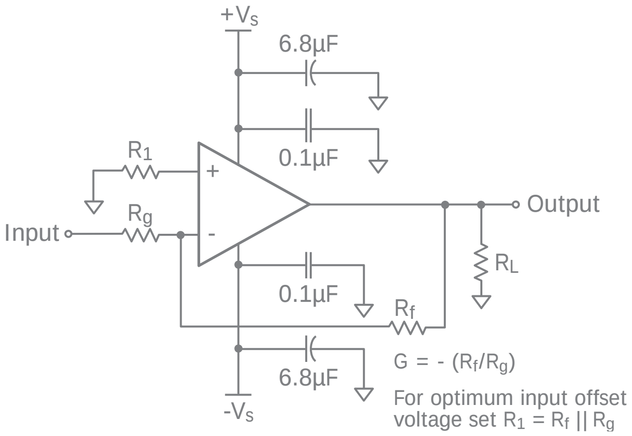


Figure 1. Typical Non-Inverting Gain Circuit



$G = -(R_f/R_g)$

For optimum input offset voltage set $R_1 = R_f \,||\, R_g$

Figure 2. Typical Inverting Gain Circuit

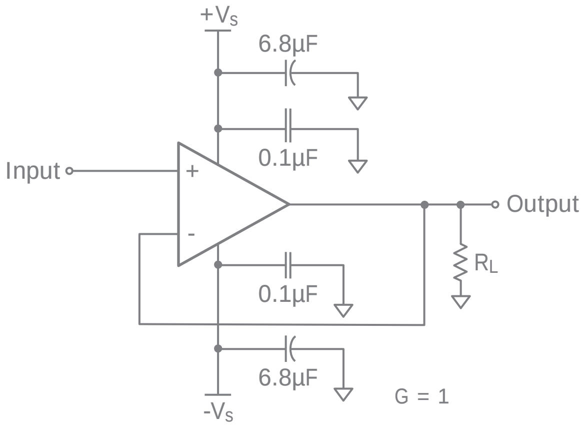


Figure 3. Unity Gain Circuit

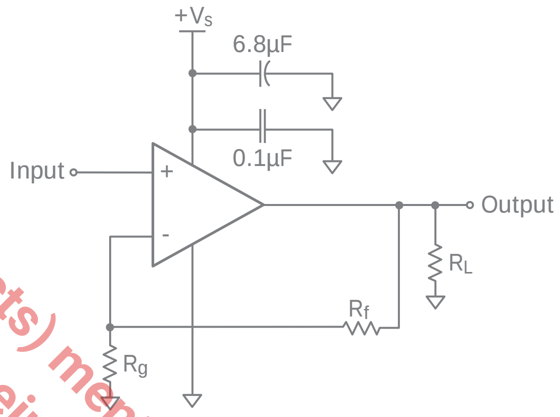


Figure 4. Single Supply Non-Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value ThetaJA (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}{}^{2})/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{SUPPLY}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or Vsupply/2.

The CLC1020 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions.

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

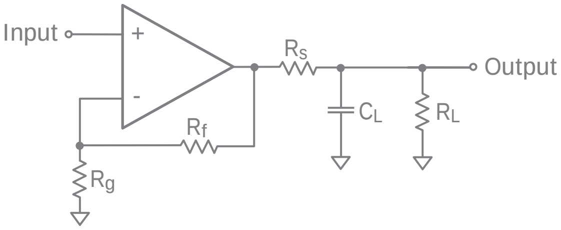


Figure 5. Addition of R_S for Driving Capacitive Loads

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1020 and will typically recover in less than 5us from an overdrive condition. Figure 6 shows the CLC1020 in an overdriven condition.

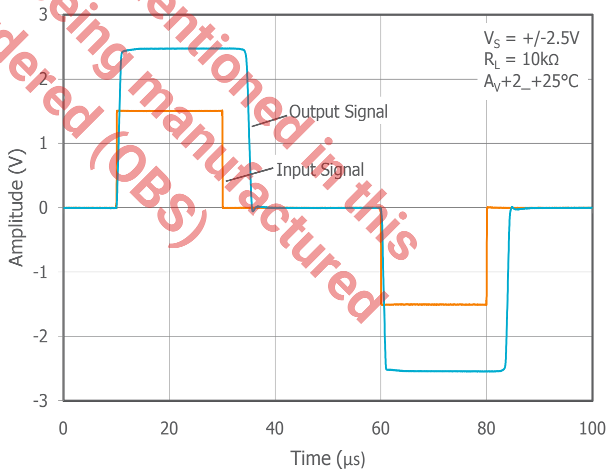


Figure 6. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling

- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB004	CLC1020 in TSOT

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-11. These evaluation boards are built for dual supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.

2. Use C3 (6.8μF) and C4 (0.1μF), if the -V_S pin of the amplifier is not directly connected to the ground plane.

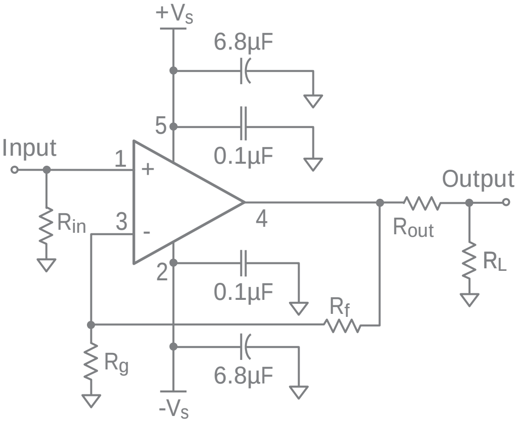

+VS
6.8μF
5
0.1μF
Input
1
+
Rin
3
-
4
Output
Rout
RL
2
0.1μF
Rf
Rg
6.8μF
-VS

Figure 7. CEB004 Schematic

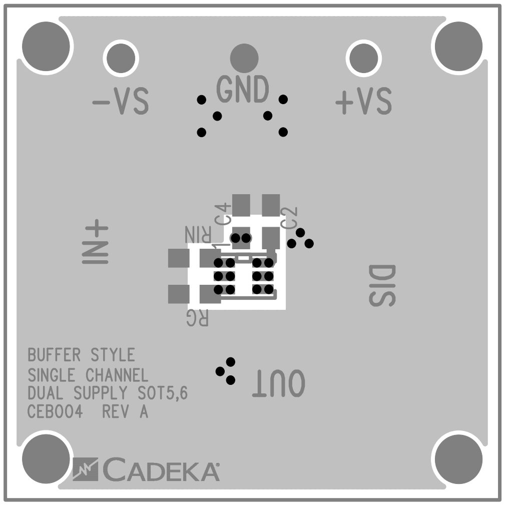

-VS
GND
+VS
IN+
RIN
C4
C2
DIS
RG
BUFFER STYLE
SINGLE CHANNEL
DUAL SUPPLY SOT5,6
CEB004 REV A
OUT
CADEKA

Figure 8. CEB004 Top View

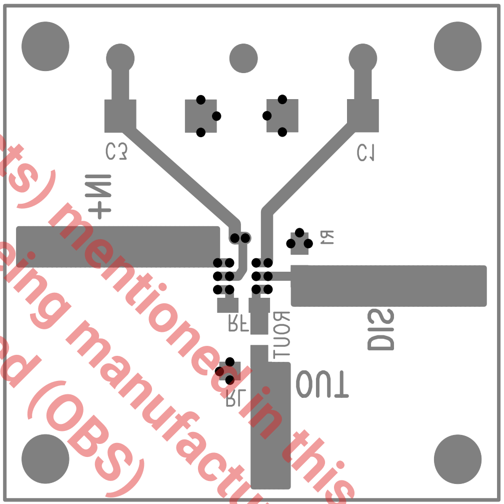
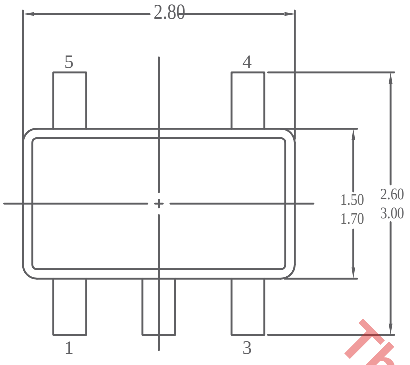
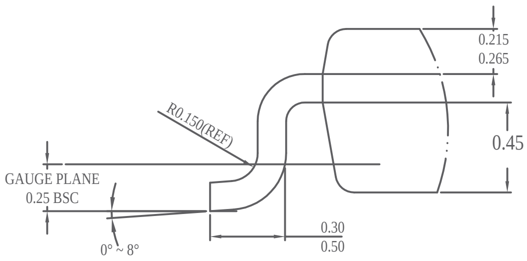

C3
C1
IN+
R1
RF
ROUT
DIS
RL
OUT

Figure 9. CEB004 Bottom View

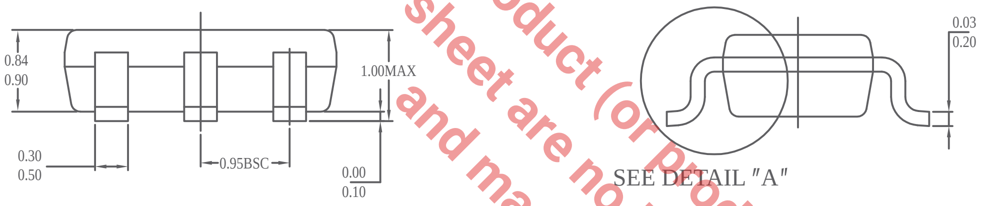
Mechanical Dimensions

TSOT-5 Package





DETAIL "A"



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE INTERLEAD FALSH OR PROTRUSION
3. PACKAGE WIDTH DOES NOTINCLUDE INTERLEAD FALSH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFROMS TO JEDEC MO-193, VARIATION AA.
6. DRAWING IS NOT TO SCALE.

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