KH560
Wideband, Low Distortion Driver Amplifier

Features
- 120MHz bandwidth at +24dBm output
- Low distortion
  (2nd/3rd: -60/-62dBc @ 20MHz and 10dBm)
- Output short circuit protection
- User-definable output impedance, gain, and compensation
- Internal current limiting
- Direct replacement for CLC560

Applications
- Output amplification
- Arbitrary waveform generation
- ATE systems
- Cable/line driving
- Function generators
- SAW drivers
- Flash A/D driving and testing

General Description
The KH560 is a wideband DC coupled, amplifier that combines high output drive and low distortion. At an output of +24dBm (10Vpp into 50Ω), the -3dB bandwidth is 120MHz. As illustrated in the table below, distortion performance remains excellent even when amplifying high-frequency signals to high output power levels.

With the output current internally limited to 250mA, the KH560 is fully protected against shorts to ground and can, with the addition of a series limiting resistor at the output, withstand shorts to the ±15V supplies.

The KH560 has been designed for maximum flexibility in a wide variety of demanding applications. The two resistors comprising the feedback network set both the gain and the output impedance, without requiring the series backmatch resistor needed by most op amps. This allows driving into a matched load without dropping half the voltage swing through a series matching resistor. External compensation allows user adjustment of the frequency response. The KH560 is specified for both maximally flat frequency response and 0% pulse overshoot compensations.

The combination of wide bandwidth, high output power, and low distortion, coupled with gain, output impedance and frequency response flexibility, makes the KH560 ideal for waveform generator applications. Excellent stability driving capacitive loads yields superior performance driving ADC’s, long transmission lines, and SAW devices. A companion part, the KH561, offers higher full power bandwidth for broadband sinusoidal applications.

The KH560 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

<table>
<thead>
<tr>
<th>Version</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>KH560AI</td>
<td>-25°C to +85°C</td>
<td>24-pin Ceramic DIP</td>
</tr>
<tr>
<td>KH560AK</td>
<td>-55°C to +125°C</td>
<td>24-pin Ceramic DIP, features burn-in and hermetic testing</td>
</tr>
<tr>
<td>KH560AM</td>
<td>-55°C to +125°C</td>
<td>24-pin Ceramic DIP, environmentally screened and electronically tested to MIL-STD-883</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typical Distortion Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>10dBm</td>
</tr>
<tr>
<td>18dBm</td>
</tr>
<tr>
<td>24dBm</td>
</tr>
</tbody>
</table>
**KH560 Electrical Characteristics** \((A_v = +10V, V_{CC} = ±15V, R_L = 50\,Ω, R_f = 410\,Ω, R_g = 40\,Ω, R_o = 50\,Ω; \text{unless specified})\)

**NOTES TO THE ELECTRICAL SPECIFICATIONS**

The electrical characteristics shown here apply to the specific test conditions shown above (see also Figure 1 in description of the operation). The KH560 provides an equivalent, non-zero, output impedance determined by the external resistors. The signal gain to the load is therefore load dependent. **The signal gain shown above \((A_v = +10\) is the no load gain.** The actual gain to the matching 50Ω load used in these specifications is half of this (+5).

The KH560 requires an external compensation capacitor. Unless otherwise noted, this has been set to 10.5pF for the frequency domain specifications (yielding a maximally flat frequency response) and 12.5pF for the time domain specifications (yielding a 0% small signal pulse overshoot response).

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>CONDITIONS</th>
<th>TYP</th>
<th>MIN &amp; MAX RATINGS</th>
<th>UNITS</th>
<th>SYM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case Temperature</td>
<td>KH560AI</td>
<td>+25°C</td>
<td>-25°C</td>
<td>+25°C</td>
<td>+85°C</td>
</tr>
<tr>
<td>Case Temperature</td>
<td>KH560AK/AM</td>
<td>+25°C</td>
<td>-55°C</td>
<td>+25°C</td>
<td>+125°C</td>
</tr>
</tbody>
</table>

**FREQUENCY DOMAIN RESPONSE** \((\text{Max. Flat Compensation})\)

- **+3dB bandwidth**
  - maximally flat compensation: \(V_o < 2V_{pp} (+10\text{dBm})\) 215 >175 >185 >175 MHz SSBW
  - 0% overshoot compensation: \(V_o < 2V_{pp} (+10\text{dBm})\) 210 >170 >180 >170 MHz FSBW
  (see Frequency Response vs. Output Power plot)
  - gain flatness: \(V_o < 2V_{pp} (+10\text{dBm})\) 0 <0.50 <0.40 <0.50 dB GFPL
  - peaking: 0.1 -50MHz 0 <1.25 <0.75 <1.00 dB GFPH
  - rolloff: at 100MHz 0.1 <1.00 <0.75 <1.00 dB GFR
  - group delay: to 100MHz 3.1 -- -- -- ns GD
  - linear phase deviation: to 100MHz 0.6 <1.7 <1.2 <2.7 ° LPD
  - return loss: to 100MHz -15 <12 <12 <12 dB RL

**DISTORTION** \((\text{Max. Flat Compensation})\)

- 2nd harmonic distortion
  - 24dBm (10V_{pp}): 20MHz -46 <0.36 <0.36 <0.33 dBc HD2H
  - 18dBm (5V_{pp}): 20MHz -51 <0.44 <0.44 <0.42 dBc HD2L
  - 10dBm (2V_{pp}): 20MHz -50 <0.43 <0.43 <0.40 dBc HD2M
  - 10dBm (2V_{pp}): 100MHz -54 <0.32 <0.32 <0.32 dBc HD2LH

- 3rd harmonic distortion
  - 24dBm (10V_{pp}): 20MHz -38 <0.32 <0.32 <0.25 dBc HD3H
  - 18dBm (5V_{pp}): 20MHz -48 <0.42 <0.45 <0.42 dBc HD3L
  - 10dBm (2V_{pp}): 20MHz -54 <0.50 <0.50 <0.48 dBc HD3LM
  - 10dBm (2V_{pp}): 100MHz -44 <0.40 <0.40 <0.36 dBc HD3LH

- 2-tone 3rd order
  - intermod intercept^2
  - 20MHz 40 >38 >38 >38 dBm IM3L
  - 50MHz 35 >32 >32 >32 dBm IM3M
  - 1000HZ 25 >23 >23 >20 dBm IM3H

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
### KH560 Electrical Characteristics

**(A<sub>v</sub> = +10V, V<sub>CC</sub> = ±15V, R<sub>L</sub> = 50Ω, R<sub>f</sub> = 410Ω, R<sub>G</sub> = 40Ω, R<sub>o</sub> = 50Ω unless specified)**

#### PARAMETERS CONDITIONS | TYP | MIN & MAX RATINGS | UNITS | SYM
---|---|---|---|---
Case Temperature | KH560AI | +25°C | -25°C | +25°C | +85°C
Case Temperature | KH560AK/AM | +25°C | -55°C | +25°C | +125°C

#### TIME DOMAIN RESPONSE (0% Overshoot Compensation)
- **rise and fall time**
  - 2V step: 1.6 < 2.0 < 1.9 < 2.0 ns TRS
  - 10V step: 3.6 < 3.8 < 4.5 < 5.3 ns TRL
- **settling time to 0.1% (time <1µs)**
  - 5V step: 10 < 15 < 15 < 25 ns TS
- **long term thermal tail (time >1µs)**
  - 5V step: 0.4 < 0.5 < 0.5 < 0.5 % SE
- **slew rate**
  - 10V<sub>pp</sub>, 175MHz: 2600 > 2300 > 2000 > 1800 V/µs SR
- **overshoot**
  - maximally flat compensation: 5 < 13 < 10 < 13 % OSMF
  - 0% overshoot compensation: 0 < 5 < 3 < 5 % OSZO

#### EQUIVALENT INPUT NOISE
- **voltage** > 100KHz: 2.1 < 2.5 < 2.5 < 2.5 nV/√Hz VN
- **inverting current** > 100KHz: 34 < 40 < 40 < 45 pA/√Hz ICN
- **non-inverting current** > 100KHz: 2.8 < 4.5 < 4.5 < 5.0 pA/√Hz NCN
- **noise floor** > 100KHz: -159 < -157 < -157 < -157 dBm/(1Hz) SNF
- **integrated noise** 1kHz to 200MHz: 35 < 45 < 45 < 45 µV INV
- **noise figure** > 100KHz: 15 < 17 < 17 < 17 dB NF

#### STATIC, DC PERFORMANCE
- **input offset voltage**
  - *: 2.0 < 14.0 < 5.0 < 15.0 mV VIO
- **average temperature coefficient**
  - *: 35 < 100 < 20 < 100 µV/°C DVIO
- **non-inverting bias current**
  - *: 5.0 < 35 < 20 < 20 µA IBN
- **average temperature coefficient**
  - *: 20 < 175 < 100 nA/°C DIBN
- **inverting bias current**
  - *: 10.0 < 50 < 30 < 50 µA IBI
- **average temperature coefficient**
  - *: 100 < 200 < 200 nA/°C DIBI
- **power supply rejection ratio (DC)**
  - *: 60 > 58 > 58 > 57 dB PSRR
- **supply current** no load: 50 < 60 < 60 < 65 mA ICC

#### MISCELLANEOUS PERFORMANCE
- **open loop current gain (±1% tolerance)**
  - 10.0 < – < – < – mA/mA G
- **average temperature coefficient**
  - +0.02 < +0.03 < – < +0.02 %/°C DG
- **inverting input resistance**
  - (±5% tolerance)
  - 14.0 < – < – < – Ω RIN
- **average temperature coefficient**
  - +0.02 < – < – < +0.02 Ω/°C DRIN
- **non-inverting input resistance**
  - 700 < 200 < 400 < 400 KΩ RNI
- **non-inverting input capacitance**
  - to 100MHz: 2.3 < 3.0 < 3.0 < 3.0 pF CNI
- **output voltage range**
  - 150mA load current: ±10.5 > 10.0 > 10.0 > 10.0 V VO
- **output current limit**
  - 210 < 250 < 250 < 250 mA OCL

#### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min/Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; (reversed supplies will destroy part)</td>
<td>±20V</td>
</tr>
<tr>
<td>differential input voltage</td>
<td>±3V</td>
</tr>
<tr>
<td>common mode input voltage</td>
<td>±V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>junction temperature (see thermal model)</td>
<td>+175°C</td>
</tr>
<tr>
<td>storage temperature</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>lead temperature (soldering 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>output current (internally limited)</td>
<td>±250mA</td>
</tr>
</tbody>
</table>

#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min/Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>±10V to ±15V</td>
</tr>
<tr>
<td>I&lt;sub&gt;o&lt;/sub&gt;</td>
<td>≤ ±200mA</td>
</tr>
<tr>
<td>common mode input voltage</td>
<td>&lt; ±(V&lt;sub&gt;CC&lt;/sub&gt; - 6)V</td>
</tr>
<tr>
<td>junction temperature (no load)</td>
<td>25Ω to 200Ω</td>
</tr>
<tr>
<td>gain range (no-load voltage gain)</td>
<td>+5 to +80</td>
</tr>
<tr>
<td>case temperature: AI</td>
<td>-25°C to +85°C</td>
</tr>
<tr>
<td>case temperature: AK/AM</td>
<td>-55°C to +125°C</td>
</tr>
</tbody>
</table>

#### Notes

1. *: AI/AK/AM 100% tested at +25°C
2. †: AK/AM 100% tested at +25°C and sample tested at -55°C and +125°C
3. †: AI sample tested at +25°C
4. Test Tones are set ±100kHz of indicated frequency.
5. Noise tests are performed from 5MHz to 200MHz.
KH560 Typical Performance Characteristics \( (T_A = +25^\circ C, \text{ Circuit in Figure 1; unless specified}) \)

### Small Signal Gain and Phase

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Gain (dB)</th>
<th>Phase (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>150</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>200</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>250</td>
<td>0</td>
</tr>
</tbody>
</table>

### Frequency Response vs. Gain

- **Normalized Magnitude (1dB/div)**
- **Frequency (MHz)**: 5, 0, 50, 100, 150, 200, 250
- **Gain (dB)**: 5, 10, 15, 20, 25, 30

### Frequency Response vs. Output Power

- **Normalized Magnitude (1dB/div)**
- **Frequency (MHz)**: 5, 0, 50, 100, 150, 200, 250
- **Output Power (dBm)**: -4dBm, 0dBm, 4dBm, 8dBm, 12dBm, 16dBm

### Frequency Response vs. RL

- **Normalized Magnitude (1dB/div)**
- **Frequency (MHz)**: 5, 0, 50, 100, 150, 200, 250
- **RL (Ohm)**: 50, 75, 100

### Frequency Response Driving CL

- **Normalized Magnitude (1dB/div)**
- **Frequency (MHz)**: 5, 0, 50, 100, 150, 200, 250
- **CL (pF)**: 100, 50, 20

### Two Tone, 3rd-Order Intermodulation

- **Intercept (2.5dB/div)**
- **Frequency (MHz)**: 4, 8, 12, 16, 20, 24

### 2nd Harmonic Distortion vs. Frequency

- **Distortion (dBc)**
- **Output Power (dB)**: 4, 8, 12, 16, 20, 24

### 3rd Harmonic Distortion vs. Frequency

- **Distortion (dBc)**
- **Output Power (dB)**: 4, 8, 12, 16, 20, 24

### Frequency Response Driving CL

- **Normalized Magnitude (5dBc/div)**
- **Frequency (MHz)**: 5, 10, 20, 30, 40, 50, 100

### 2nd Harmonic Distortion Driving CL

- **Distortion (5dBc/div)**
- **Output Power (dB)**: 4, 8, 12, 16, 20, 24

### 3rd Harmonic Distortion Driving CL

- **Distortion (5dBc/div)**
- **Output Power (dB)**: 4, 8, 12, 16, 20, 24
KH560 Typical Performance Characteristics (TA = +25°C, Circuit in Figure 1; unless specified)
SUMMARY DESIGN EQUATIONS AND DEFINITIONS

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_f = (G + 1)R_o - A_vR_i$</td>
<td>Feedback resistor from output to inverting input</td>
</tr>
<tr>
<td>$R_g = \frac{R_f - R_o}{A_v - 1}$</td>
<td>Gain setting resistor from inverting input to ground</td>
</tr>
<tr>
<td>$C_x = \frac{1}{R_o} - 0.08 \times 300 (1 - \frac{2}{R_g})$</td>
<td>External compensation capacitor from output to pin 19 (in pF)</td>
</tr>
</tbody>
</table>

Where:
- $R_o$ – Desired equivalent output impedance
- $A_v$ – Non-inverting input to output voltage gain with no load
- $G$ – Internal current gain from inverting input to output = 10 ±1%
- $R_i$ – Internal inverting input impedance = 14Ω ±5%
- $R_s$ – Non-inverting input termination resistor
- $R_L$ – Load resistor
- $A_L$ – Voltage gain from non-inverting input to load resistor

KH560 Description of Operation

Looking at the circuit of Figure 1 (the topology and resistor values used in setting the data sheet specifications), the KH560 appears to bear a strong external resemblance to a classical op amp. As shown in the simplified block diagram of Figure 2, however, it differs in several key areas. Principally, the error signal is a current into the inverting input (current feedback) and the forward gain from this current to the output is relatively low, but very well controlled, current gain. The KH560 has been intentionally designed to have a low internal gain and a current mode output in order that an equivalent output impedance can be achieved without the series matching resistor more commonly required of low output impedance op amps. Many of the benefits of a high loop gain have, however, been retained through a very careful control of the KH560’s internal characteristics.

The feedback and gain setting resistors determine both the output impedance and the gain. $R_f$ predominately sets the output impedance ($R_o$), while $R_g$ predominately determines the no load gain ($A_v$), solving for the required $R_i$ and $R_g$, given a desired $R_o$ and $A_v$, yields the design equations shown below. Conversely, given an $R_f$ and $R_g$, the performance equations show that both $R_i$ and $R_g$ play a part in setting $R_o$ and $A_v$. Independent $R_o$ and $A_v$ adjustment would be possible if the inverting input impedance ($R_i$) were 0 but, with $R_i = 14Ω$ as shown in the specification listing, independent gain and output impedance setting is not directly possible.

Design Equations

$$R_f = (G + 1)R_o - A_vR_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Performance Equations

$$R_o = \frac{G + 1 + \frac{R_f}{R_i}}{G + 1 + \frac{R_f}{R_g}}$$

$$A_v = 1 + \frac{G - \frac{R_i}{R_f}}{G + 1 + \frac{R_i}{R_g}}$$

Where:
- $G$ – forward current gain (=10)
- $R_i$ – inverting node input resistance (=14Ω)
- $R_o$ – desired output impedance
- $A_v$ – desired non-inverting voltage gain with no load

Simplified Circuit Description

Looking at the KH560’s simplified schematic in Figure 2, the amplifier’s operation may be described. Going from the non-inverting input at pin 8 to the inverting input at pin 18, transistors Q1 – Q4 act as an open loop unity gain buffer forcing the inverting node voltage to follow the non-inverting voltage input.

Transistors Q3 and Q4 also act as a low impedance (14Ω) looking into pin 18) path for the feedback error current. This current, $i_{err}$, flows through those transistors into a very well defined current mirror having a gain of 10 from this error current to the output. The current mirror outputs act as the amplifier output.

The input stage bias currents are supply voltage independent. Since these set the bias level for the whole...
part, relatively constant performance over supply voltage is achieved. A current sense in the error current leg of the 10X current mirror feeds back to the bias current setup providing a current shutdown feature when the output current approaches 250mA.

**Figure 2: Simplified Circuit Diagram**

**Developing the Performance Equations**

The KH560 is intended to provide both a controllable voltage gain from input to output as well as a controllable output impedance. It is best to treat these two operations separately with no load in place. Then, with the no-load gain and output impedance determined, the gain to the load will simply be the no-load gain attenuated by the voltage divider formed by the load and the equivalent output impedance.

Figure 3 steps through the output impedance development using an equivalent model of Figure 2. Offering an equivalent, non-zero, output impedance into a matched load allows the KH560 to operate at lower internal voltage swings for a given desired swing at the load. This allows higher voltage swings to be delivered at the load for a given power supply voltage at lower distortion levels than an equivalent op amp needing to generate twice the voltage swing actually desired at the matched load. This improved distortion is specified and tested over a wide range as shown in the specification listing.

**Figure 3: Output Impedance Derivation**

Get both $V_o$ and $I_o$ into terms of just the error current, $i_{err}$, using:

$$V^- = i_{err} R_i$$ and $$I_f = i_{err} \frac{V^-}{R_g} = i_{err} \left(1 + \frac{R_i}{R_g}\right)$$

$$V_o = V^- + i_f R_f = i_{err} \left[R_i + R_f \left(1 + \frac{R_i}{R_g}\right)\right]$$

and

$$I_o = G_{ierr} + i_f = i_{err} \left[G + 1 + \frac{R_i}{R_g}\right]$$

then

$$R_o = \frac{V_o}{I_o} = \frac{R_f + R_i \left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

note that $R_o \left|_{R_i=0} = \frac{R_f}{G+1}\right.$

**Figure 4: No Load Gain Derivation**

Note that the $R_o$ expression simplifies considerably if $R_i = 0$. Also note that if the forward current gain were to go to infinity, the output impedance would go to 0. This would be the normal op amp topology with a very high internal gain. The KH560 achieves a non-zero $R_o$ by setting the internal forward gain to be a low, well controlled, value.

**Developing the No-Load Gain Expression**

Taking the output impedance expression as one constraint setting the external resistor values, we now need to develop the no-load voltage gain expression from the non-inverting input to the output as the other constraint. Figure 4 shows the derivation of the no load gain.
recognize that [taking $V_i$ positive]

\[ V_o = V^- + G_i \cdot R_f \]

solving for $V^-$ from two directions

\[ V^- = V_i - i_{err} \cdot R_i = (G+1) i_{err} \cdot R_g \]

solving for $i_{err}$ from this

\[ i_{err} = \frac{V_i}{(G+1) \cdot R_g + R_i} \]

then

\[ V^- = V_i - \frac{V_i \cdot R_i}{(G+1) \cdot R_g + R_i} \]

and, substituting for $V^-$ and $i_{err}$ in the original $V_o$ expression

\[ V_o = V_i \left[ 1 + \frac{G \cdot R_f - R_i}{(G+1) \cdot R_g + R_i} \right] \]

pulling an $\frac{R_f}{R_g}$ out of the fraction

\[ A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_g} \left[ \frac{G - R_i}{G+1} \right] \]

note that $A_v \bigg|_{R_i = 0} = 1 + \frac{R_f}{R_g} \left( \frac{G}{G+1} \right)$

**Figure 4: Voltage Gain Derivation**

Note again that if $R_i = 0$ this expression would simplify considerably. Also, if $G$ were very large the voltage gain expression would reduce to the familiar non-inverting op amp gain equation. These two performance equations, shown below, provide a means to derive the design equations for $R_f$ and $R_g$ given a desired no load gain and output impedance.

**Performance Equations**

\[
\begin{align*}
R_f + R_i & \left( 1 + \frac{R_f}{R_g} \right) \\
R_o & = \frac{G+1 - \frac{R_i}{R_g}}{R_g} \\
A_v & = 1 + \frac{R_f}{R_g} \left[ \frac{G - R_i}{G+1} \right] \\
\end{align*}
\]

**Design Equations**

\[
\begin{align*}
R_f & = (G+1) R_o - A_v \cdot R_i \\
R_g & = \frac{R_f - R_o}{A_v - 1} \\
\end{align*}
\]

**Equivalent Model**

Given that the physical feedback and gain setting resistors have been determined in accordance with the design equations shown above, an equivalent model may be created for the gain to the load where the amplifier block is taken as a standard op amp. Figure 5 shows this analysis model and the resulting gain equation to the load.

\[
V_o = V_i \left( 1 + \frac{R_f - R_o}{R_g} \right) \frac{R_L}{R_L + R_o}
\]

substituting in for $R_f$ and $R_g$ with their design equation yields

\[
\frac{V_o}{V_i} = A_v \frac{R_L}{R_L + R_o} = A_L \text{ (gain to load)}
\]

**Figure 5: Equivalent Model**

This model is used to generate the DC error and noise performance equations. As with any equivalent model, the primary intent is to match the external terminal characteristics recognizing that the model distorts the internal currents and voltages. In this case, the model would incorrectly predict the output pin voltage swing for a given swing at the load. But it does provide a simplified means of getting to the external terminal characteristics.

**External Compensation Capacitor ($C_x$)**

As shown in the test circuit of Figure 1, the KH560 requires an external compensation capacitor from the output to pin 19. The recommended values described here assume that a maximally flat frequency response into a matched load is desired. The required $C_x$ varies widely with the desired value of output impedance and to a lesser degree on the desired gain. Note from Figure 2, the simplified internal schematic, that the actual total compensation ($C_t$) is the series combination of $C_x$ and the internal 10pF from pin 19 to the compensation nodes. The total compensation ($C_t$) is developed in two steps as shown below.

\[
C_t = \frac{300}{R_o} \left( 1 - \frac{2.0}{R_g} \right) \text{ pF intermediate equation}
\]

\[
C_t = \frac{C_1}{1 + (0.02) C_1} \text{ pF total compensation}
\]
With this total value derived, the required external $C_x$ is developed by backing out the effect of the internal 10pF. This, and an expression for the external $C_x$ without the intermediate steps are shown below.

$$C_x = \frac{10C_1}{10 - C_1}$$

or

$$C_x = \frac{1}{300 \left( 1 - \frac{2}{R_o} \right)} - 0.08 \text{ pF}$$

The plot in Figure 6 shows the required $C_x$ vs. gain for several desired output impedances using the equations shown above. Note that for lower $R_o$'s, $C_x$ can get very large. But, since the total compensation is actually the series combination of $C_x$ and 10pF, going to very high $C_x$'s is increasingly ineffective as the total compensation is only slightly changed. This, in part, sets the lower limits on allowable $R_o$.

**Figure 6: External Compensation Capacitance ($C_x$)**

A 0% small signal overshoot response can be achieved by increasing $C_x$ slightly from the maximally flat value. Note that this applies only for small signals due to slew rate effects coming into play for large, fast edge rates.

Beyond the nominal compensation values developed thus far, this external $C_x$ provides a very flexible means for tailoring the frequency response under a wide variety of gain and loading conditions. It is oftentimes useful to use a small adjustable cap in development to determine a $C_x$ suitable to the application, then fixing that value for production. An excellent 5pF to 20pF trimmer cap for this is a Sprague-Goodman part #GKX20000.

When the KH560 is used to drive a capacitive load, such as an ADC or SAW device, the load will act to compensate the response along with $C_x$. Generally, considerably lower $C_x$ values are required than the earlier development would indicate. This is advantageous in that a low $R_o$ would be desired to drive a capacitive load which, without the compensating effect of load itself, would otherwise require very large $C_x$ values.

**Gain and Output Impedance Range**

Figure 7 shows a plot of the recommended gain and output impedances for the KH560. Operation outside of this region is certainly possible with some degradation in performance. Several factors contribute to set this range. At very low output impedances, the required value of feedback resistor becomes so low as to excessively load the output causing a rapid degradation in distortion. The maximum $R_o$ was set somewhat arbitrarily at 200Ω. This allows the KH560 to drive into a 2:1 step down transformer matching to a 50Ω load. (This offers some advantages from a distortion standpoint.)

**Figure 7: Recommended Gain and Output Impedance Range**

For a given $R_o$, the minimum gain shown in Figure 7 has been set to keep the equivalent input noise voltage less than 4nV/√Hz. Generally, the equivalent input noise voltage decreases with higher signal gains. The high gain limit has been set by targeting a minimum $R_g$ of 10Ω or a minimum $R_f$ of 100Ω.

**Amplifier Configurations**

The KH560 is intended for a fixed, non-inverting, gain configuration as shown in Figure 1. The KH561 offers an enhanced slew rate at the expense of higher long-term thermal tail in the pulse response than the KH560. Due to its low internal forward gain, the inverting node does not present a low impedance, or virtual ground, node. Hence, in an inverting configuration, the signals source impedance will see a finite load whose value depends on the output loading. Inverting mode operation can be best achieved using a wideband, unity gain buffer with low output impedance to isolate the source from this varying load. A DC level can, however, be summed into the inverting node to offset the output either for offset correction or signal conditioning.

**Accuracy Calculations**

Several factors contribute to limit the achievable KH560 accuracy. These include the DC errors, noise effects,
and the impact internal amplifier characteristics have on the signal gain. Both the output DC error and noise model may be developed using the equivalent model of Figure 5. Generally, non-inverting input errors show up at the output with the same gain as the input signal, while the inverting current errors have a gain of simply \((R_f - R_o)\) to the output voltage (neglecting the \(R_o \) to \(R_L\) attenuation).

**Output DC Offset:**

The DC error terms shown in the specification listing along with the model of Figure 5 may be used to estimate the output DC offset voltage and drift. Each term shown in the specification listing can be of either polarity. While the equations shown below are for output offset voltage, the same equation may be used for the drift with each term replaced by its temperature drift value shown in the specification listing.

\[
V_{os} = (I_{bn} \cdot R_s \pm V_{io}) \left(1 + \frac{R_f - R_o}{R_g}\right) \pm I_{bi} (R_f - R_o)
\]

where:

- \(I_{bn}\) = non-inverting bias current
- \(I_{bi}\) = inverting bias current
- \(V_{io}\) = input offset voltage

An example calculation for the circuit in Figure 1 using typical 25°C DC error terms and \(R_s = 25\Omega\), \(R_L = 50\Omega\) yields:

\[
V_o = |(5\mu A \cdot 25\Omega \pm 2.0mV) 10 \pm 10\mu A (360\Omega)|\cdot 1/2 = 12.4mV
\]

Recall that the source impedance, \(R_s\), includes both the terminating and signal source impedance and that the actual DC level to the load includes the voltage divider between \(R_o\) and \(R_L\). Also note that for the KH560, as well as for all current feedback amplifiers, the non-inverting and inverting bias currents do not track each other in either magnitude or polarity. Hence, there is no meaning in an offset current specification, and source impedance matching to cancel bias currents is ineffective.

**Noise Analysis:**

Although the DC error terms are in fact random, the calculation shown above assumes they are all additive in a worst case sense. The effect of all the various noise sources are combined as a root sum of squared terms to get an overall expression for the spot noise voltage. The circuit of Figure 8 shows the equivalent circuit with all the various noise voltages and currents included along with their gains to the output.

\[
e_n = \sqrt{\frac{\left(e_{ni}^2 + \left(i_{ni} R_s\right)^2 + 4 k T R_s + \frac{i_i^2 \left(R_f - R_o\right)^2}{A_v^2}\right)}{4 k T \left(R_f - R_o\right) A_v + 4 k T R_o}}
\]
For the circuit of Figure 1, the equivalent input noise voltage may be calculated using the data sheet spot noises and \( R_s = 25\Omega, R_L = \infty \). Recall that 4kT = 16E-21J. All terms cast as \((nV/\sqrt{Hz})^2\):

\[
e_n = \sqrt{(2.1)^2 + (0.07)^2 + (0.632)^2 + (1.22)^2 + (0.759)^2 + (0.089)^2}
\]

\[
e_n = 2.62nV/\sqrt{Hz}
\]

**Gain Accuracy (DC):**
A classical op amp's gain accuracy is principally set by the accuracy of the external resistors. The KH560 also depends on the internal characteristics of the forward current gain and inverting input impedance. The performance equations for \( A_v \) and \( R_o \) along with the Thevinin model of Figure 5 are the most direct way of assessing the absolute gain accuracy. Note that internal temperature drifts will decrease the absolute gain slightly as the part warms up. Also note that the parameter tolerances affect both the signal gain and output impedance. The gain tolerance to the load must include both of these effects as well as any variation in the load. The impact of each parameter shown in the performance equations on the gain to the load (\( A_L \)) is shown below.

- Increasing current gain \( G \) Increases \( A_L \)
- Increasing inverting input \( R_i \) Decreases \( A_L \)
- Increasing \( R_f \) Increases \( A_L \)
- Increasing \( R_g \) Decreases \( A_L \)

**Applications Suggestions**

**Driving a Capacitive Load:**
The KH560 is particularly suitable for driving a capacitive load. Unlike a classical op amp (with an inductive output impedance), the KH560's output impedance, while starting out real at the programmed value, goes somewhat capacitive at higher frequencies. This yields a very stable performance driving a capacitive load. The overall response is limited by the \((1/RC)\) bandwidth set by the KH560's output impedance and the load capacitance. It is therefore advantageous to set a low \( R_o \) with the constraint that extremely low \( R_i \) values will degrade the distortion performance. \( R_o = 25\Omega \) was selected for the data sheet plots. Note from distortion plots into a capacitive load that the KH560 achieves better than 60dBc THD (10-bits) driving 2Vpp into a 50pF load through 30MHz.

**Improving the Output Impedance Match vs. Frequency - Using \( R_x \):**

Using the loop gain to provide a non-zero output impedance provides a very good impedance match at low frequencies. As shown on the Output Return Loss plot, however, this match degrades at higher frequencies. Adding a small external resistor in series with the higher frequencies, \( R_x \), as part of the output impedance (and adjusting the programmed \( R_o \) accordingly) provides a much better match over frequency. Figure 9 shows this approach.

**Interpreting the Slew Rate:**
The slew rate shown in the data sheet applies to the voltage swing at the load for the circuit of Figure 1. Twice this value would be required of a low output impedance amplifier using an external matching resistor to achieve the same slew rate at the load.

**Layout Suggestions:**
The fastest fine scale pulse response settling requires careful attention to the power supply decoupling. Generally, the larger electrolytic capacitor ground connections should be as near the load ground (or cable shield connection) as is reasonable, while the higher frequency ceramic de-coupling caps should be as near the KH560's supply pins as possible to a low inductance ground plane.

**Evaluation Boards:**
An evaluation board (showing a good high frequency layout) for the KH560 is available. This board may be ordered as part #730019.

**Thermal Analysis and Protection:**
A thermal analysis of a chip and wire hybrid is directed at determining the maximum junction temperature of all the internal transistors. From the total internal power dissipation, a case temperature may be developed using the ambient temperature and the case to ambient thermal impedance. Then, each of the dominant power dissipating paths are considered to determine which has the maximum rise above case temperature.

The thermal model and analysis steps are shown below. As is typical, the model is cast as an electrical model where the temperatures are voltages, the power dissipators are current sources, and the thermal impedances are resistances. Refer to the summary design equations and Figure 1 for a description of terms.
Figure 10: Thermal Model

\[ I_o = \frac{V_o}{R_{eq}} \] total output current

with \( R_{eq} = R_L \left( \frac{R_L A_L}{A_L - 1} \right) \) total load

\[ I_t = \frac{1}{2} \left( I_o + \sqrt{I_o^2 + (0.06)^2} \right) \] total internal output stage current

\[ P_t = I_t \left( V_{CC} - 1.4 - 17.3\Omega \cdot I_t \right) \] output stage power

\[ P_q = 0.2 \cdot I_t \left( V_{CC} - V_o - 0.7 - 15.3\Omega \cdot I_t \right) \] power in hottest internal junction prior to output stage

\[ P_{circuit} = 1.3 \cdot V_{CC} \left( 2 \cdot I_t - I_o + 19.2mA \right) - P_t - P_q \] power in remainder of circuit [note \( V_{CC} = 1 - V_{CC} \)]

Note that the \( P_t \) and \( P_q \) equations are written for positive \( V_o \). Absolute values of \(-V_{CC}, V_o, \) and \( I_o \), should be used for a negative going \( V_o \), since we are only interested in delta \( V \)’s. For bipolar swings, the two powers for each output polarity are developed as shown above then ratioed by the duty cycle. Having the total internal power, as well as its component parts, the maximum junction temperature may be computed as follows:

\[ T_c = T_A + (P_q + P_T + P_{circuit}) \cdot \theta_{ca} \] Case Temperature

\[ \theta_{ca} = 35°C/W \] for the KH560 with no heatsink in still air

\[ T_{j(t)} = T_c + P_t \cdot 20°C/W \] output transistor junction temperature

\[ T_{j(q)} = T_c + P_q \cdot 200°C/W \] hottest internal junction temperature

**The Limiting Factor for Output Power is Maximum Junction Temperature**

Reducing \( \theta_{ca} \) through either heatsinking and/or airflow can greatly reduce the junction temperatures. One effective means of heatsinking the KH560 is to use a thermally conductive pad under the part from the package bottom to a top surface ground plane on the component side. Tests have shown a \( \theta_{ca} \) of 24°C in still air using a “Sil Pad” available from Bergquist (800-347-4572).

As an example of calculating the maximum internal junction temperatures, consider the circuit of Figure 1 driving ±2.5V, 50% duty cycle, square wave into a 50Ω load.

\[ R_{eq} = 50Ω \left( \frac{410Ω \cdot 5}{5 - 1} \right) = 45.6Ω \]

\[ I_o = 2.5V / (45.6Ω) = 54.9mA \]

\[ I_T = \frac{1}{2} \left( 54.9mA + \sqrt{(54.9mA)^2 + (0.06)^2} \right) = 68.1mA \]

\[ P_T = 68.1mA \left( 15 - 2.5 - 0.7 - 15.3Ω \cdot 68.1mA \right) = 733mW \] total power in both sides of the output stage

\[ P_q = 0.2 \cdot 68.1mA \left( 15 - 1.4 - 17.3Ω \cdot 68.1mA \right) = 169mW \] total power in both sides of hottest junctions prior to output stage

\[ P_{circuit} = 1.3 \cdot 15 \left( 2 \cdot 68.1mA - 54.9mA + 19.2mA \right) - 733mW - 169mW = 1.058W \] power in the remainder of circuit

With these powers and \( T_A = 25°C \) and \( \theta_{ca} = 35°C/W \)

\[ T_c = 25°C + (.733 + .169 + 1.058) \cdot 35 = 94°C \] case temperature

From this, the hottest internal junctions may be found as

\[ T_{j(t)} = 94°C + \frac{1}{2} \cdot (733) \cdot 20 = 101°C \] output stage

\[ T_{j(q)} = 94°C + \frac{1}{2} \cdot (.169 \cdot 200) = 111°C \] hottest internal junction

Note that 1/2 of the total \( P_T \) and \( P_q \) powers were used here since the 50% duty cycle output splits the power evenly between the two halves of the circuit whereas the total powers were used to get case temperature.

Even with the output current internally limited to 250mA, the KH560’s short circuiting capability is principally a thermal issue. Generally, the KH560 can survive short duration shorts to ground without any special effort. For protection against shorts to the ±15 volt supply voltages, it is very useful to reduce some of the voltage across the output stage transistors by using some external output resistance, \( R_x \), as shown in Figure 9.

**Evaluation Board**

An evaluation board (part number 730019) for the KH560 is available.
## KH560 Package Dimensions

![Diagram of KH560 Package Dimensions]

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<th>Symbol</th>
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**NOTES:**
- Seal: seam weld (AM, AK), epoxy (AI)
- Lead finish: gold finish
- Package composition:
  - Package: ceramic
  - Lid: kovar/nickel (AM, AK), ceramic (AI)
  - Leadframe: alloy 42
  - Die attach: epoxy

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**For Further Assistance:**
Exar Corporation Headquarters and Sales Offices
48720 Kato Road
Fremont, CA 94538 - USA
Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7001
www.exar.com

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