

General Description

The MxL83411 is a family of monolithic quadruple differential line RS-485/RS-422 receivers that supports communication up to 10Mbps in harsh industrial environments. The bus pins tolerate IEC electrical fast transients (EFT), IEC electrostatic discharge (ESD), offer a wide input voltage range, and input hysteresis.

Guaranteed low propagation delays and channel-to-channel and part-to-part propagation delay skews ensure maximum system performance. Several package and operating temperature options coupled with wide power supply range support (from 3.3 to 5V) provide a versatile portfolio that can be used in applications ranging from high-speed motor drives to wireless infrastructure and building automation. The integration of four receiver channels into compact TSSOP or NSOIC packages makes these products well suited to space-constrained applications that require robust, high-performance communication. The MxL83411 device offers global enable pins, which allow all four channels to be enabled or disabled simultaneously. Industry standard footprint and pinout ensure seamless compatibility.

Features

- Meets or exceeds the requirements of the *TIA/EIA-485A* and *EIA/TIA-422B* standards
- Supply voltage from 3.3V to 5V
- Extended operating temperature range from -40°C to 125°C
- Operational common-mode range from -7V to 12V
- Fail-safe open receiver (Rx) inputs
- 1/4 unit load (128 bus nodes)
- Available in global enable configuration
- High-data rates up to 10Mbps
- Glitch-free power-up/power-down for hot plug-in capability
- Channel-to-channel propagation delay skew of $\pm 6\text{ns}$
- Robust system protection:
 - $\pm 2\text{kV}$ EFT (*IEC 61000-4-4*)
 - $\pm 8\text{kV}$ ESD Contact (*IEC 61000-4-2*)
 - $\pm 15\text{kV}$ ESD Human Body Model

Applications

- Industrial and process control equipment
- Level translators
- Telecommunication equipment
- High-performance motor drives
- Smart Grid
- Industrial transport

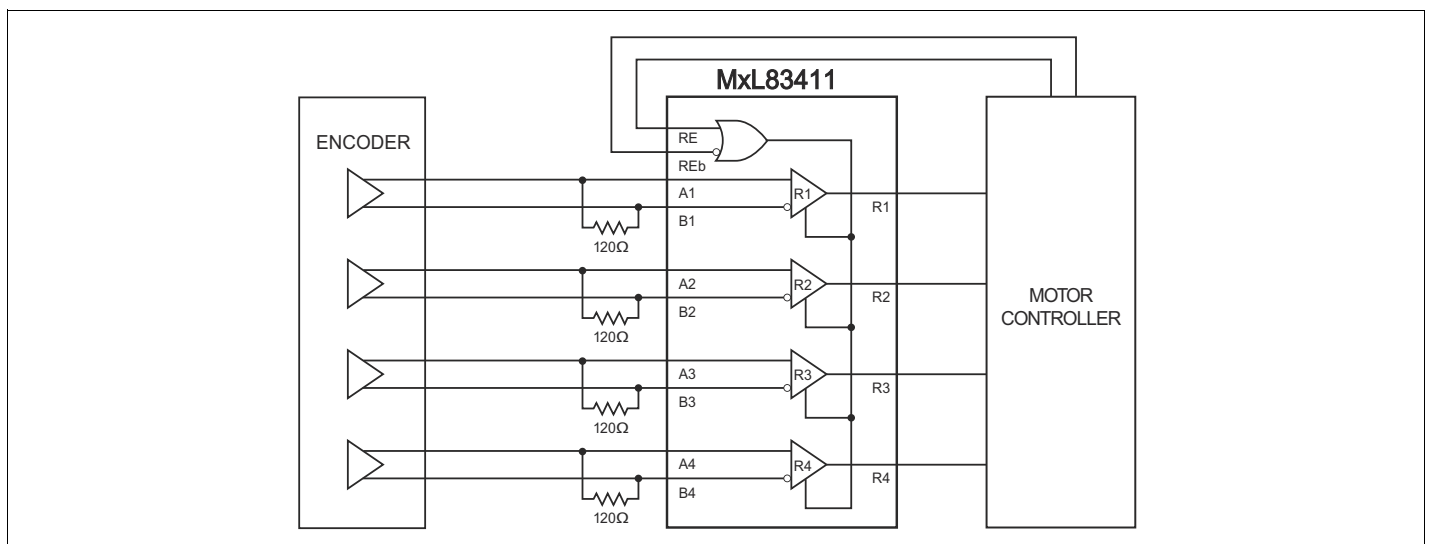


Figure 1: Typical Application Schematic

Revision History

Document No.	Release Date	Change Description
281DSR01	May 3, 2024	Updated: <ul style="list-style-type: none">■ "Thermal Information" table.■ "Recommended Operating Conditions" table.■ "Receiver Switching Characteristics (10Mbps)" table.■ "Mechanical Dimensions—NSOIC16" figure.■ "Mechanical Dimensions—TSSOP16" figure.■ "Ordering Information" section.
281DSR00	November 6, 2023	Initial release.

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Specifications

Absolute Maximum Ratings

Important: Stresses beyond what is listed in [Table 1](#) may cause permanent damage to the device. Exposure to any absolute maximum rating condition may affect device reliability and lifetime.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply Voltage (V_{CC})	-0.3	6	V
Control Input Voltage (RE)	-0.3	6	V
Control Input Voltage (REb)	-0.3	$V_{CC} + 0.3$	V
Receiver Input Voltage (AX, BX)	-25	25	V
Receiver Output Voltage (RX)	-0.3	$V_{CC} + 0.3$	V
Receiver Output Short-Circuit Current	-40	40	mA
Maximum Storage Temperature	-95	150	°C

ESD and EFT Ratings

Table 2: ESD and EFT Ratings

Parameter	Limit	Units
HBM - Human Body Model (pins AX and BX)	±15	kV
IEC 61000-4-2 Contact Discharge (pins AX and BX)	±8	kV
IEC 61000-4-4 Electrical Fast Transient (pins AX and BX)	±2	kV

Thermal Information

Table 3: Thermal Information

Thermal Metric		MxL83411		
		NSOIC16	TSSOP16	Units
T_A	Ambient temperature	25	25	°C
P	Die power	0.09	0.09	W
T_J	Junction temperature	30.41	32.68	°C
T_C	Case temperature	30.09	32.54	°C
T_B	Bottom temperature	26.71	27.39	°C
θ_{JA}	Junction-to-ambient thermal resistance	60.10	85.38	°C/W
Ψ_{JT}	Thermal metric	3.56	1.60	°C/W
Ψ_{JB}	Junction-to-case, at tab	41.13	58.77	°C/W
θ_{JB}	Junction-to-board	42.46	59.94	°C/W
θ_{JC}	Junction-to-case thermal resistance	29.32	32.01	°C/W

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	3.0	5.5	V
High Level Input Voltage (RE and REb pin)	V_{IH}	2.0	-	V
Low Level Input Voltage (RE and REb pin)	V_{IL}	-	0.8	V
Operational Common-Mode Input Voltage	V_{CM}	-7	12	V
Operating Ambient Temperature	T_A	-40	125	°C
Junction Temperature	T_J	-40	150	°C

Electrical Characteristics

Unless otherwise noted, $V_{CC} = 3V$ to $5.5V$, ambient temperature $T_{MIN} < T_A < T_{MAX}$. Typical values are at $V_{CC} = 3.3V$, ambient temperature $T_A = 25^{\circ}C$.

Table 5: Receiver DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Receiver Input Current (AX, BX)	I_I	$V_{CC} = 0$ or $5.5V$, $V_I = 12V$	-	-	250	μA
		$V_{CC} = 0$ or $5.5V$, $V_I = -7V$	-200	-	-	μA
Receiver Input Resistance	R_{IN}	$-7V \leq V_{A/B} \leq 12V$, $\Delta V/\Delta I$, power on or off	48	-	-	$k\Omega$
Receiver Positive-going Input Threshold	V_{TH+}	For $3V \leq V_{CC} \leq 5.5V$: Over common-mode range of $-7V$ to $12V$	-	-	0.2	V
Receiver Negative-going Input Threshold	V_{TH-}	For $3V \leq V_{CC} \leq 5.5V$: Over common-mode range of $-7V$ to $12V$	-0.2	-	-	V
Input Hysteresis	V_{HYS}	-	-	70	-	mV
Logic Inputs and Receiver Outputs						
Input Logic Threshold Low	V_{IL}	RE, REb	-	-	0.8	V
Input Logic Threshold High	V_{IH}	RE, REb	2.0	-	V_{CC}	V
Input Logic Hysteresis	V_{IHYS}	RE, REb	-	100	-	mV
Logic Input Current	I_{IL}	RE (pull-down)	-1	-	100	μA
		REb (pull-up)	-100	-	1	μA
Output High Voltage	V_{OH}	$I_{OH} = -4mA$, $V_{ID} = 200mV$, $3V \leq V_{CC} \leq 5.5V$	$V_{CC} - 0.6$	-	-	V
		$I_{OH} = -8mA$, $V_{ID} = 200mV$, $4.5V \leq V_{CC} \leq 5.5V$	$V_{CC} - 0.6$	-	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 4mA$, $V_{ID} = -200mV$, $3V \leq V_{CC} \leq 5.5V$	-	0.2	0.4	V
		$I_{OL} = 8mA$, $V_{ID} = -200mV$, $4.5V \leq V_{CC} \leq 5.5V$	-	0.2	0.4	V
Output High-Impedance Current	I_{OZR}	$0 \leq V_{RO} \leq 5.5V$, RE = 0V, REb = V_{CC}	-1	-	1	μA
Device						
Supply Current	I_{CC}	RE = V_{CC} or REb = GND	-	2.1	4	mA

Receiver Switching Characteristics—MxL83411 (10Mbps)

Unless otherwise noted, $V_{CC} = 3V$ to $5.5V$, ambient temperature $T_{MIN} < T_A < T_{MAX}$. Typical values are at $V_{CC} = 3.3V$, ambient temperature $T_A = 25^\circ C$.

Table 6: Receiver Switching Characteristics (10Mbps)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Maximum Data Rate	-	$ V_{ID} = 3V$, $C_L = 15pF$	10	-	-	Mbps
Receiver Propagation Delay	t_{RPLH} , t_{RPHL}	$ V_{ID} = 3V$, $C_L = 15pF$ (Figure 3 on page 5).	2	10	20	ns
Receiver Skew	$ t_{RPHL} - t_{RPLH} $	$ V_{ID} = 3V$, $C_L = 15pF$ (Figure 3 on page 5).	-	-	6	ns
Receiver Output Rise/Fall Time	t_r	$ V_{ID} = 3V$, $C_L = 15pF$	-	3	7	ns
	t_f	$ V_{ID} = 3V$, $C_L = 15pF$	-	3	7	ns
Channel-to-Channel Delay Skew	$t_{SK(C-C)}$	$ V_{ID} = 3V$, $C_L = 15pF$, same supply voltage and operating temperature.	-	-	6	ns
Part-to-Part Propagation Delay Skew	$t_{SK(P-P)}$	$ V_{ID} = 3V$, $C_L = 15pF$, same supply voltage and operating temperature.	-	-	12	ns
Receiver Disable Time from Output High	t_{RHZ}	$C_L = 15pF$, $R_L = 1k\Omega$ (Figure 4 on page 6).	-	10	25	ns
Receiver Disable Time from Output Low	t_{RLZ}	$C_L = 15pF$, $R_L = 1k\Omega$ (Figure 4 on page 6).	-	10	25	ns
Receiver Enable Time to Output High	t_{RZH}	$C_L = 15pF$, $R_L = 1k\Omega$ (Figure 4 on page 6).	-	15	30	ns
Receiver Enable Time to Output Low	t_{RZL}	$C_L = 15pF$, $R_L = 1k\Omega$ (Figure 4 on page 6).	-	15	30	ns

Test Circuits and Timing Diagrams

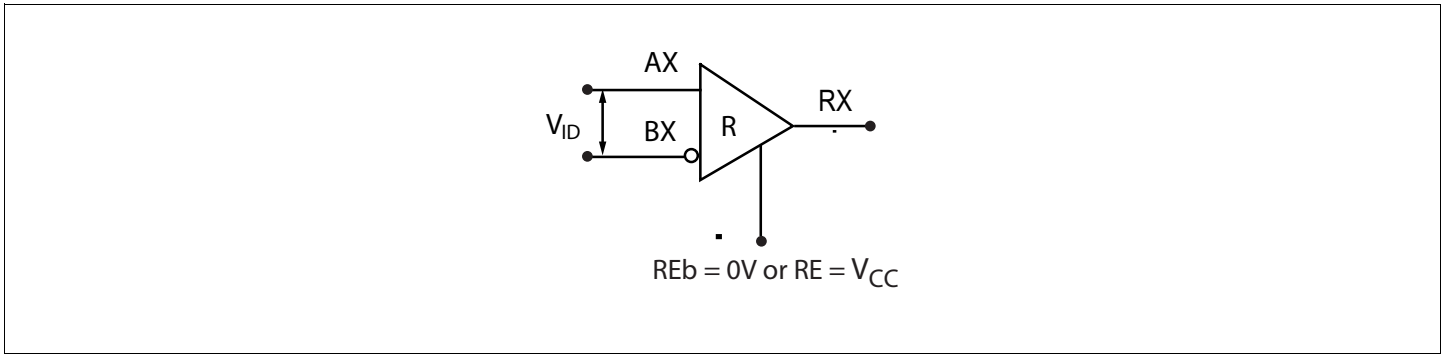


Figure 2: Receiver DC Test Circuit

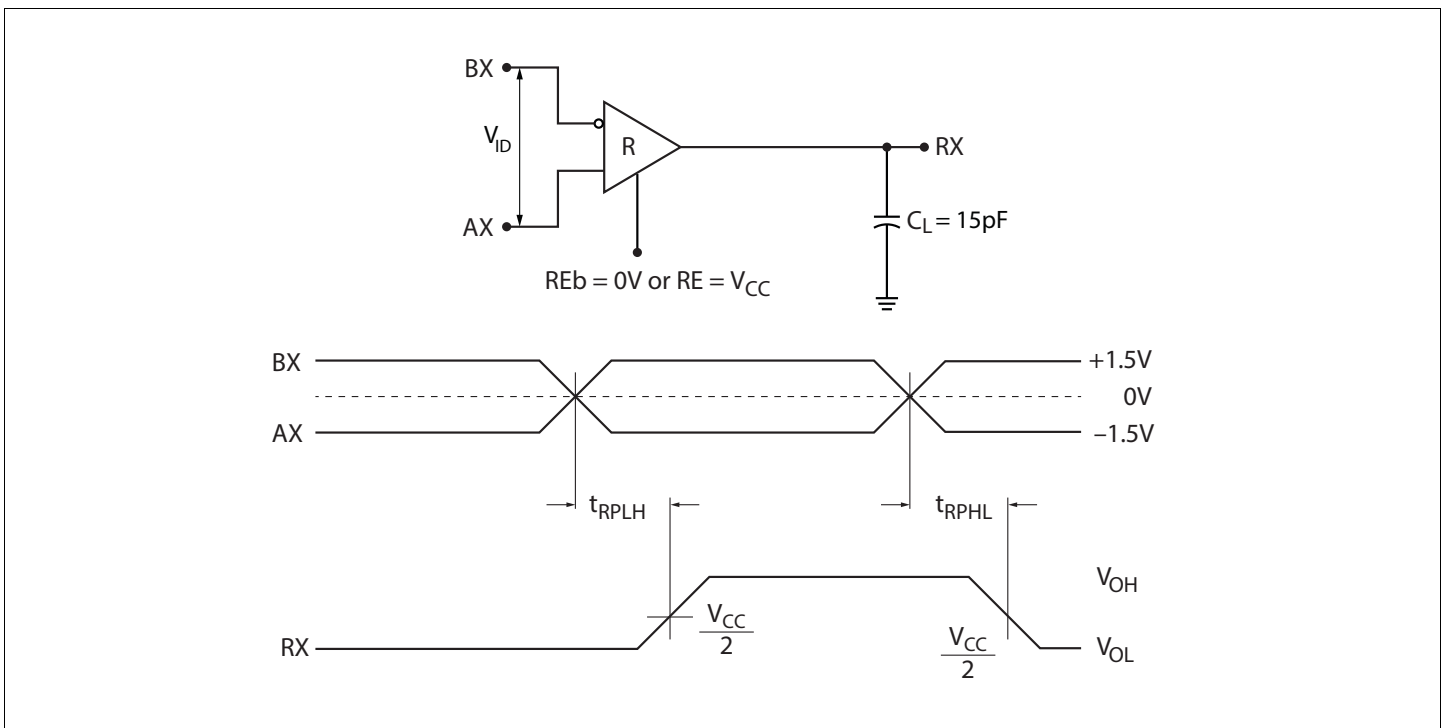


Figure 3: Receiver Propagation Delay Test Circuit and Timing Diagram

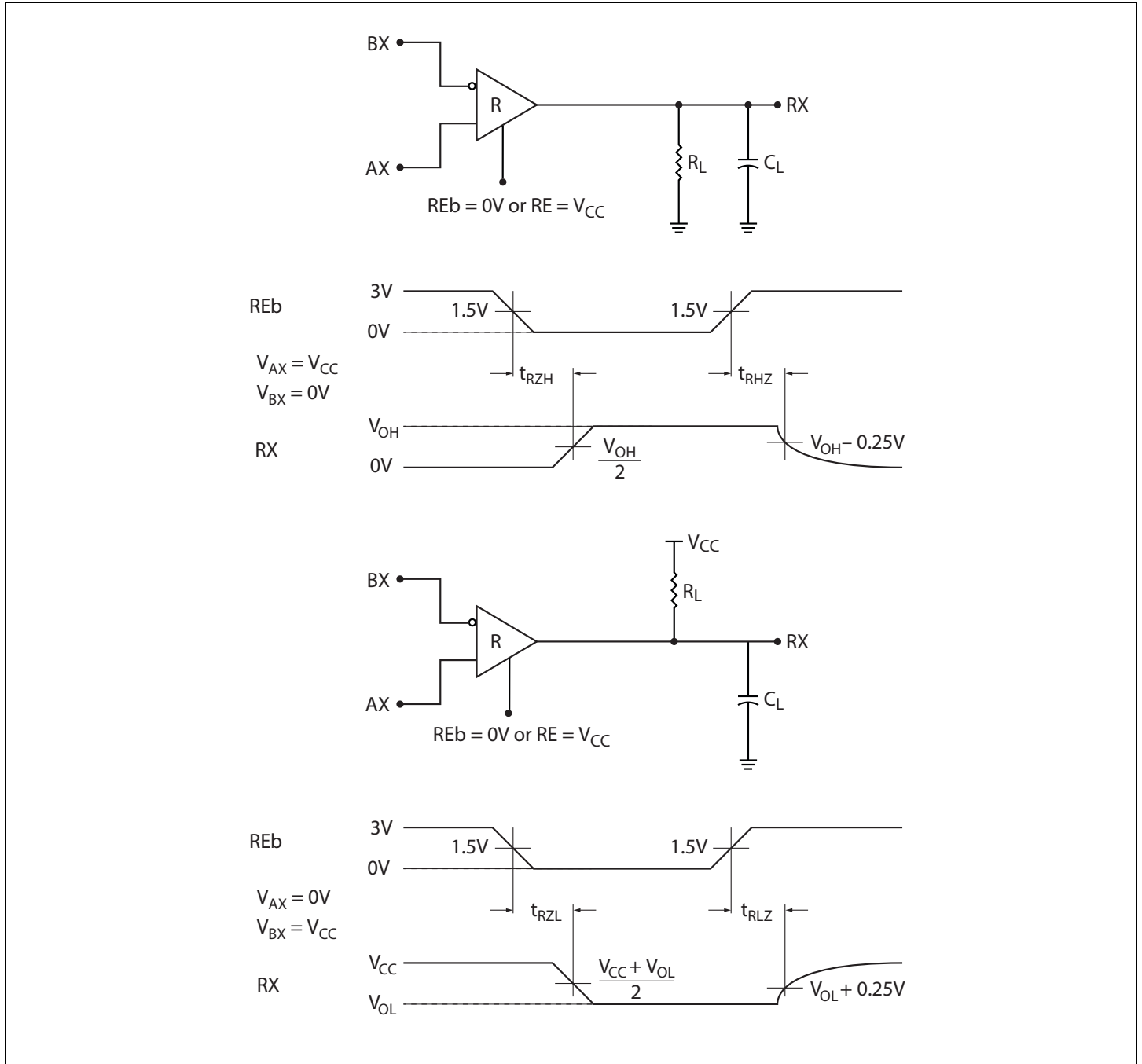


Figure 4: Receiver Enable and Disable Times Test Circuit and Timing Diagram

Typical Performance Characteristics

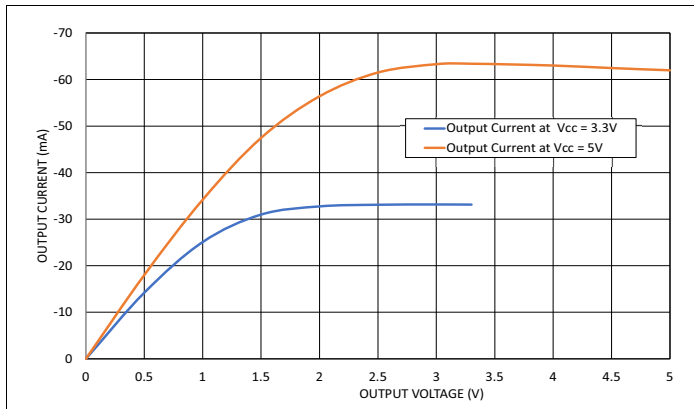


Figure 5: Output Current vs Output Low Voltage

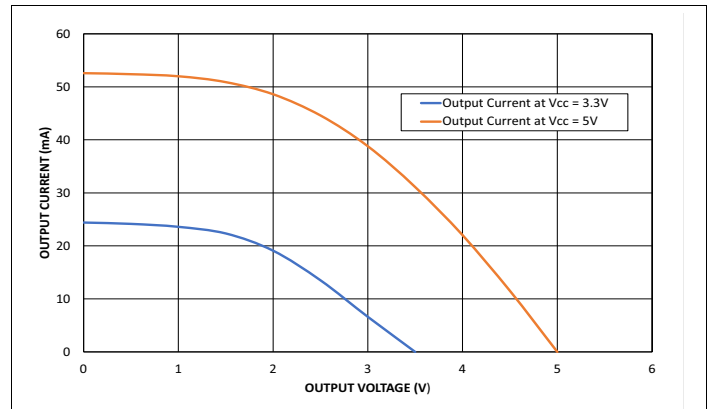


Figure 6: Output Current vs Output High Voltage

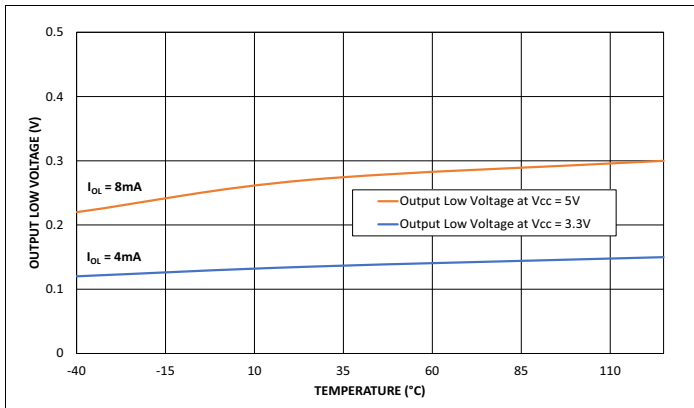


Figure 7: Output Low Voltage vs Temperature

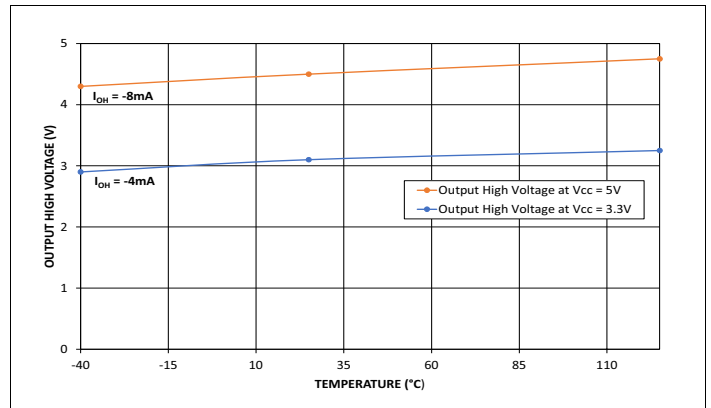


Figure 8: Output High Voltage vs Temperature

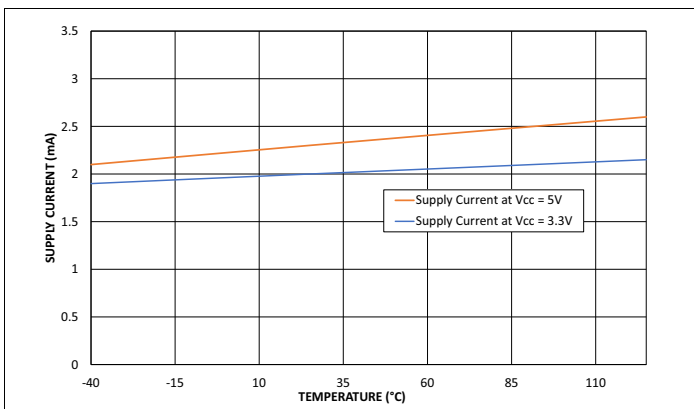


Figure 9: Supply Current vs. Temperature

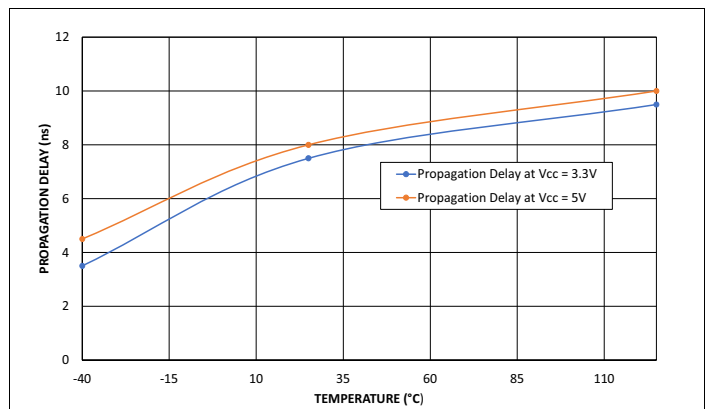


Figure 10: Propagation Delay vs. Temperature

Function Tables

Table 7: Receiver Enable Logic Configuration

Receiver Enable					
Inputs		Outputs			
RE	REb	R1	R2	R3	R4
0	0	Enable	Enable	Enable	Enable
0	1	High-Z	High-Z	High-Z	High-Z
1	0	Enable	Enable	Enable	Enable
1	1	Enable	Enable	Enable	Enable

Table 8: General Configuration

Differential A-B	RE/REb	RX Output
$V_{ID} \geq V_{TH+}$	Enabled	H
$V_{TH-} \leq V_{ID} \leq V_{TH+}$	Enabled	Undefined
$V_{ID} \leq V_{TH-}$	Enabled	L
Open	Enabled	H
X	Disabled	High-Z

Pin Information

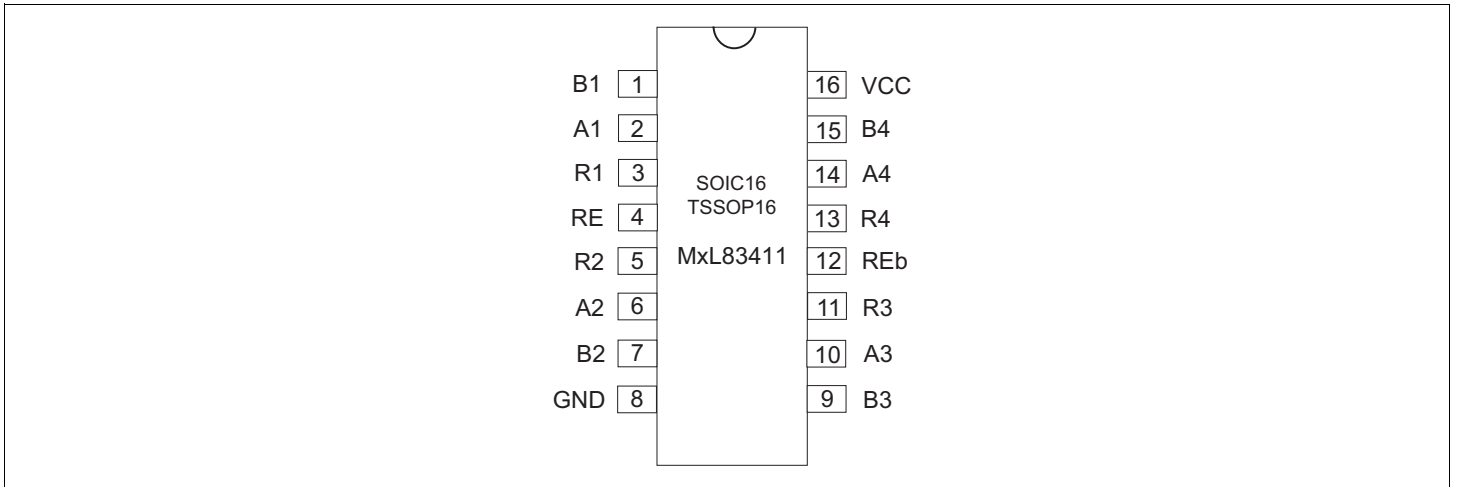


Figure 11: Pin Configuration

Pin Descriptions

Table 9: Pin Assignments

Pin Number	Pin Name	Function
1, 7, 9, 15	B1, B2, B3, B4	Channel X inverting receiver input.
2, 6, 10, 14	A1, A2, A3, A4	Channel X non-inverting receiver input.
3, 5, 11, 13	R1, R2, R3, R4	Receiver output. Enabled when RE = high or REb = low. See Table 8 on page 8.
4	RE	Active-high receiver output enable. A logic-high on this input enables all receivers. When RE = low and REb = high, all receivers are disabled, and the outputs go high impedance. RE has a pull-down resistor to the ground.
8	GND	Ground.
12	REb	Active-low receiver output enable. A logic-low on this input enables all receivers. When REb = high and RE = low, all receivers are disabled, and the outputs go high impedance. REb has a pull-up resistor to V _{CC} .
16	VCC	System power supply input (from 3.0V to 5.5V).

Application Information

The MxL83411 is a family of monolithic quadruple differential line RS-485/RS-422 receivers that meet the necessary requirements for *TIA/EIA-485-A* and *TIA/EIA-422-B* serial interface standards. This device is suitable for different applications ranging from high-speed motor drives to wireless infrastructure and building automation. The MxL83411 is an excellent choice for all space-constrained applications that require robust, high-performance communication, high immunity to electrical fast transient (EFT) protection (*IEC 61000-4-4*), and electrostatic discharge (ESD) protection (*IEC61000-4-2*).

The MxL83411 device has a common-mode range of -7V to 12V to accommodate ground potential differences between receiver nodes. This device can operate with a wide supply voltage range from 3V to 5.5V power supply, with a speed of 10Mbps in both standard and extended industrial temperature ranges.

ESD Protection (IEC 61000-4-2)

The *IEC 61000-4-2* standard covers ESD testing and performance of finished equipment. However, it does not refer to integrated circuits. The MxL83411 helps you design equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. MaxLinear develops state-of-the-art structures employed on the bus pins to protect the device and the rest of the system against ESD damage during operation.

The receiver inputs of the MxL83411 device are characterized for protection to the following limits:

- $\pm 15\text{kV}$ using the Human Body Model.
- $\pm 8\text{kV}$ using the ESD contact discharge method specified in *IEC 61000-4-2*.

Electrical Fast Transient Protection (IEC 61000-4-4)

Inductive loads such as relays, switch contractors, or industrial motors can create high-frequency bursts during their operations. Electrical fast transient (EFT) tests evaluate immunity of electrical and electronic equipment when subjected to repetitive electrical fast transient or bursts. The MxL83411 device is qualified to the following limit:

- $\pm 2\text{kV}$ using the EFT method specified in *IEC 61000-4-4*.

128 Receivers on the Bus

The standard RS-485 receiver input impedance is $12\text{k}\Omega$ (1 unit load), and the standard driver can drive up to 32 unit loads (UL). The MxL83411 family of receivers has a $\frac{1}{4}$ -unit load receiver input impedance of $48\text{k}\Omega$, allowing up to 128 receivers to be connected in parallel on the bus line.

Standard Fail-Safe Receivers

The receiver inputs of the MxL83411 device guarantee to produce a logic-high output when the inputs are open-circuited (no termination resistor between inputs A and B). However, when the bus is terminated and the transmitters are disabled, the differential voltage between inputs A and B falls into the *undetermined* zone ($-200\text{mV} \leq V_{AB} \leq 200\text{mV}$). Consequently, the output becomes undefined. To properly maintain a fail-safe receiver output with a terminated bus line, input A must be biased at least 200mV above input B for the receiver output to produce a logic high for the standard fail-safe receiver.

For more information about the differences between standard and advanced RS-485/RS-422 fail-safe receivers, refer to the *RS-485 Advanced Fail-Safe Feature Application Note (291AN)*.

Global Enable Configurations

The MxL83411 device offers a global enable configuration. All four receiver outputs are enabled simultaneously when $RE = V_{CC}$ or $REb = GND$.

When $REb = V_{CC}$ and $RE = GND$, all four receiver outputs are in high impedance state.

For more information about configuration, see [Table 7](#) on page 8.

Enhanced Receiver Noise Immunity

The MxL83411 differential receivers feature a fully symmetrical threshold to maintain duty cycle of the signal even with small amplitude input signals. With a large receiver hysteresis, the MxL83411 can provide additional noise immunity from standard RS-485/RS-422 receivers, preventing high frequency noise pulses from the RS-485/RS-422 bus from appearing on the receiver outputs.

Low Propagation Delay and Skew

The MxL83411 device provides low propagation delays, low channel-to-channel skews, and low device-to-device skews, even between devices from different manufacturing lots. This feature allows multiple channels and devices to receive communication data with minimal skew with respect to each other.

Channel-to-channel skew ($t_{SK(C-C)}$) is defined as the difference between the maximum channel delay and minimum channel delay measured across all four channels within a single device keeping the same power supply, same input signal (V_{ID} and V_{CM}) and same operating temperature.

Part-to-part skew ($t_{SK(P-P)}$) is defined as the difference between the maximum channel delay and minimum channel delay measured across the devices from different manufacturing lots keeping the same power supply, same input signal (V_{ID} and V_{CM}) and same operating temperature.

Multi-Protocol Receive Mode Support

When communication is required between systems that support different interfaces, you can use the MxL83411 receiver as a translation device to bridge between multiple interfaces. The following cases are possible usage between host transmitter and MxL83411 receiver.

Case 1: Single-ended driver (TTL, CMOS, LVTTTL, or LVCMOS) to TTL level logic output

The MxL83411 receiver can receive single-ended data from standard high-speed TTL, CMOS, LVTTTL, or LVCMOS output driver. It is accomplished by tying one of the inputs to a fixed bias voltage at $V_{CC}/2$ and connecting the other input to the single-ended driver output. In this application, the MxL83411 receiver acts as a level shifter to convert variable-level signal input into TTL-level logic output. The receiver trip point can be adjusted to accommodate different driver output swings by changing the resistor divider at the bias input. [Figure 12](#) shows the single-ended receiver configuration with driver from TTL, CMOS, LVTTTL, or LVCMOS as output and receiver connected via a short PCB trace to non-inverting input A (+). The 4.7K resistors act as a voltage divider to set the inverting input B (-) at $V_{CC}/2$.

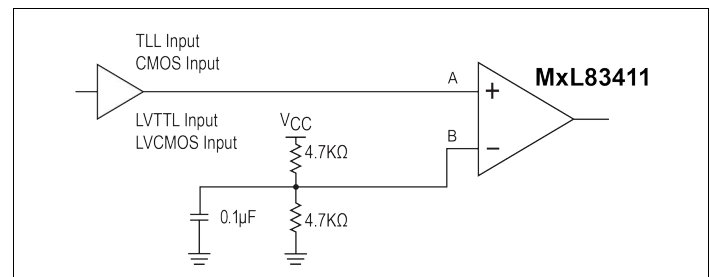


Figure 12: Multi-Protocol Receive Mode Support Case 1

Table 10: Multi-Protocol Receive Mode with various TTL, CMOS, LVTTTL, or LVCMOS Level Input

Driver $V_{CC}(V)$	Input B (-) Bias at $V_{CC}/2$	Input A(+) Connect to Driver Output	5V Output R (TTL)	3.3V Output R (LVTTTL)
5.0V	2.5V	TTL/CMOS (74ALS125, 74AC125...)	TTL output	LVTTTL output
3.6V	1.8V	LVTTTL (74LV125...)	TTL output	LVTTTL output
3.3V	1.65V	LVCMOS (74LVC125...)	TTL output	LVTTTL output

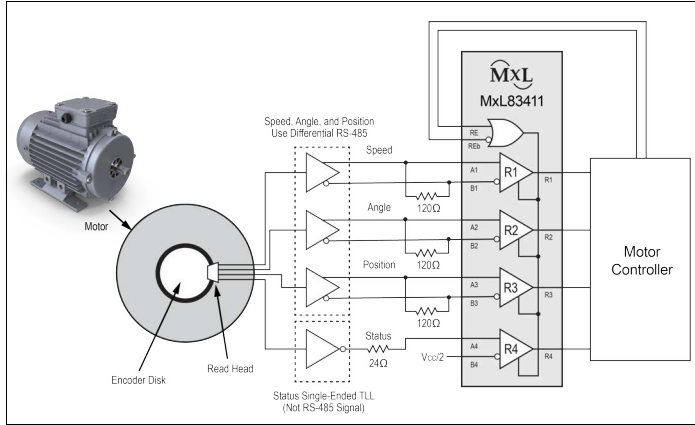


Figure 13: Application Block Diagram of Multi-Protocol Receive Mode

Case 2: Logic inversion to TTL level output

The MxL83411 receiver can be configured as a logic inverter for standard high-speed output driver. In this configuration, the input signal can be connected to inverting input B (-) with voltage divider network connected to non-inverting input A (+).

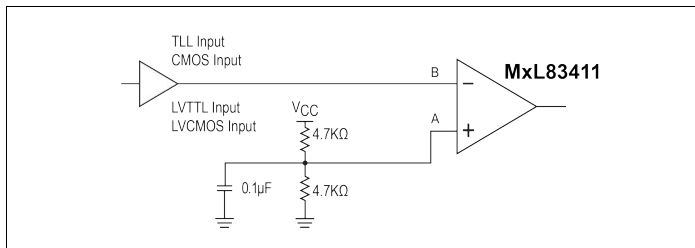


Figure 14: Multi-Protocol Receive Mode Support Case 2 (Logic Inversion)

Case 3: Single-ended RS-232 driver output to TTL level logic output (translation of RS-232 signal to TTL's level)

A single-ended RS-232 driver output can be converted to TTL level logic output by using the MxL83411 as a receiver. The RS-232 driver typically has single-ended output swing from -5.5V to +5.5V and can be directly connected into terminal A (+) of MxL83411 with terminal B (-) which connects to GND. Since the MxL83411 receiver inputs can tolerate up to ±15V, there is no requirement to attenuate the RS-232 signal at terminal A (+) input. This configuration supports conversion of RS-232 driver up to approximately 3Mbps.

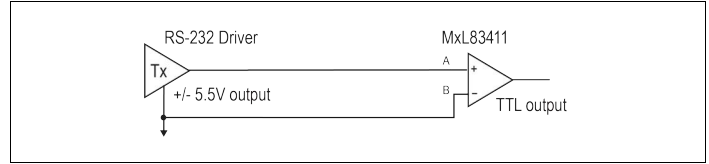


Figure 15: Multi-Protocol Receive Mode Support Case 3a

In some cases, the RS-232 driver output levels can be as high as ±15V. For this special case, a resistor divider network with 2KΩ and 3KΩ provides the required attenuation to put it into the correct operating voltage range. It attenuates the RS-232 signal by 40%, reducing the output level from ±15V to ±9V. It allows conversion of the RS-232 driver output up to 1.5Mbps.

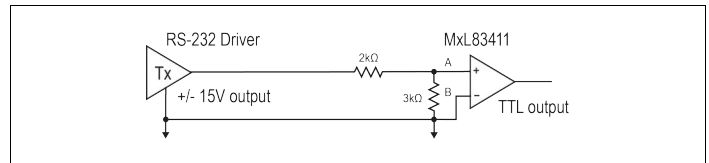


Figure 16: Multi-Protocol Receive Mode Support Case 3b

Note that due to the increased skew when input voltage exceeds ±3.0V (or 6V peak to peak), the multi-protocol receive mode configuration could not operate at the highest data rates.

The following table lists the maximum data rate supported for multi-protocol receive mode operations.

Table 11: Multi-Protocol Receive Mode Data Rate Support

Device	Multi-Protocol Receive Mode Input Voltage	Maximum Data Rate Achievable ¹
MxL83411	±0.5V	10Mbps
	±1.0V	10Mbps
	±2.0V	10Mbps
	±3.0V	10Mbps
	±5.0V	4Mbps
	±7.0V	2Mbps
	±9.0V	1.5Mbps
	±11.0V	1Mbps
	±13.0V	500Kbps
	±15V	200Kbps

1. These values are representative performance of a typical device with duty cycle of 60/40 percent.

Mechanical Dimensions

NSOIC16

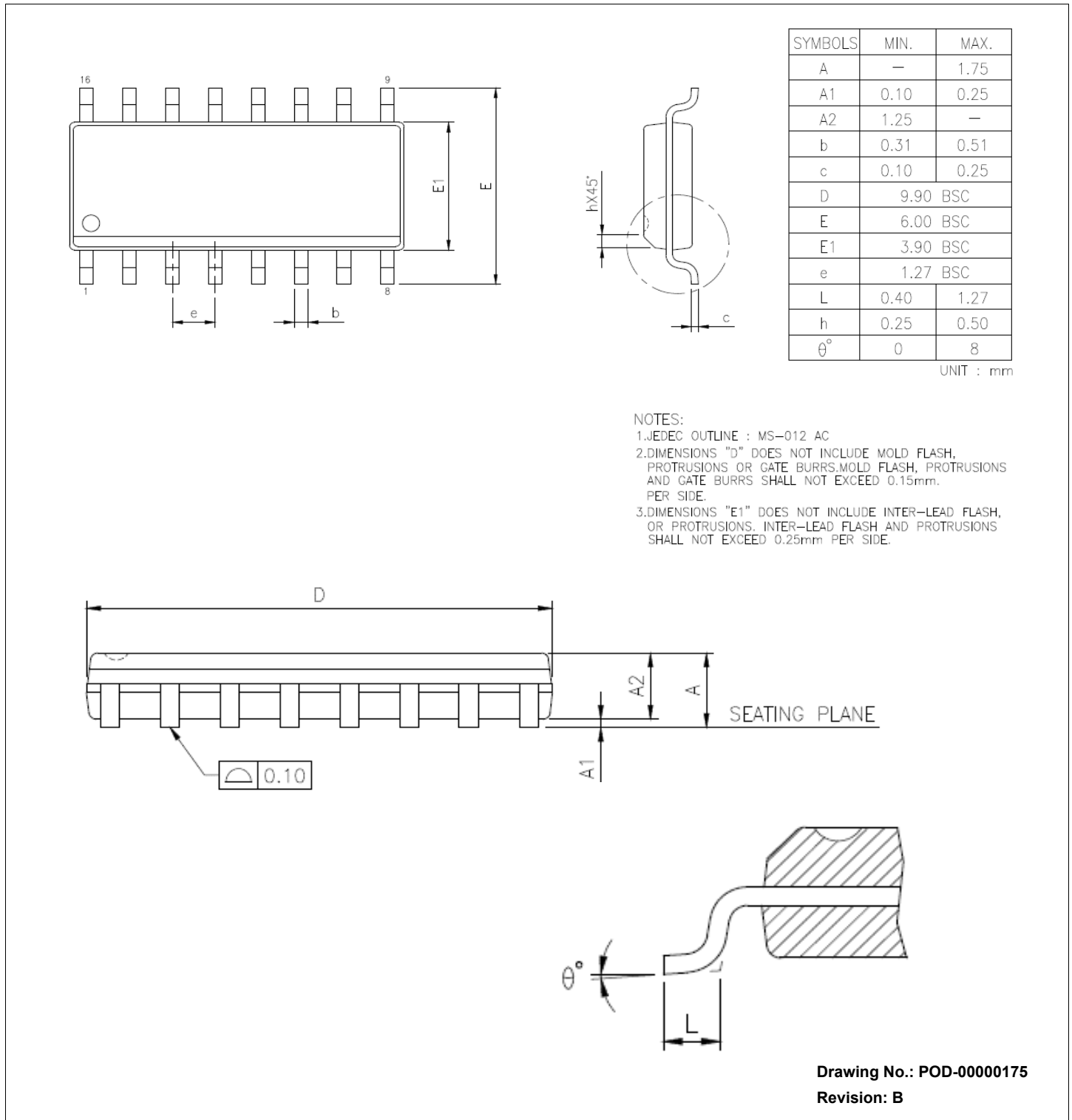


Figure 17: Mechanical Dimensions—NSOIC16

TSSOP16

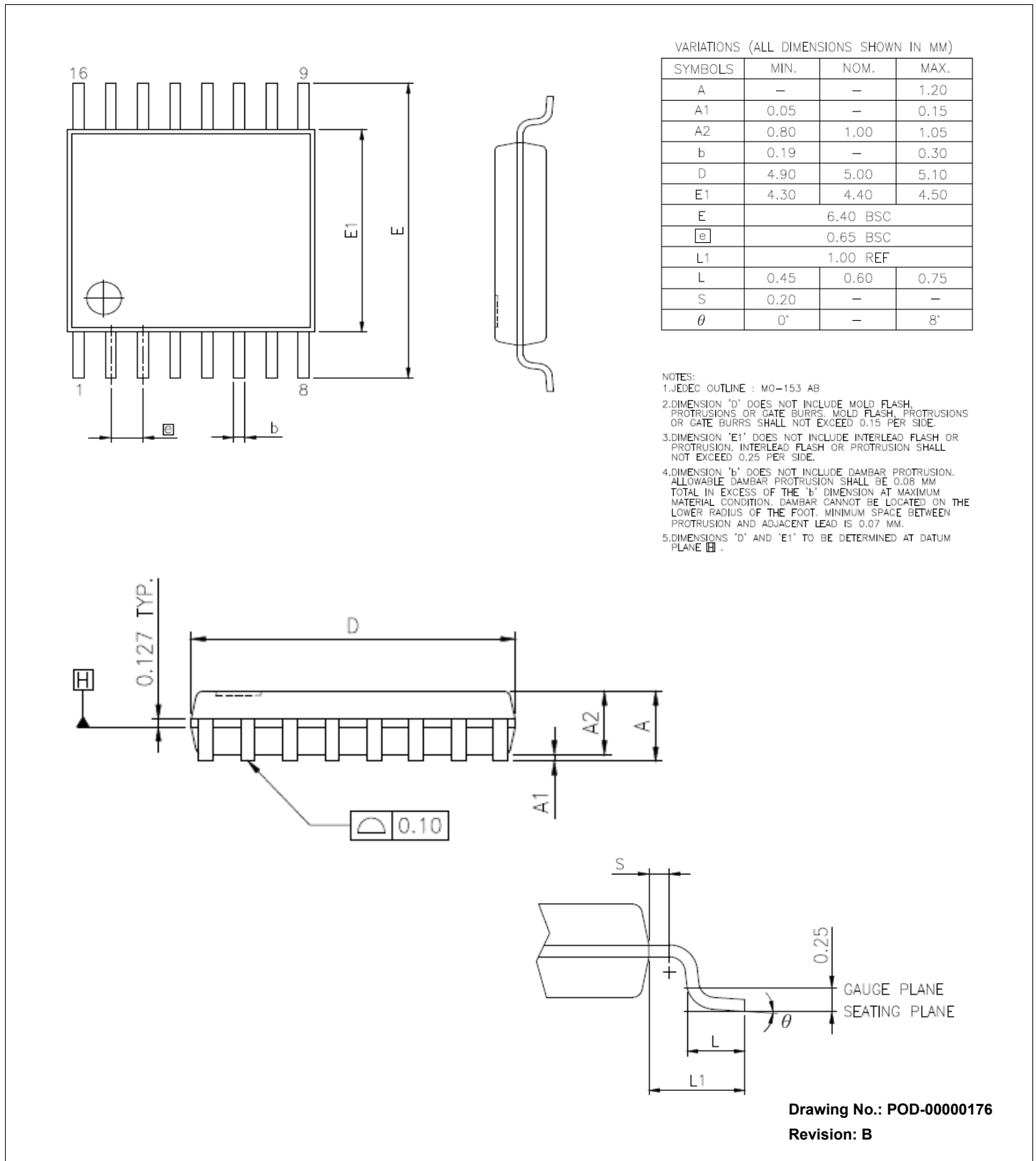


Figure 18: Mechanical Dimensions—TSSOP16

Ordering Information

Table 12: Ordering Information

Ordering Part Number	Data Rate (Mbps)	Operating Temperature Range	Package	Packaging
MXL83411E-ADA-R	10	-40°C to 125°C	NSOIC16	Tape and Reel
MXL83411E-AGA-R	10	-40°C to 125°C	TSSOP16	Tape and Reel
MXL83411I-ADA-R	10	-40°C to 85°C	NSOIC16	Tape and Reel
MXL83411I-AGA-R	10	-40°C to 85°C	TSSOP16	Tape and Reel
MXL83411E-ADA-EVK-1	MxL83411 Evaluation Kit NSOIC16			
MXL83411E-AGA-EVK-1	MxL83411 Evaluation Kit TSSOP16			

Note:

- For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL83411.
- For more information about the EVKs, refer to the *MxL83411 Quad Receiver EVK User Manual (029UM)*.



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