SP3082E/ SP3083E/ SP3084E/ SP3085E/ SP3088E

Data Sheet

Advanced-Failsafe RS-485 / RS-422 Transceivers

1/8th Unit Load, Slew-Rate Limited, ±15kV ESD-Protected

General Description

The SP3082E-SP3088E family of RS-485 devices are designed for reliable, bidirectional communication on multipoint bus transmission lines. Each device contains one differential driver and one differential receiver. The SP3082E, SP3085E and SP3088E are half-duplex devices; other part numbers are full-duplex. All devices comply with TIA/EIA-485 and TIA/EIA-422 standards. Lead-free and RoHS compliant packages are available for all models.

These devices are ruggedized for use in harsh operating conditions over the entire common-mode voltage range from -7V to +12V. Receivers are specially designed to fail-safe to a logic high output state if the inputs are left un-driven or shorted. All RS-485 bus-pins are protected against severe ESD events up to ±15kV (Air-Gap and Human Body Model) and up to ±8kV Contact Discharge (IEC 61000-4-2). Drivers are protected from excess current flow caused by bus contention or output short-circuits by both an internal current limit and a thermal-overload shutdown. Devices are rated for industrial (-40 to +85ºC) operating temperatures. Receivers have exceptionally high input impedance, which places only 1/8th the standard load on a shared bus. Up to 256 transceivers may coexist while preserving full signal margin.

All devices operate from a single 5.0V power supply and draw negligible quiescent power. All versions except the SP3084E may independently enable and disable their driver and receiver and enter a low power shutdown mode if both driver and receiver are disabled. All outputs maintain high impedance in shutdown or when powered-off.

SP3084E obsolete

Features

- 5.0V single supply operation
- Receiver failsafe on open, shorted or terminated lines
- 1/8th Unit Load, 256 transceivers on bus
- Robust ESD protection for RS-485 pins
  - ±15kV Air-Gap Discharge
  - ±15kV Human Body Model
  - ±8kV Contact Discharge
- Controlled driver slew rates
  - 115kbps, Low EMI (SP3082E)
  - 500kbps, Low EMI (SP3083E, SP3084E, SP3085E)
  - High Speed, 20Mbps (SP3088E)
- Hot Swap glitch protection on control inputs
- Driver short circuit current limit and thermal shutdown for overload protection
- Ultra-low 400µA quiescent current
- 1µA shutdown mode (except SP3084E)
- Industry standard package footprints

Applications

- Motor Control
- Building Automation
- Security Systems
- Remote Meter Reading
- Long or un-terminated transmission lines

Ordering Information - page 27

Product Selector Guide

SP3084E obsolete

Table 1: Product Selector Guide

Part Number	Duplex	Data Rate (Mbps)	Shutdown	Receiver & Driver Enable	Transceivers on Bus	Footprint	Pin-Compatible Upgrade from:
SP3082E	Half	0.115	Yes	Yes	256	SN75176	SP483, MAX3082
SP3083E	Full	0.5	Yes	Yes	256	SN75180	MAX3083
SP3084E	Full	0.5	No	No	256	SN75179	MAX3084
SP3085E	Half	0.5	Yes	Yes	256	SN75176	MAX3085
SP3088E	Half	20	Yes	Yes	256	SN75176	SP1481, MAX3088

Revision History

Document No.	Release Date	Change Description
M	2/22/07	Legacy Sipex Datasheet.
1.0.0	06/23/09	Convert to Exar format and change revision to 1.0.0.
1.0.1	08/26/11	Correct type error to Vcc range on page 4 from Vcc = 5.0V +/-5% to Vcc = 5.0V +/-10%. Add +/-65V transient over voltage tolerance to ABS Maximum Ratings and add Figure 11 test circuit.
1.0.2	08/29/19	Update to MaxLinear format, update Ordering Information. Move Pin Information section to just before Detailed Description section, ESD Ratings to below Absolute Maximum Ratings section, and Product Selector Guide to page 1. Correct Half Duplex Network Typical Application. Removed obsolete SP3080E, SP3081E, SP3086E and SP3087E.
2.0.0	07/22/22	**Updated:** ■ In "Figure 54: Driver Enable and Disable Times Test Circuit and Timing Diagram", ■ t_{ZL} replaced with t_{ZH}. ■ $t_{ZL(SHDN)}$ replaced with $t_{ZH(SHDN)}$. ■ t_{LZ} replaced with t_{HZ}. ■ In "Figure 55: Driver Enable and Disable Times Test Circuit and Timing Diagram", V_{CC} OUT replaced with OUT and V_{CC} added on the right side. ■ In "Receiver Enable and Disable Timing Diagram" figure, t_{LZ} relocated. ■ In general, all figures including subscripts updated to show subscripts properly. **Added:** ■ In "Absolute Maximum Ratings" table, Receiver output current parameter. **Removed:** ■ In "Electrical Characteristics" table, Receiver output short circuit current parameter. ■ In "Ordering Information" table, SP3084EEN-L/TR obsolete part number.

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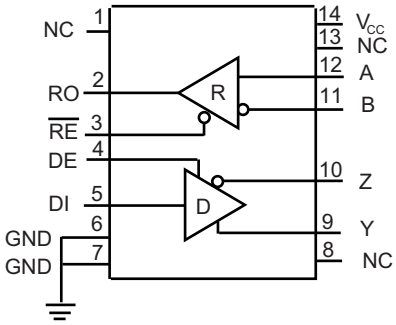
Device Architecture and Block Diagrams

SP3084E obsolete

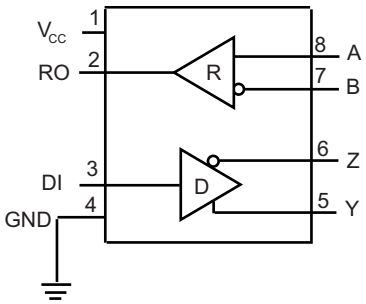
Devices are available in three industry standard architectures and footprints. In each footprint, there are three speed grades available.



14-pin Full Duplex:

SP3083E, 500kbps slew limited

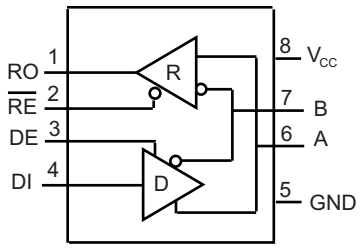
Figure 2: 14-pin Full Duplex



8-pin Full Duplex:

SP3084E, 500kbps slew limited

Figure 3: 8-pin Full Duplex



8-pin Half Duplex:

SP3082E, 115kbps slew limited

SP3085E, 500kbps slew limited

SP3088E, 20Mbps

Figure 4: 8-pin Half Duplex

Specifications

Absolute Maximum Ratings

Important: These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage V_{CC}		7.0	V
Input voltage at control input pins ($\overline{RE}$, DE)	–0.3	V_{CC}+ 0.3	V
Driver input voltage (DI)	–0.3	V_{CC}+ 0.3	V
Driver output voltage (A, B, Y & Z)	–13	13	V
Receiver output voltage (RO)	–0.3	V_{CC}+ 0.3	V
Receiver input voltage (A, B)	–13	13	V
Voltage input range, transient pulse, A, B, Y and Z through 100Ω, see Figure 59	–65	65	V
Receiver output current	–95	95	mA
Package Power Dissipation			
Maximum junction temperature		150	°C
8-pin SO Θ_{JA}		128.4	°C/W
14-pin SO Θ_{JA}		86	°C/W
Operating Temperature Ranges			
Storage temperature range	–65	150	°C
Lead temperature (soldering, 10s)		300	°C

ESD Ratings

Table 2: ESD Ratings

Parameter	Limit	Units
HBM - Human Body Model (pins A, B, Y & Z)	±15	kV
HBM - Human Body Model (pins RO, DI, DE)	±2	kV
IEC 1000-4-2 Airgap Discharge (pins Y, Z, A & B)	±15	kV
IEC 1000-4-2 Contact Discharge (pins Y, Z, A & B)	±8	kV

Recommended Operating Conditions

SP3084E obsolete

V_{CC} = 5V ±10%, T_{MIN} to T_{MAX}, unless otherwise noted, typical values are V_{CC} = 5V and T_A = 25°C.

Table 3: Recommended Operating Conditions

Recommended Operating Conditions		Minimum	Typical	Maximum	Unit
Supply voltage V_{CC}		4.5	5	5.5	V
Input voltage on A and B pins		–7		12	V
High-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		2		V_{CC}	V
Low-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		0		0.8	V
Output current	Driver	–60		60	mA
	Receiver	–8		8	
Signaling rate, $1/t_{UI}$	SP3082E			0.115	Mbps
	SP3083E, SP3084E, SP3085E			0.5	
	SP3088E			20	
Operating free air temperature, T_A	Industrial grade (E)	–40		85	°C

1. The least positive (most negative) limit is designated as the maximum value.

Electrical Characteristics

Table 4: Electrical Characteristics

Parameter		Test Condition		Minimum	Typical	Maximum	Units
Digital Input Signals: DI, DE, $\overline{RE}$							
Logic input thresholds		High, V_{IH}		2.0			V
		Low, V_{IL}				0.8	
Logic input current		T_A = 25°C, after first transition				±1	µA
Input hysteresis		T_A = 25°C			100		mV
Driver							
Differential driver output (V_{OD})		No load				V_{CC}	V
Differential driver output, Test 1		R_L= 100Ω (RS-422)		2		V_{CC}	V
		R_L= 54Ω (RS-485)		1.5	2.7	V_{CC}	
Differential driver output, Test 2		V_{CM} = -7 to +12V		1.5		V_{CC}	V
Change in magnitude of differential output voltage (ΔV_{OD})(1)		R_L= 54Ω or 100Ω				±0.2	V
Driver common mode output voltage (V_{CC})		R_L= 54Ω or 100Ω		1		3	V
Change in common mode output voltage (ΔV_{OC})		R_L= 54Ω or 100Ω				±0.2	uA
Driver short circuit current limit		-7V ≤ V_{OUT} ≤ 12V(5)				±250	mA
Output leakage current (Full-duplex versions, Y & Z pins)(2)		DE = 0, $\overline{RE}$ = 0, V_{CC} = 0 or 5.5V	V_{OUT} = 12V			125	µA
			V_{OUT} = -7V	–100			
Receiver							
Receiver input resistance		-7V ≤ V_{CM} ≤ 12V		96			kΩ
Input current (A, B pins)		DE = 0, $\overline{RE}$ = 0 V_{CC} = 0 or 5.5V	V_{IN} = 12V			125	µA
			V_{IN} = -7V	–100			
Receiver differential threshold (V_A - V_B)		-7V ≤ V_{CM} ≤ 12V		–200	–125	–40	mV
Receiver input hysteresis					25		mV
Receiver output voltage	V_{OH}	I_{OUT} = -8mA, V_{ID} = -40mV		V_{CC} - 1.5			V
	V_{OL}	I_{OUT} = -8mA, V_{ID} = -200mV				0.4	
High-Z receiver output current		V_{CC} = 5.5V, 0 ≤ V_{OUT} ≤ V_{CC}				±1	µA

Table 4: Electrical Characteristics

Parameter		Test Condition	Minimum	Typical	Maximum	Units
Supply and Protection						
Supply current	I_Q, active mode	No load, DI = 0 or V_{CC}		400	900	µA
	Shutdown mode	DE = 0, $\overline{RE}$ = V_{CC}, DI = V_{CC}			1	µA
Thermal shutdown temperature		Junction temperature		165		°C
Thermal shutdown hysteresis				15		

1. Change in magnitude of differential output voltage and change in magnitude of common mode output voltage are the changes in output voltage when DI input changes state.

2. Except devices which don't have DE or $\overline{RE}$ inputs.

3. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the device does not enter shutdown. If the enable inputs are held in this state for at least 600ns, the device is assured to be in shutdown. In this low power mode, most circuitry is disabled and supply current is typically 1nA.

4. Characterized, not 100% tested.

5. See Figure 52.

Timing Characteristics

SP3084E obsolete

Unless otherwise noted, V_{CC} = 5.0 ±0.5V, ambient temperature T_A from -40 to 85°C.

Table 5: SP3082E Driver Characteristics

Driver Characteristics	Conditions	Minimum	Typical	Maximum	Unit
Data signaling rate (1 / t_{UI})	Duty cycle 40 to 60%	115			kbps
Driver propagation delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF	500		2600	ns
Driver output rise / fall time (t_R, t_F)		667	1200	2500	ns
Driver differential skew (t_{PLH} - t_{PHL})				±200	ns
Shutdown to driver output valid (t_{DZV})				6000	ns

Table 6: SP3083E, SP3084E, SP3085E Driver Characteristics

Driver Characteristics	Conditions	Minimum	Typical	Maximum	Unit
Data signaling rate (1 / t_{UI})	Duty cycle 40 to 60%	500			kbps
Driver propagation delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF	250		1000	ns
Driver output rise / fall time (t_R, t_F)		200	530	750	ns
Driver differential skew (t_{PLH} - t_{PHL})				±100	ns
Driver enable to output high (t_{DZH})	SP3083E, SP3084E			2500	ns
Driver enable to output low (t_{DZL})				2500	ns
Driver disable from output high (t_{DHZ})				100	ns
Driver disable from output low (t_{DLZ})				100	ns
Shutdown to driver output valid (t_{DZV})				4500	ns

Table 7: SP3088E Driver Characteristics

Receiver Characteristics	Conditions	Minimum	Typical	Maximum	Unit
Data signaling rate (1 / t_{UI})	Duty cycle 40 to 60%	20			Mbps
Driver propagation delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF		12	20	ns
Driver output rise / fall time (t_R, t_F)			6	10	ns
Driver differential skew (t_{PLH} - t_{PHL})				±5	ns
Shutdown to driver output valid (t_{DZV})				250	ns

Table 8: Receiver Characteristics

Receiver Characteristic	Conditions	Minimum	Typical	Maximum	Unit
Receiver prop. delay SP3082E - SP3085E	C_L = 15pF, V_{ID} = ±2V		75	200	ns
Receiver prop. delay SP3088E				75	ns
Prop. delay skew SP3082E - SP3085E				±30	ns
Prop. delay skew SP3088E				±5	ns
Receiver output rise / fall time	C_L = 15pF			15	ns
Receiver enable to output high (t_{ZH})				50	ns
Receiver enable from output low (t_{ZL})				50	ns
Receiver disable from high (t_{HZ})				50	ns
Receiver disable from low (t_{LZ})				50	ns
Shutdown to receiver output valid (t_{ROV})				3500	ns
Time to shutdown[2, 3, 4]		50	200	600	ns

Typical Performance Characteristics

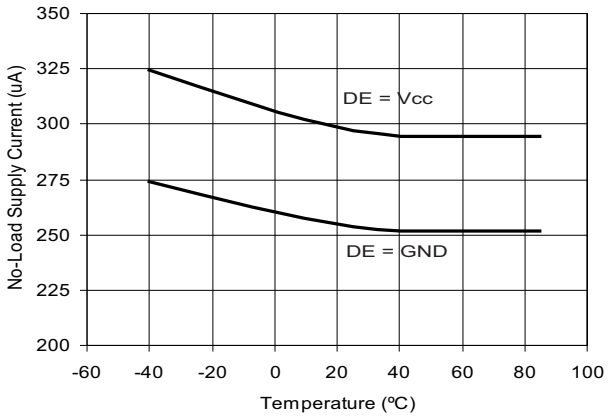


Figure 5: No-Load Supply Current vs. Temperature

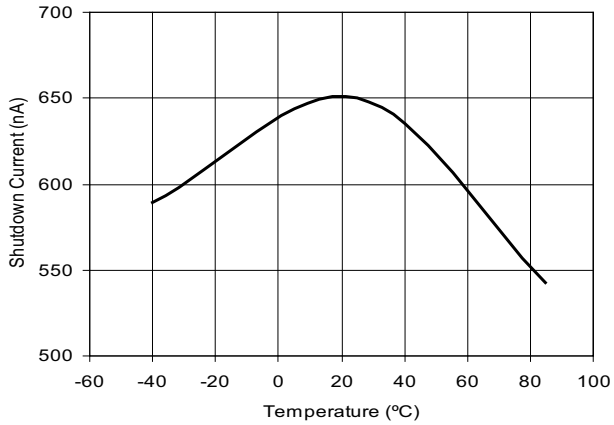


Figure 6: Shutdown Current vs. Temperature

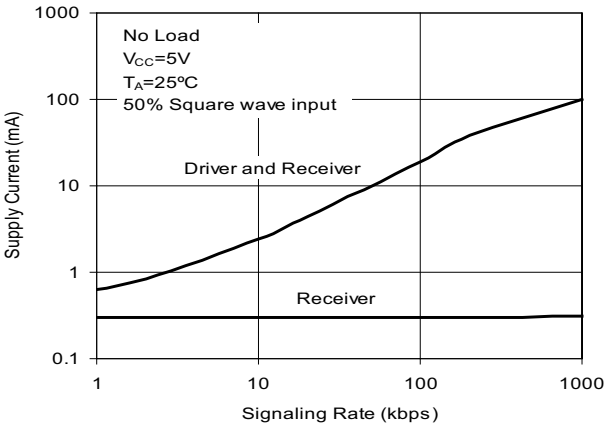


Figure 7: Supply Current vs. Signaling Rate (SP3082E)

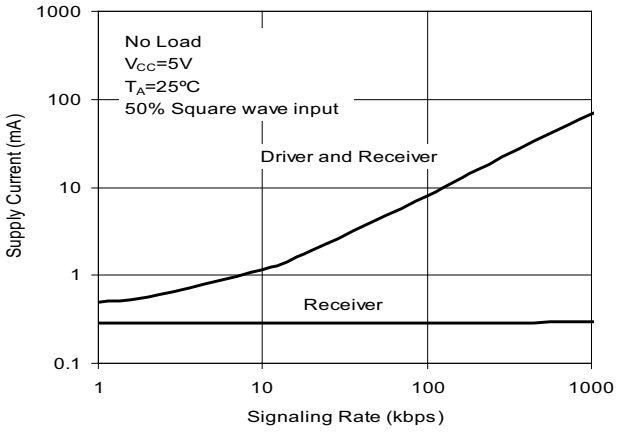


Figure 8: Supply Current vs. Signaling Rate (SP3083E - SP3085E)

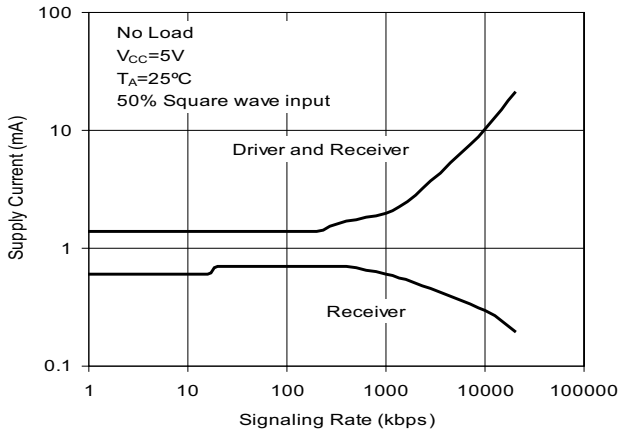


Figure 9: Supply Current vs. Signaling Rate (SP3088E)

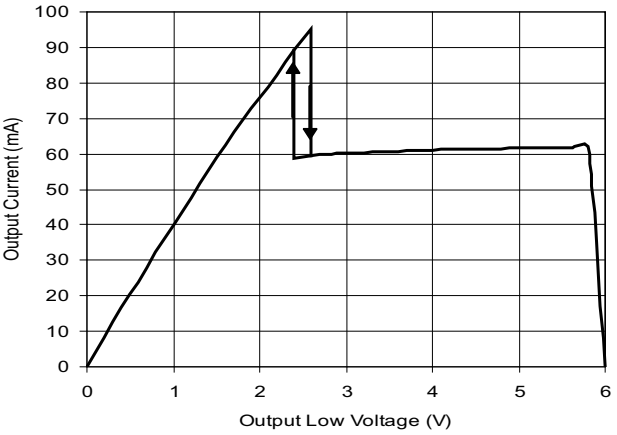


Figure 10: Output Current vs. Driver Output Low Voltage

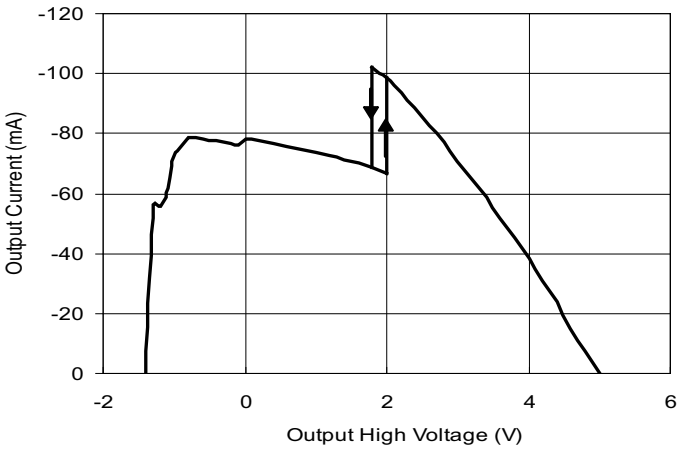


Figure 11: Output Current vs. Driver Output High Voltage

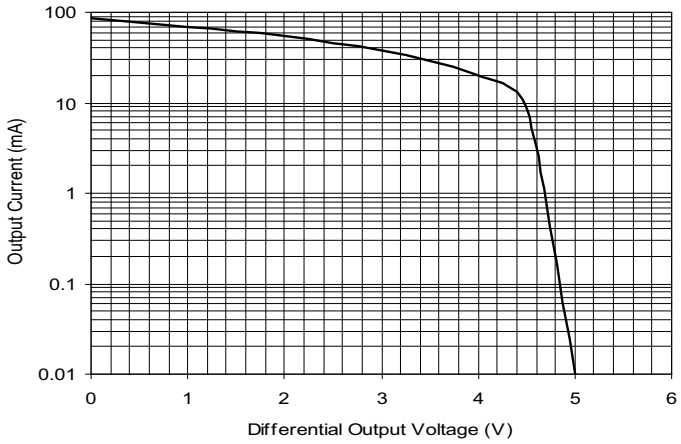


Figure 12: Driver Output Current vs. Differential Output Voltage

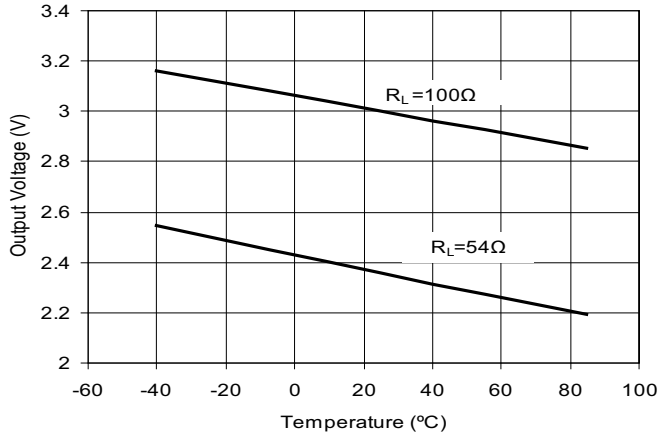


Figure 13: Driver Differential Output Voltage vs. Temperature

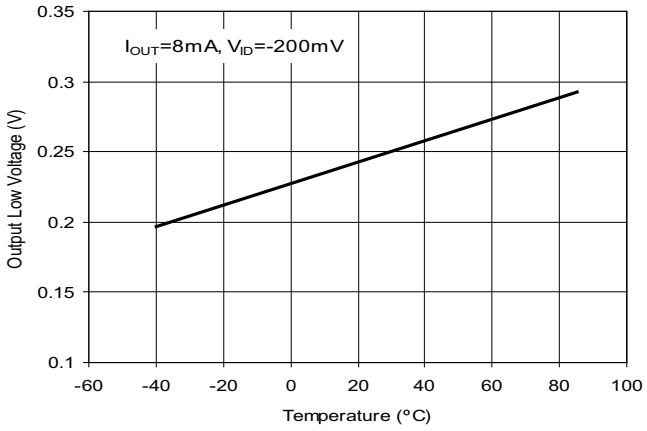


Figure 14: Receiver Output Low Voltage vs. Temperature

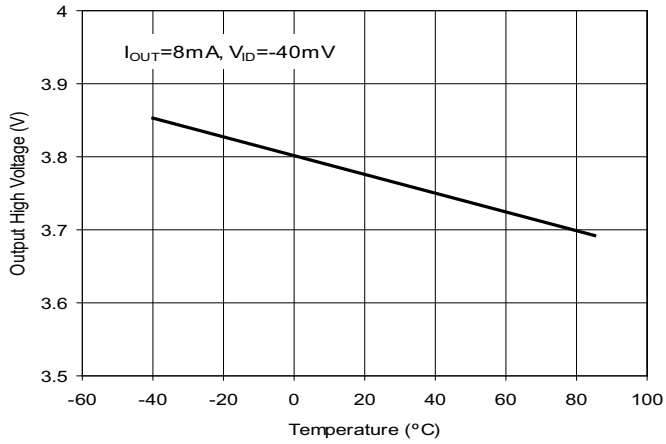


Figure 15: Receiver Output High Voltage vs. Temperature

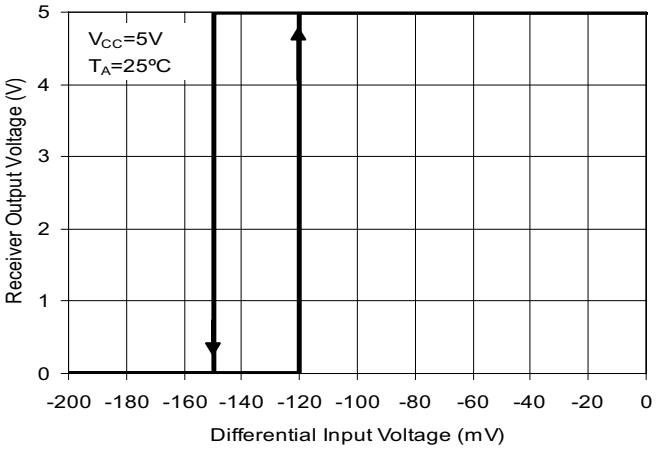


Figure 16: Receiver Output Voltage vs. Differential Input Voltage

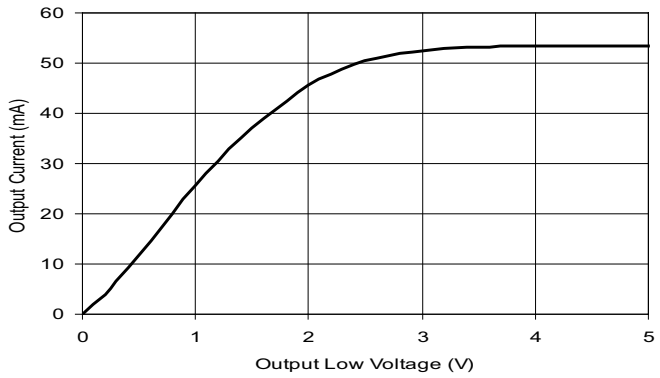


Figure 17: Output Current vs. Receiver Output Low Voltage

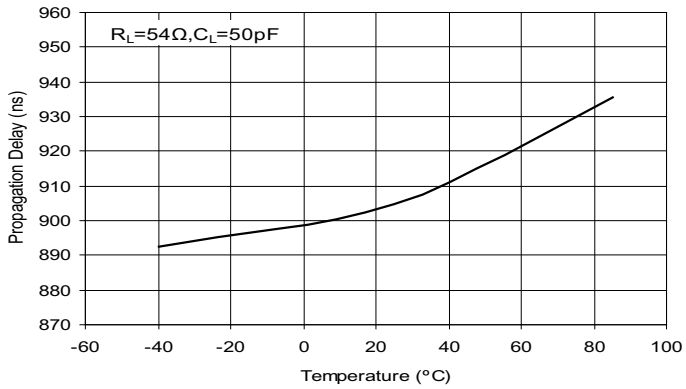


Figure 18: Driver Average Propagation Delay vs. Temperature (SP3082E)

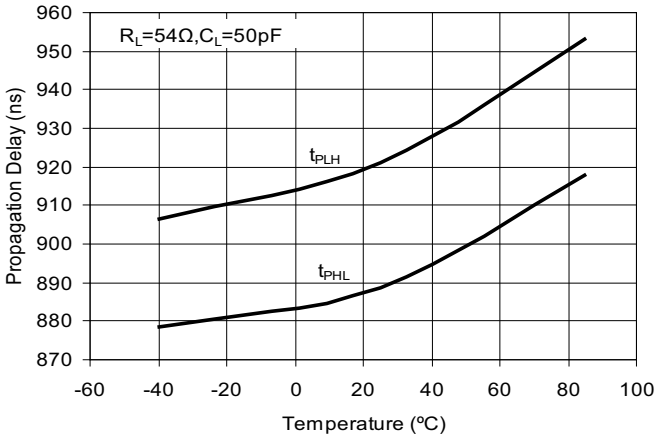


Figure 19: Driver Propagation Delay vs. Temperature (SP3082E)

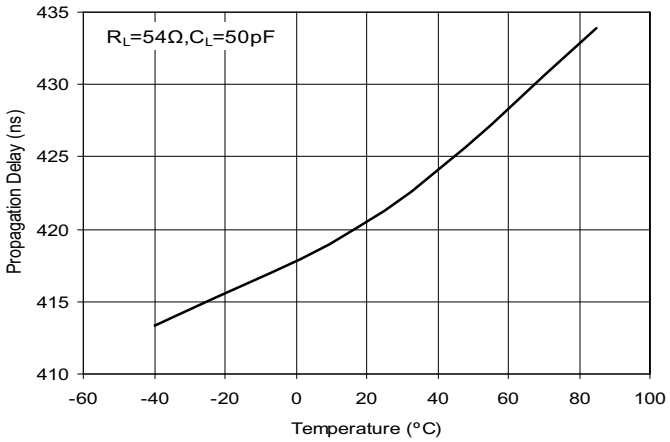


Figure 20: Driver Average Propagation Delay vs. Temperature (SP3083E - SP3085E)

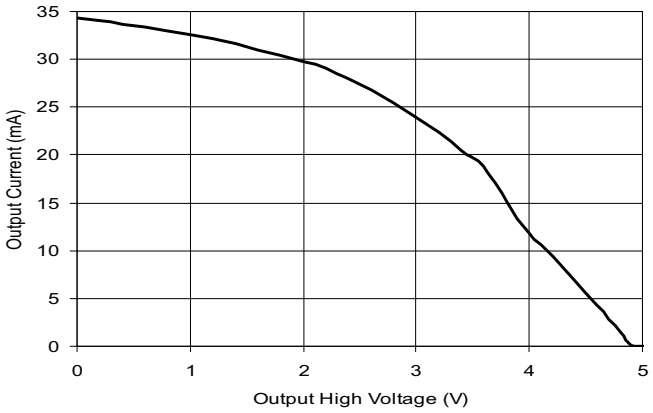


Figure 21: Output Current vs. Receiver Output High Voltage

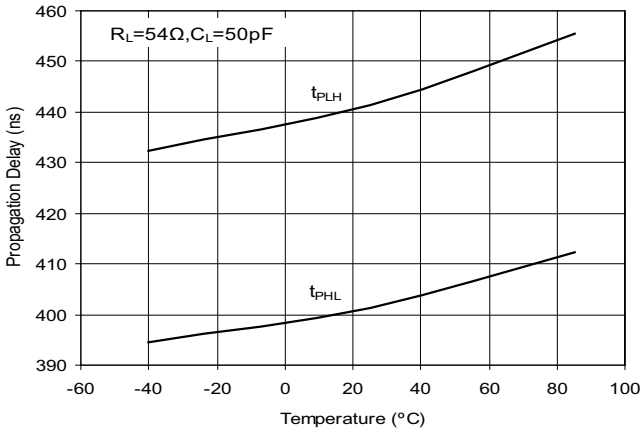


Figure 22: Driver Propagation Delay vs. Temperature (SP3083E - SP3085E)

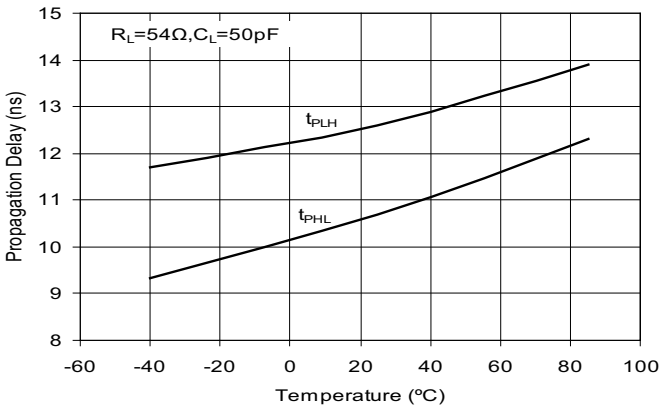


Figure 23: Driver Propagation Delay vs. Temperature (SP3088E)

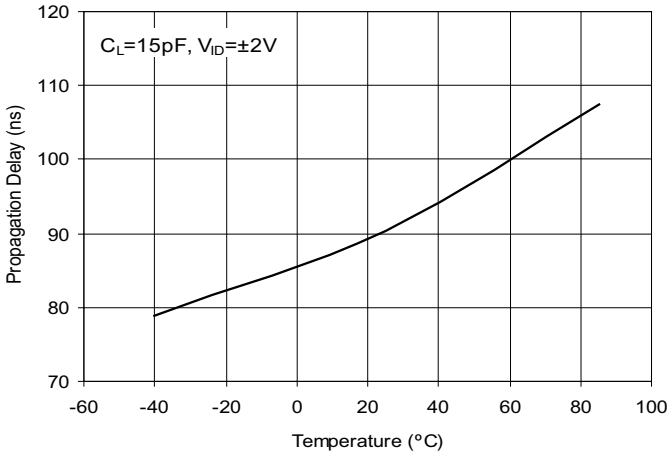


Figure 24: Receiver Average Propagation Delay vs.Temperature (SP3082E)

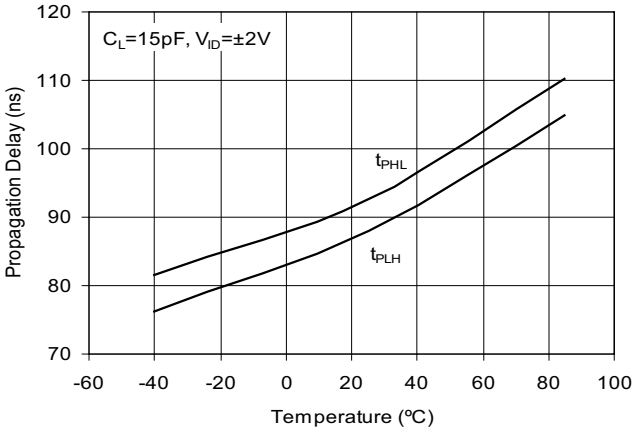


Figure 25: Receiver Propagation Delay vs. Temperature (SP3082E)

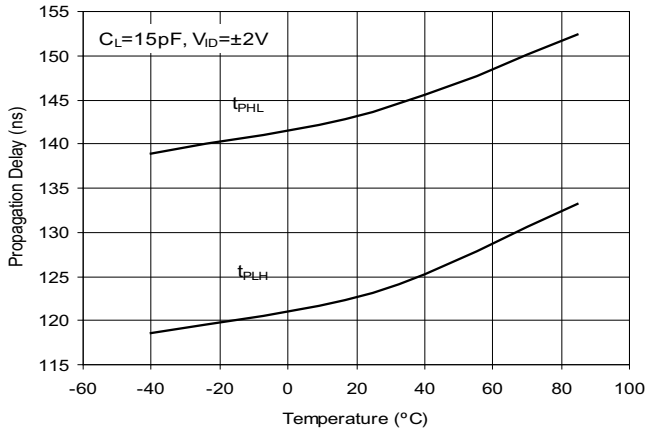


Figure 26: Receiver Propagation Delay vs. Temperature (SP3083E - SP3085E)

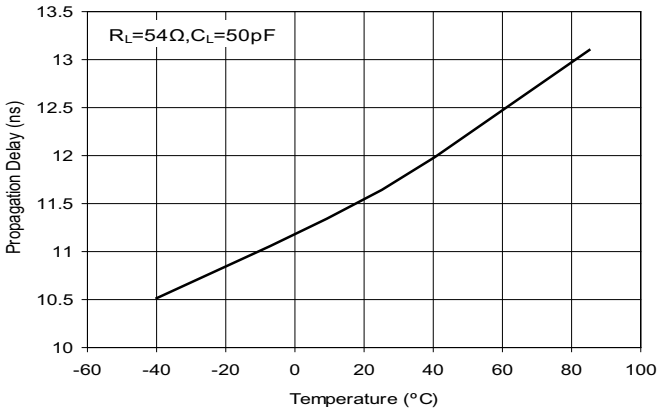


Figure 27: Driver Average Propagation Delay vs. Temperature (SP3088E)

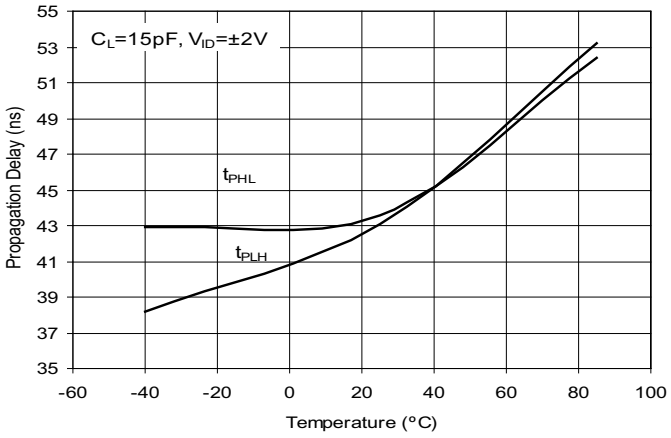


Figure 28: Receiver Propagation Delay vs. Temperature (SP3088E)

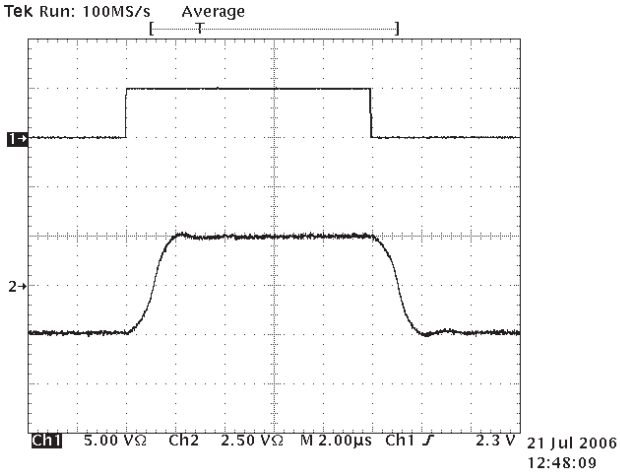


Figure 29: Driver Propagation Delay (SP3082E)

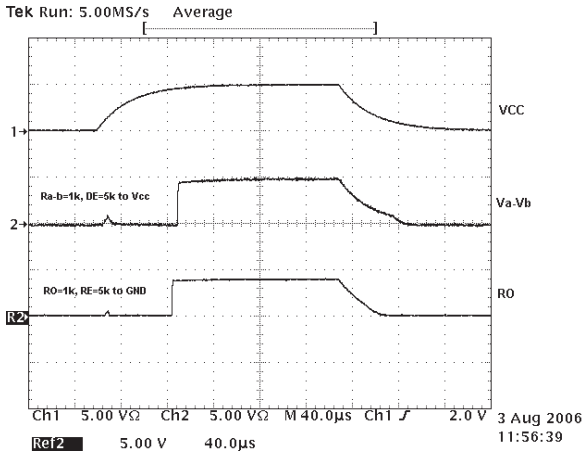


Figure 30: Driver and Receiver Hot Swap Performance vs. V_{CC}

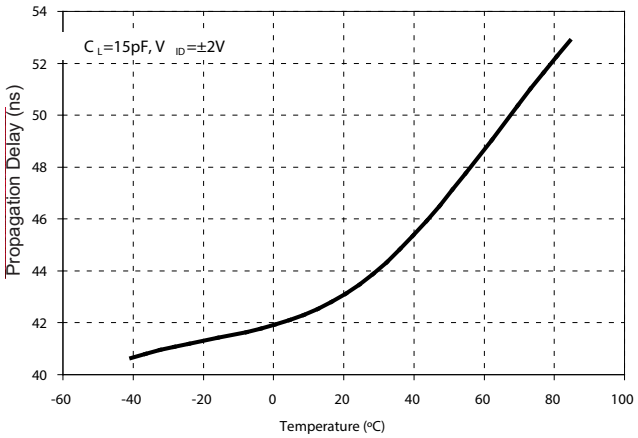


Figure 31: Receiver Average Propagation Delay vs. Temperature (SP3088E)

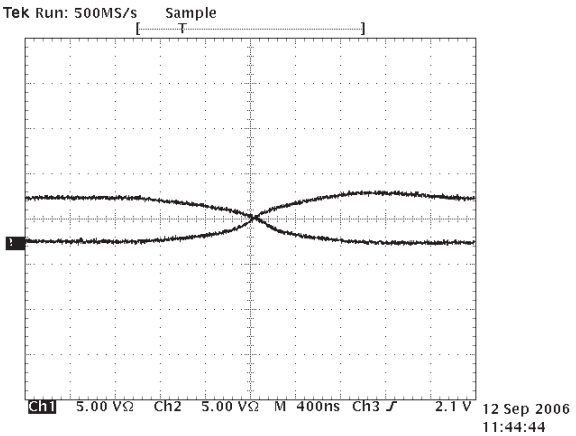


Figure 32: Driver Output Waveform Low to High (SP3082E)

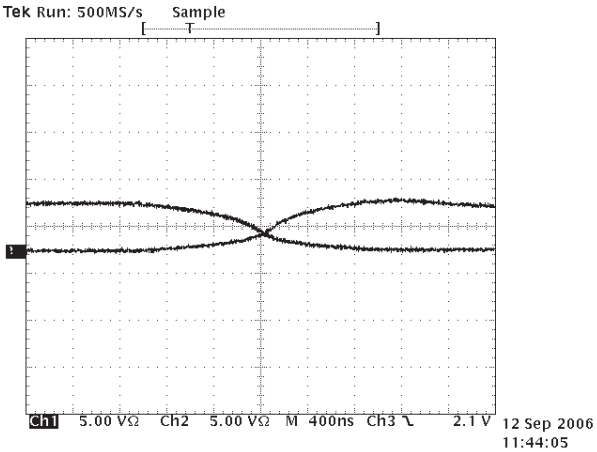


Figure 33: Driver Output Waveform High to Low (SP3082E)

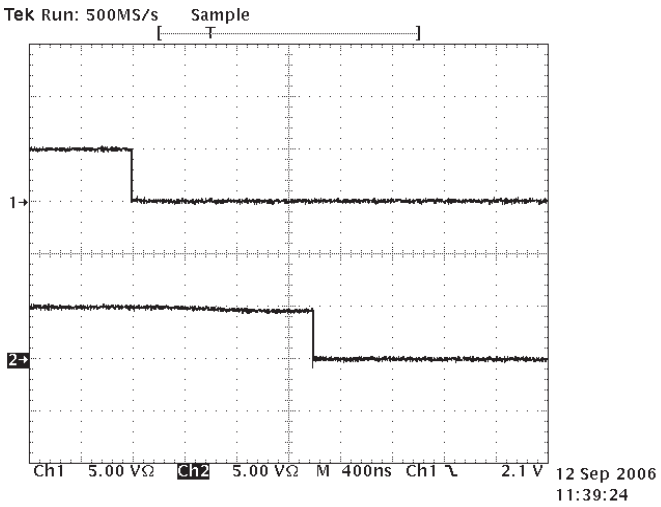


Figure 34: Driver and Receiver Waveform High to Low (SP3082E)

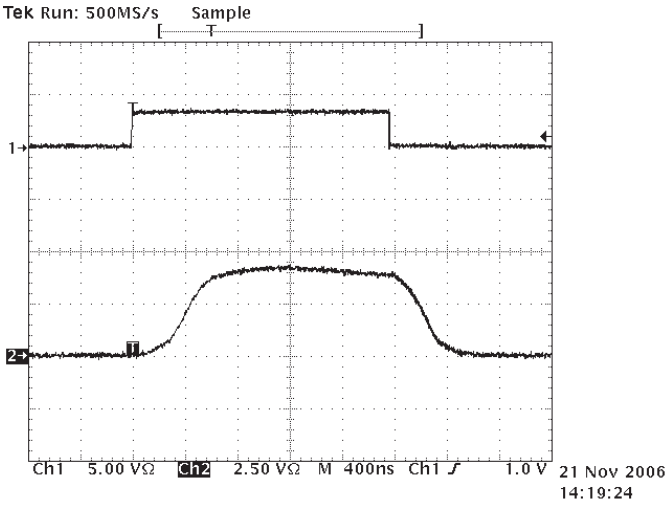


Figure 35: Driver Propagation Delay (SP3083E - SP3085E)

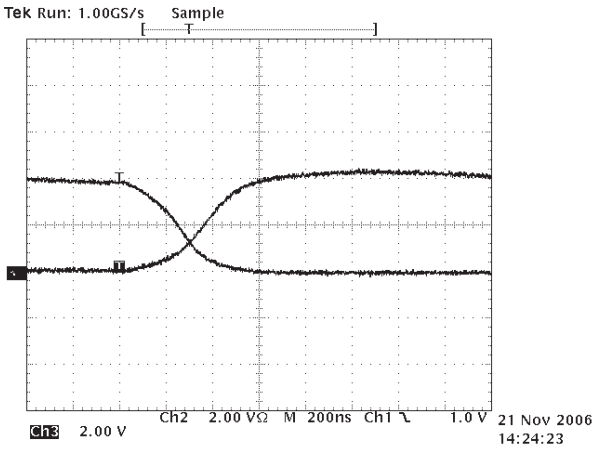


Figure 36: Driver Output Waveform Low to High (SP3083E - SP3085E)

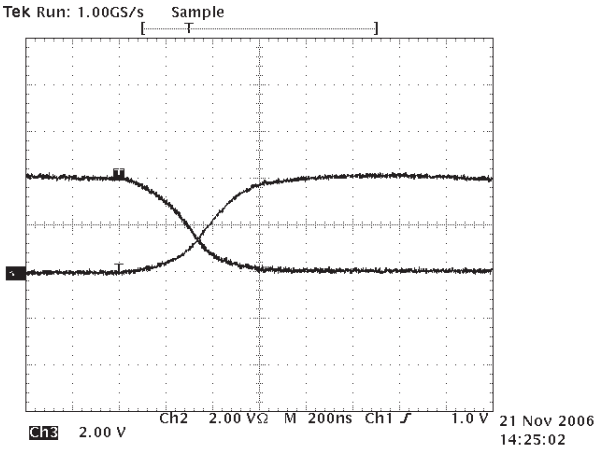


Figure 37: Driver Output Waveform High to Low (SP3083E - SP3085E)

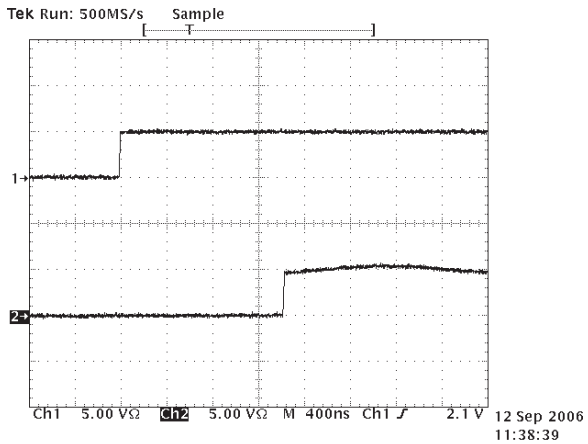


Figure 38: Driver and Receiver Waveform Low to High (SP3082E)

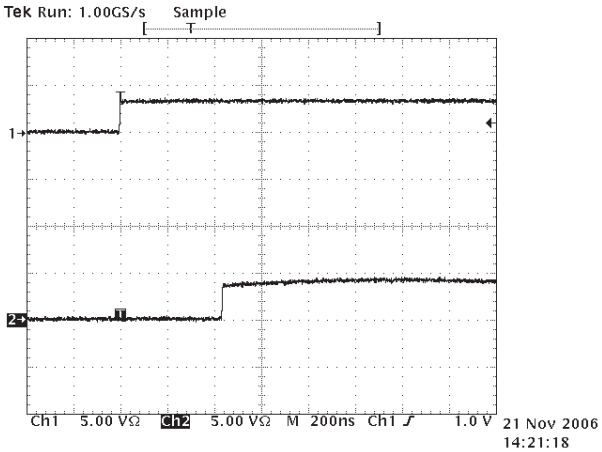


Figure 39: Driver and Receiver Waveform Low to High (SP3083E - SP3085E)

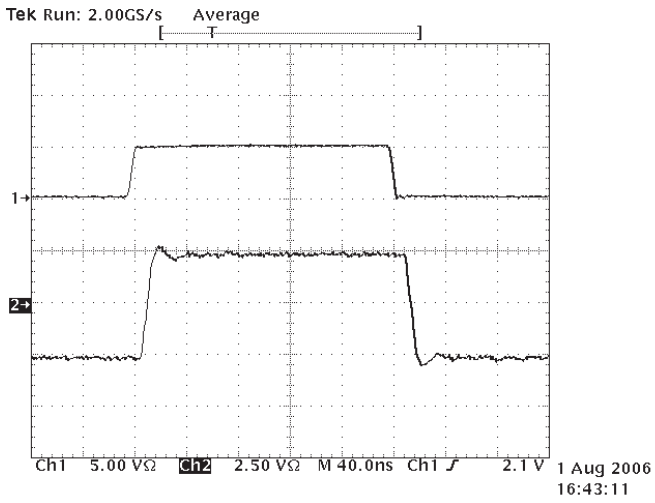


Figure 40: Driver Propagation Delay (SP3088E)

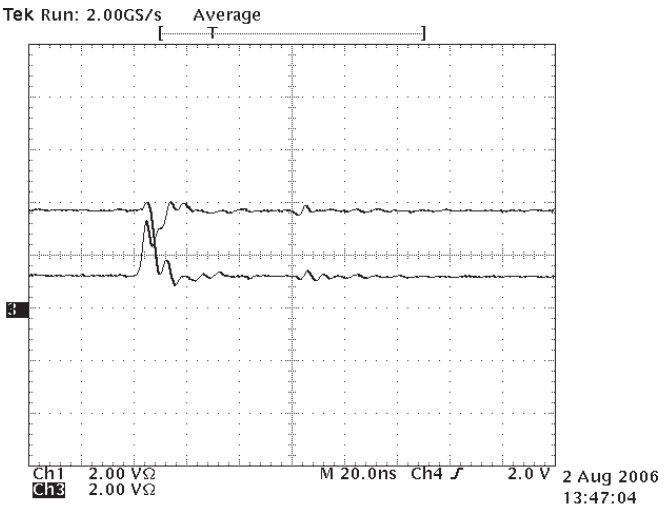


Figure 41: Driver Output Waveform Low to High (SP3088E)

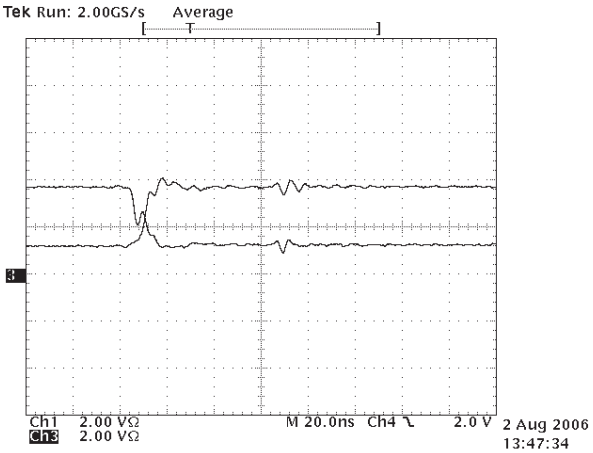


Figure 42: Driver Output Waveform High to Low (SP3088E)

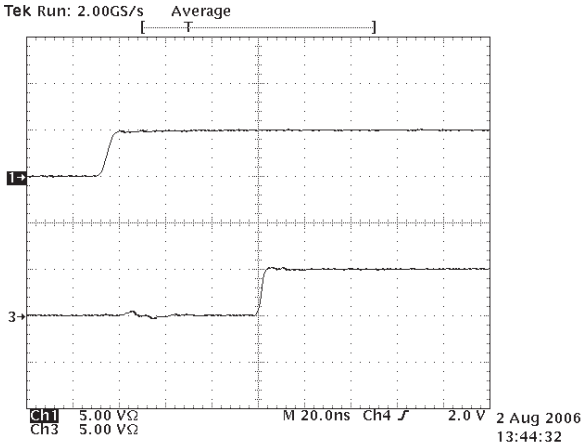


Figure 43: Driver and Receiver Waveform Low to High (SP3088E)

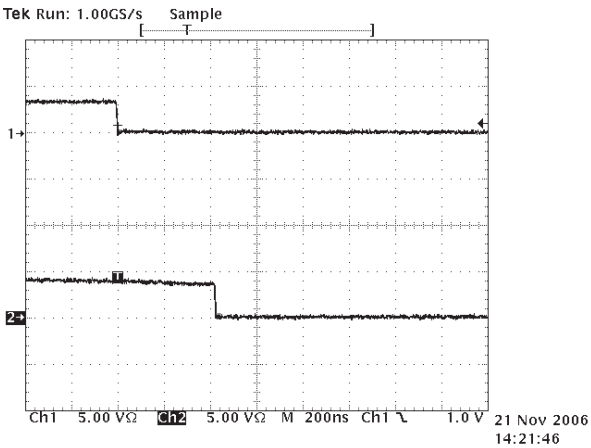


Figure 44: Driver and Receiver Waveform High to Low (SP3083E - SP3085E)

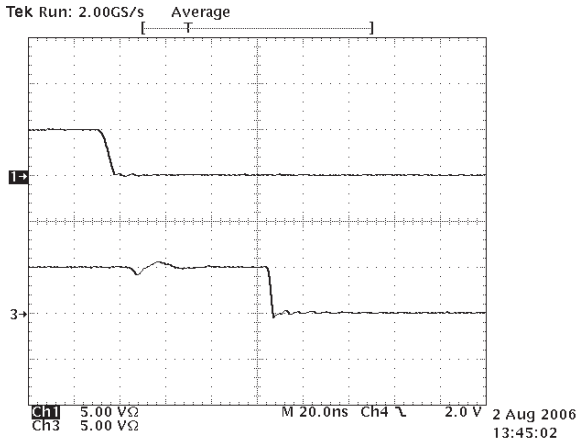


Figure 45: Driver and Receiver Waveform High to Low (SP3088E)

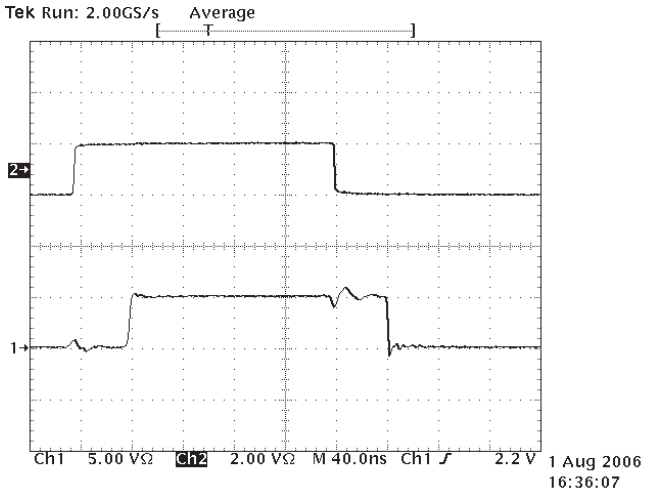


Figure 46: Receiver Propagation Delay (SP3088E)

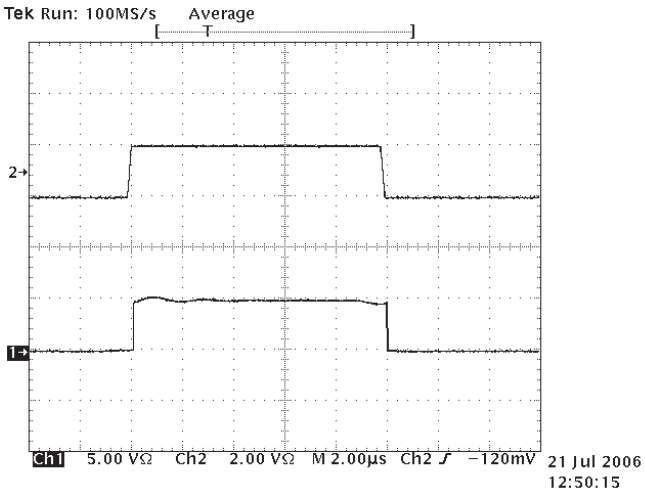


Figure 47: Receiver Propagation Delay (SP3082E)

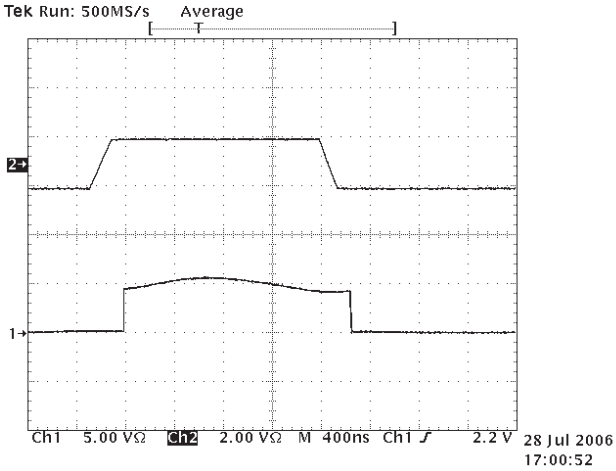


Figure 48: Receiver Propagation Delay (SP3083E - SP3085E)

Test Circuits and Timing Diagrams

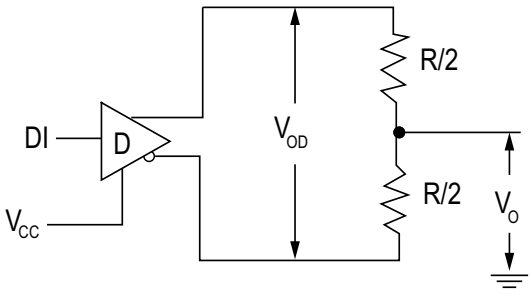


Figure 49: Driver DC Test Circuit

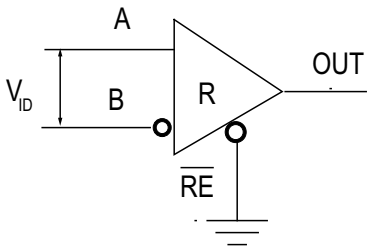


Figure 50: Receiver DC Test Circuit

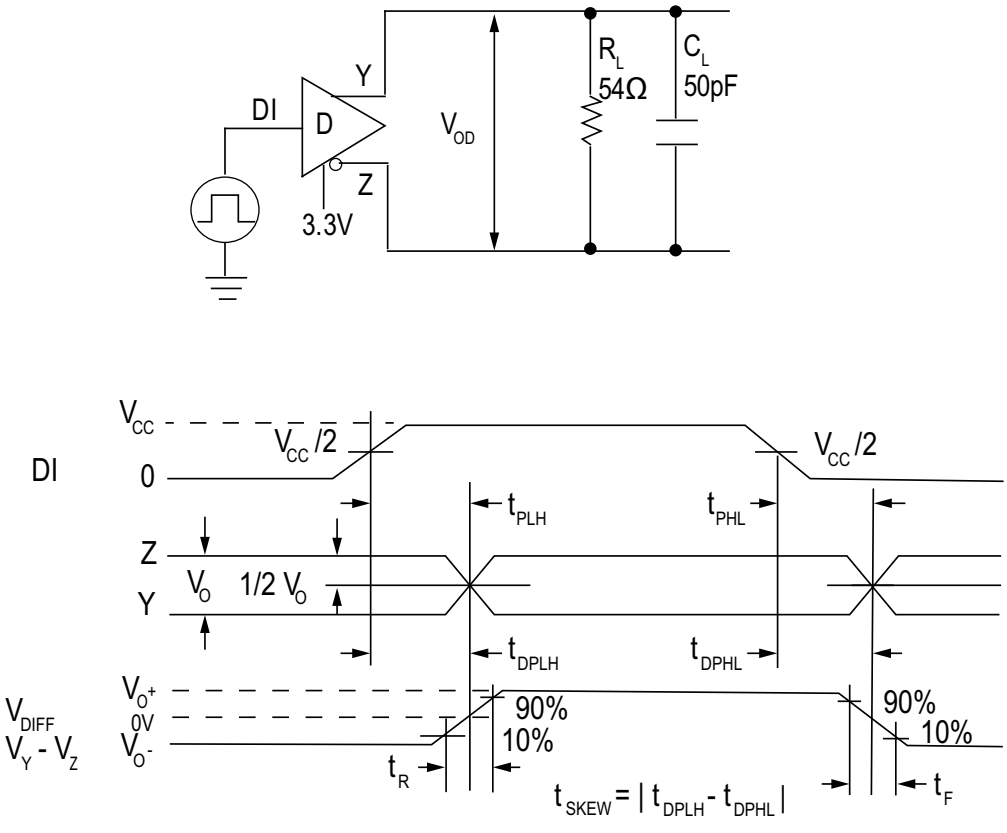


Figure 51: Driver Propagation Delay Time Test Circuit and Timing Diagram

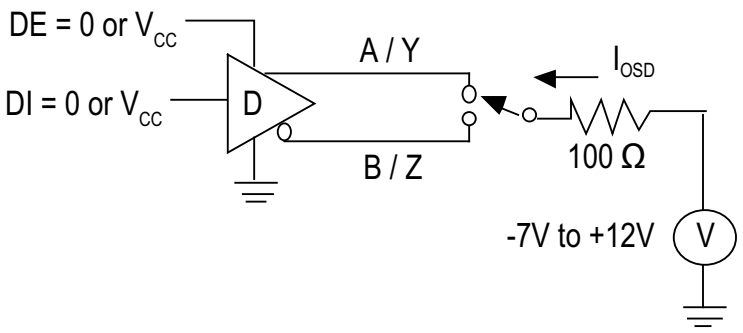


Figure 52: Driver Short Circuit Current Limit Test Circuit

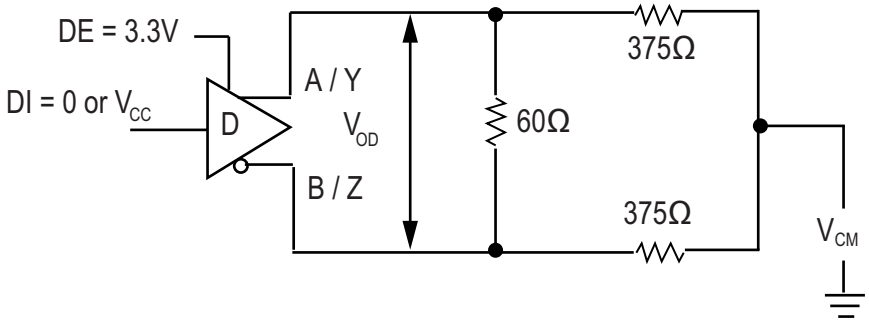


Figure 53: Driver Differential Output Test Circuit

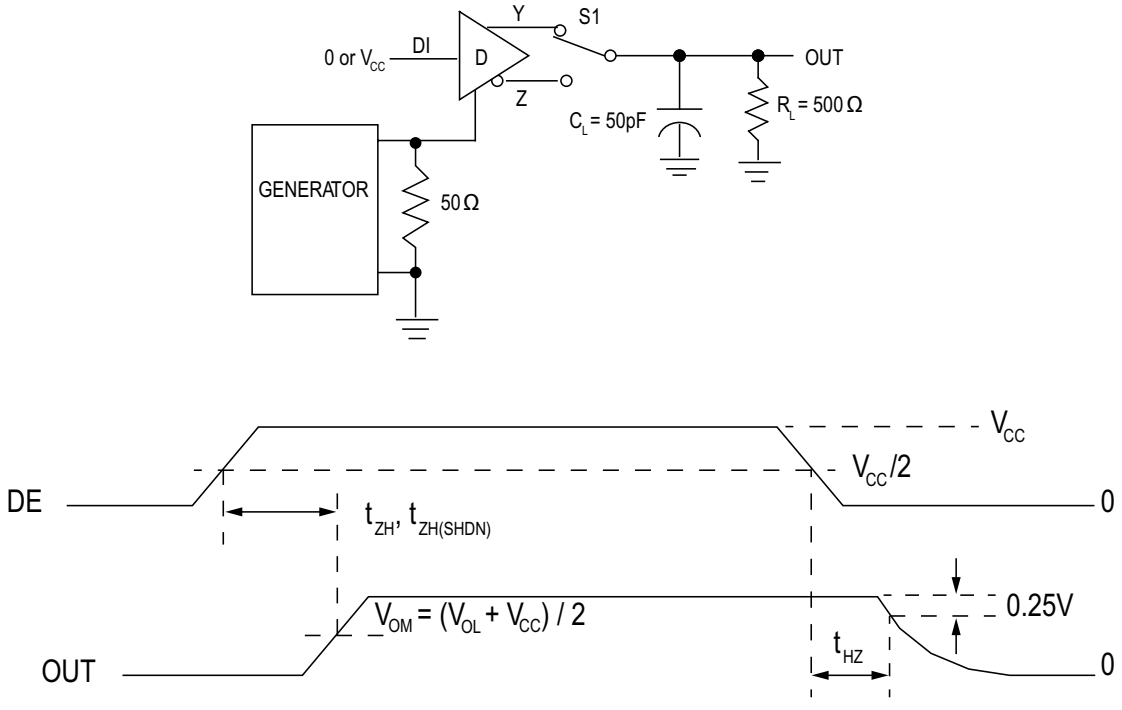


Figure 54: Driver Enable and Disable Times Test Circuit and Timing Diagram

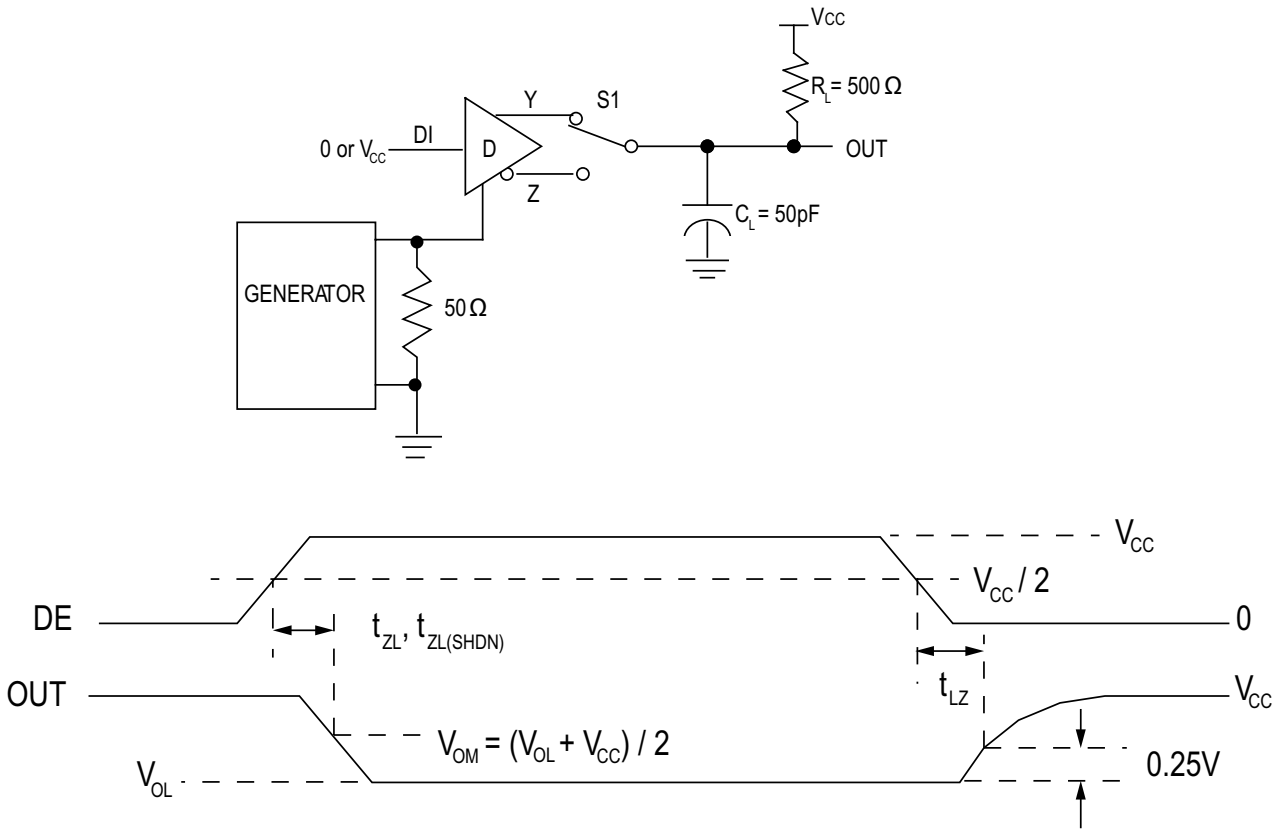


Figure 55: Driver Enable and Disable Times Test Circuit and Timing Diagram

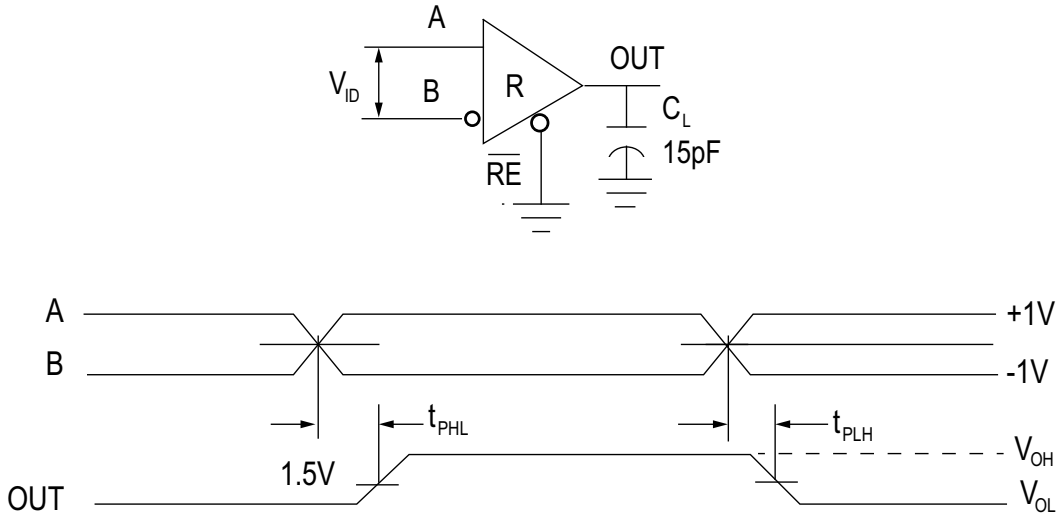


Figure 56: Receiver Propagation Delay Test Circuit and Timing Diagram

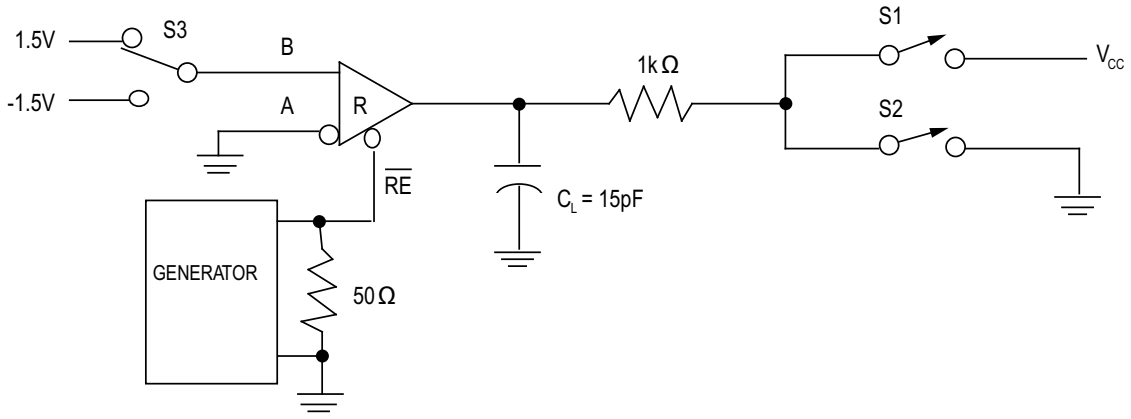


Figure 57: Receiver Enable and Disable Times Test Circuit

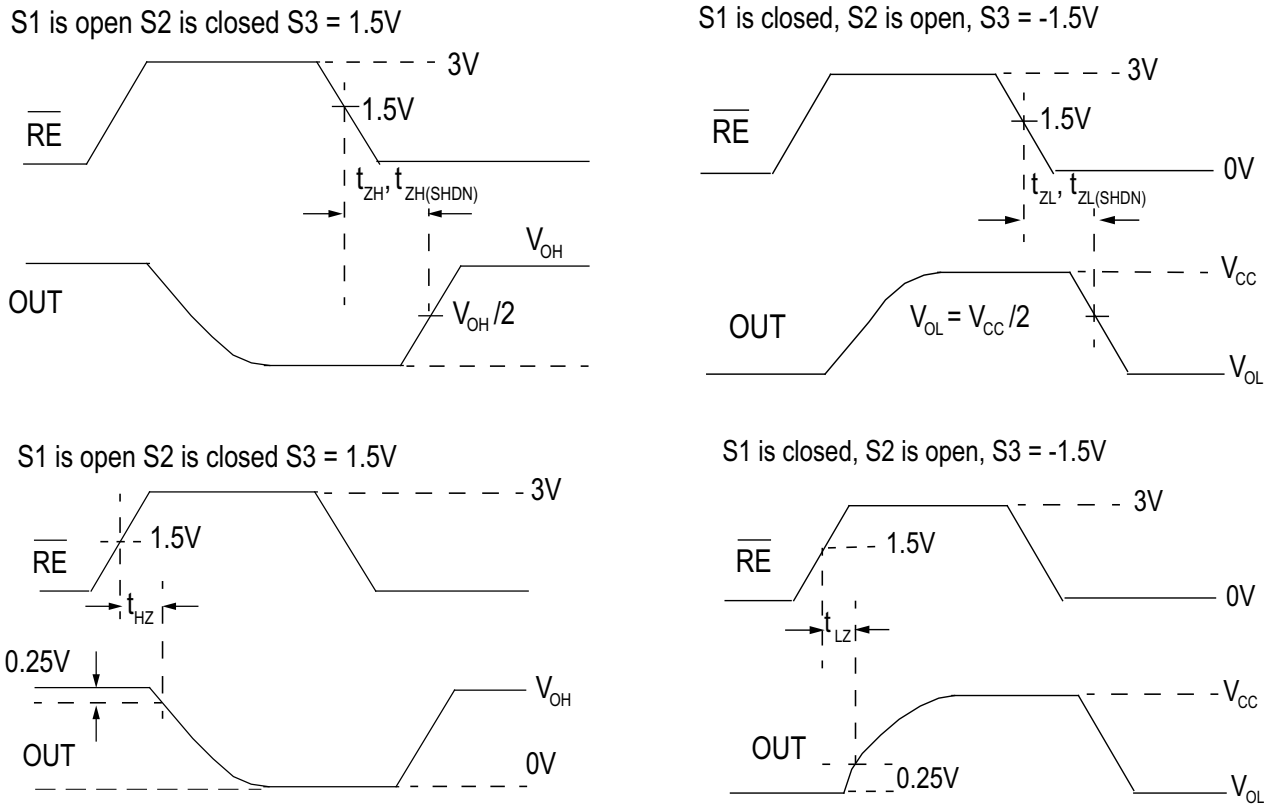
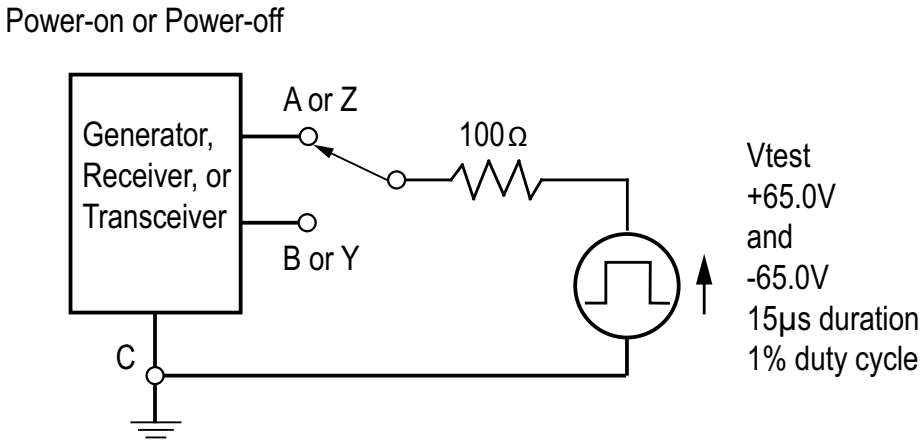


Figure 58: Receiver Enable and Disable Timing Diagram



1. Test is performed to ensure survivability only. Normal operation during transient is not specified.

Figure 59: Transient Over Voltage Tolerance Test Circuit

Function Tables

SP3084E obsolete

Table 9: SP3083E (Full Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shitdown	

Table 10: SP3083E (Full Duplex)

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	≥ -40mV	1
0	X	≤ -200mV	0
0	X	Open, Shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Table 11: SP3084E (Full Duplex)

Transmitting		
Input	Outputs	
DI	Y	Z
1	1	0
0	0	1
Open	1	0

Table 12: SP3084E (Full Duplex)

Receiving	
Inputs	Output
$V_A - V_B$	RO
≥ -40mV	1
≤ -200mV	0
Open / shorted	1

Table 13: SP3082E, SP3085E, SP3088E (Half Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shitdown	

Table 14: SP3082E, SP3085E, SP3088E (Half Duplex)

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	≥ -40mV	1
0	X	≤ -200mV	0
0	X	Open / shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Note: Receiver inputs -200mV < $V_A - V_B$ < -40mV should be considered indeterminate.

Pin Information

Pin Configurations

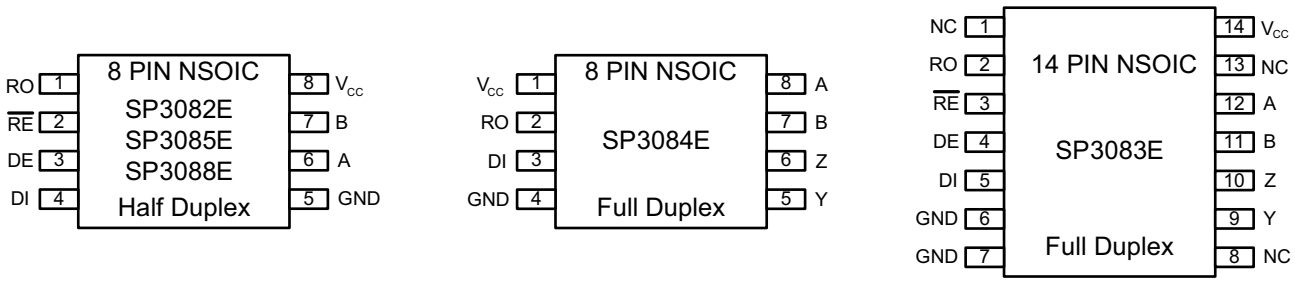


Figure 60: Pin Configurations

Pin Descriptions

SP3084E obsolete

Table 15: Pin Descriptions

Pin Number			Pin Name	Pin Function
Full Duplex Devices		Half Duplex Devices		
SP3083E	SP3084E	SP3082E, SP3085E, SP3088E		
2	2	1	RO	Receiver Output. When $\overline{RE}$ is low and if (A-B) ≥ -40mV, RO is High. If (A-B) ≤ -200mV, RO is low.
3	-	2	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode. $\overline{RE}$ is a hot swap input.
4	-	3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode. DE is a hot-swap input.
5	3	4	DI	Driver Input. With DE high, a low level on DI forces noninverting output low and inverting output high. A high level on DI forces noninverting output high and inverting output low.
6, 7	4	5	GND	Ground
9	5	-	Y	Noninverting Driver Output
10	6	-	Z	Inverting Driver Output
11	7	-	B	Inverting Receiver Input
-	-	7	B	Inverting Receiver Input and Inverting Driver Output
12	8	-	A	Noninverting Receiver Input
-	-	6	A	Noninverting Receiver Input and Noninverting Driver Output
14	1	8	V_{CC}	Positive Supply V_{CC}. Bypass to GND with a 0.1µF capacitor
1, 8, 13	-	-	NC	No connect, not internally connected.

1. On 14-pin packages connect both pins 6 and 7 to Ground.

Detailed Description

SP3084E obsolete

SP3082E - SP3088E are a family of advanced RS-485 /RS-422 transceivers. Each contains one driver and one receiver. These devices feature fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. The SP3082E, SP3083E, SP3085E and SP3088E also feature a hot-swap capability allowing live insertion without error data transfer.

The SP3082E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps. The SP3083E, SP3084E and SP3085E also offer slew-rate limits allowing transmit speeds up to 500kbps. The SP3088E driver slew rate is not limited, making transmit speeds up to 20Mbps possible.

The SP3082E, SP3085E and SP3088E are half-duplex transceivers, while the SP3083E and SP3084E are full duplex transceivers.

All devices operate from a single 5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

Receiver Input Filtering

SP3082E-SP3085E receivers incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases due to this filtering.

Advanced Fail Safe

Ordinary RS-485 differential receivers will be in an indeterminate state whenever A - B is less than ±200mV. This situation can occur whenever the data bus is not being actively driven. The Advanced Failsafe feature of the SP308xE family guarantees a logic-high receiver output if the receiver's differential inputs are shorted, open-circuit or if they are shunted by a termination resistor.

The receiver thresholds of the SP308xE family are very precise and offset by at least a 40mV noise margin from ground. This results in a logic-high receiver output at zero volts input differential while maintaining compliance with the EIA / TIA-485 standard of ±200mV.

Hot-Swap Capability

When a microprocessor or other logic device undergoes its power-up sequence, its logic-outputs are typically at high impedance. In this state they are unable to drive the DE and signals to a defined logic level. During this period, noise, parasitic coupling or leakage from other devices could cause standard CMOS enable inputs to drift to an incorrect logic level.

If circuit boards are inserted into an energized backplane (commonly called "live insertion' or 'hot swap'), power may be suddenly applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

The SP308x family contains a special power-on-reset circuit that holds DE low and $\overline{RE}$ high for approximately 10 microseconds. After this initial power-up sequence, the hot-swap circuit becomes transparent, allowing for normal, unskewed enable and disable timings.

±15kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs of the SP308xE family have extra protection against static electricity. MaxLinear's uses state of the art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown and powered down. After an ESD event, the SP3082E - SP3088E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the SP3082E - SP3088E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2
- ±15kV Air-gap

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact MaxLinear for a reliability report that documents test setup, methodology and results.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The SP308xE family helps you design equipment to meet IEC 61000-4-2, without sacrificing board space and cost for external ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, as series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (1 unit load). A standard driver can drive up to 32 unit loads. The SP308xE family of transceivers has only a 1/8-unit load receiver input impedance (96kΩ), thereby allowing eight times as many,up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

Low Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown, devices typically draw only 50nA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part was not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ apply when the parts are shut down. It drivers and receivers take longer to become enabled from low-power shutdown mode $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver /receiver-disable mode (t_{ZH}, t_{ZL}).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

Line Length, EMI and Reflections

SP3082E - SP3085E feature controlled slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables.

SP3082E driver rise and fall times are limited to no faster than 667ns, allowing error-free data transmission up to 115kbps. The SP3083E, SP3084E and SP3085E offer somewhat higher driver output slew-rate limits, allowing transmit speeds up to 500kbps.

The RS-485 / RS422 standard covers line lengths up to 4,000ft. Maximum achievable line length is a function of signal attenuation and noise. Use of slew-controlled drivers such as the SP3082E - SP3085E may help to reduce crosstalk interference and permit communication over longer transmission lines.

Termination prevents reflections by eliminating the impedance mismatches on a transmission line. Line termination is typically used if rise and fall times are shorter than the round-trip signal propagation time. Slew-limited drivers may reduce or eliminate the need for cable termination in many applications.

Typical Applications

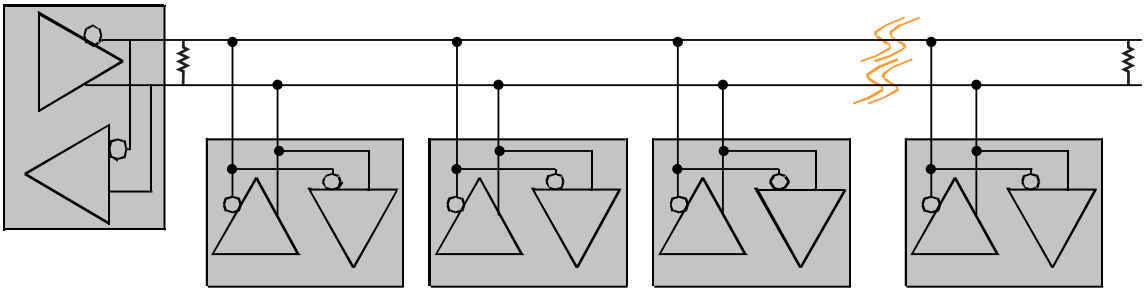


Figure 61: Half-Duplex Network

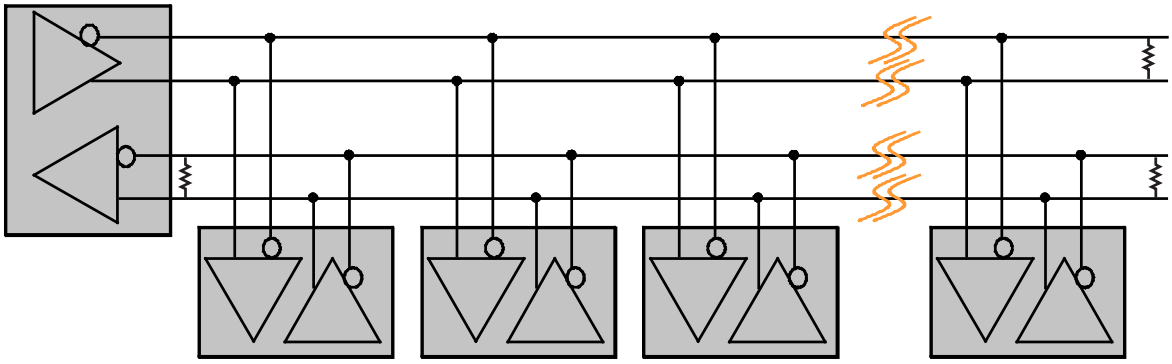


Figure 62: Bi-Directional Full-Duplex Network

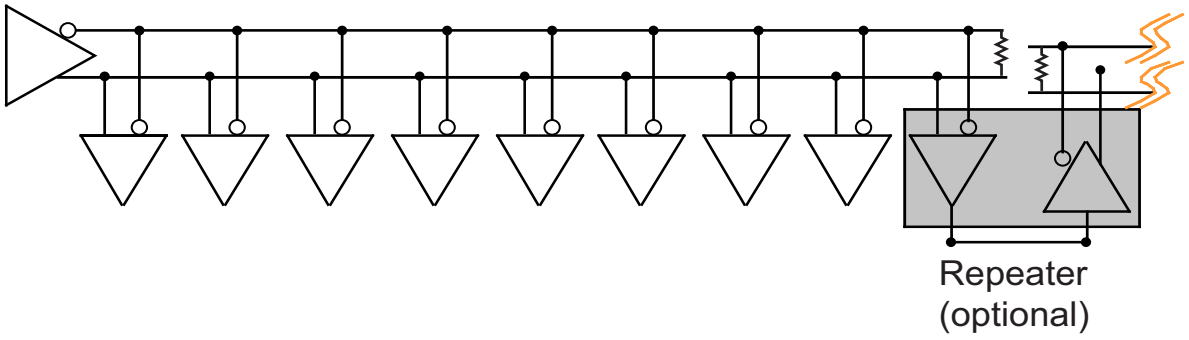
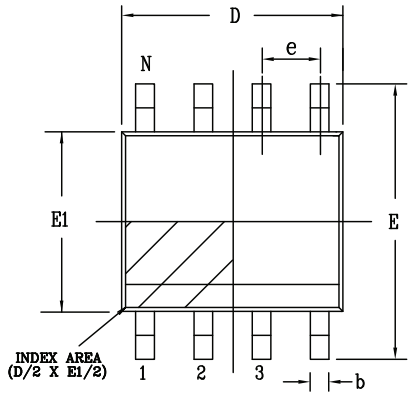
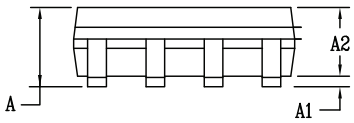


Figure 63: Point to Multi-Point Repeater

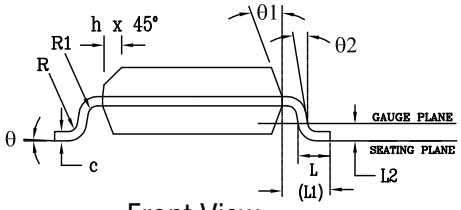
Mechanical Dimensions

NSOIC8





Side View



Front View

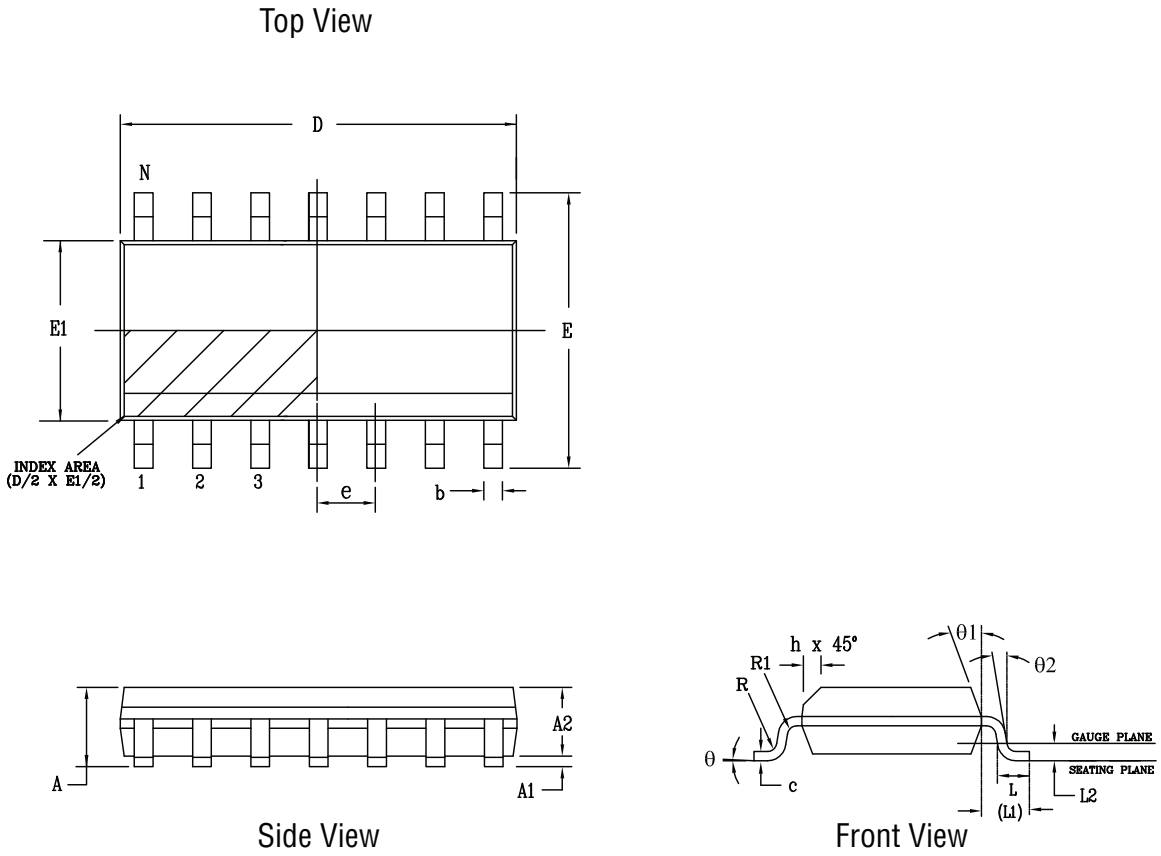
PACKAGE OUTLINE NSOIC .150" BODY JEDEC MS-012 VARIATION AA						
SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
q	0°	—	8°	0°	—	8°
q1	5°	—	15°	5°	—	15°
q2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8					

Drawing No: POD-00000108
Revision: A

Figure 64: Mechanical Dimension, NSOIC8

Mechanical Dimensions

NSOIC14



PACKAGE OUTLINE NSOIC .150" BODY JEDEC MS-012 VARIATION AB						
SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
q	0°	—	8°	0°	—	8°
q1	5°	—	15°	5°	—	15°
q2	0°	—	—	0°	—	—
D	8.65 BSC			0.341 BSC		
N	14					

Drawing No: POD-00000109
Revision: A

Figure 65: Mechanical Dimensions, NSOIC14

Ordering Information

SP3084E obsolete

Table 16: Ordering Information

Ordering Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
SP3082EEN-L	-40°C to 85°C	NSOIC8	Tube	Yes
SP3082EEN-L/TR	-40°C to 85°C	NSOIC8	Reel	Yes
SP3083EEN-L/TR	-40°C to 85°C	NSOIC14	Reel	Yes
SP3085EEN-L	-40°C to 85°C	NSOIC8	Tube	Yes
SP3085EEN-L/TR	-40°C to 85°C	NSOIC8	Reel	Yes
SP3088EEN-L	-40°C to 85°C	NSOIC8	Tube	Yes
SP3088EEN-L/TR	-40°C to 85°C	NSOIC8	Reel	Yes

Note: For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/SP3082E, www.maxlinear.com/SP3083E, www.maxlinear.com/SP3084E, www.maxlinear.com/SP3085E, and www.maxlinear.com/SP3088E.

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