GENERAL DESCRIPTION

The SP34063A is a monolithic switching regulator control circuit containing the primary functions required for DC-DC converters. This device consists of an internal temperature compensated reference, voltage comparator, controlled duty cycle oscillator with active current limit circuit, driver and high current output switch. This device was specifically designed to be used in buck, boost, and Voltage-Inverting applications with a minimum number of external components.

The SP34063A is available in the 8 pin NSOIC package.

APPLICATIONS

• Battery Charger Circuit
• NICs/Switches/Hubs
• ADSL Modems
• Negative Voltage Power Supply

FEATURES

• Supply Voltage: 3V - 36V
• Current Limiting
• Output Switch Current to 1.5A
• Adjustable Output Voltage
• Operation frequency up to 180KHz
• Low Quiescent Current
• Precision 2% Reference
• Available in 8 pin NSOIC Package

TYPICAL APPLICATION DIAGRAM

Fig. 1: SP34063A Application Diagram
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Power Supply Voltage $V_{CC}$ ........................................ 40V
Comparator Input Voltage .............................................. -0.3V to 40V
Switch Collector Voltage .............................................. 40V
Switch Emitter Voltage ($V_{PIN1}=40V$) ..................... 40V
Switch Collector to Emitter Voltage ............................. 40V
Driver Collector Voltage .............................................. 40V
Driver Collector Current (Note 2) .................................. 100mA
Switch Current ...................................................... 1.5A
Storage Temperature ............................................. -65°C to 150°C
ESD Rating (HBM - Human Body Model) ..................... 2kV

OPERATING RATINGS

Input Voltage Range $V_{IN}$ ........................................... 3.0V to 36V
Power Dissipation ($T_a=25^\circ C$ - NSOIC) ................. 780mW
Junction Temperature Range ..................................... -40°C to 150°C
Thermal Resistance $\theta_{JA}$ ........................................ 160°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Temperature of $T_a=25^\circ C$ only. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_a=25^\circ C$, and are provided for reference purposes only. Unless otherwise indicated, $V_{CC}=5.0V$, $T_a=\pm 40^\circ C$ to 85°C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Frequency $F_{OSC}$</td>
<td>30</td>
<td>38</td>
<td>45</td>
<td>KHz</td>
<td>$V_{PIN5}=0V$, $CT=1.0\mu F$, $T_a=25^\circ C$</td>
</tr>
<tr>
<td>Charge Current $I_{CHG}$</td>
<td>30</td>
<td>38</td>
<td>45</td>
<td>$\mu A$</td>
<td>$V_{CC}=5.0V$ to 36V, $T_a=25^\circ C$</td>
</tr>
<tr>
<td>Discharge Current $I_{DISCHG}$</td>
<td>180</td>
<td>240</td>
<td>290</td>
<td>$\mu A$</td>
<td>$V_{CC}=5.0V$ to 36V, $T_a=25^\circ C$</td>
</tr>
<tr>
<td>Discharge to Charge Current Ratio $I_{DISCHG}/I_{CHG}$</td>
<td>5.2</td>
<td>6.5</td>
<td>7.5</td>
<td></td>
<td>$Pin\ 7\ to\ V_{CC},\ T_a=25^\circ C$</td>
</tr>
<tr>
<td>Current Limit Sense Voltage $V_{IPK(sense)}$</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>mV</td>
<td>$I_{DISCHG}=I_{CHG},\ T_a=25^\circ C$</td>
</tr>
</tbody>
</table>

Output Switch (Note 1)

Saturation Voltage, Darlington Connection $V_{CE(sat)}$ | 1.0 | 1.3 | V | $I_{SW}=1A$, pin1,8 connected

Saturation Voltage (note 2) | 0.45 | 0.7 | V | $I_{SW}=1A$, R pin8=82ohms to $V_{CC}$, forced $\beta=20$

DC Current Gain | 50 | 75 | | $I_{SW}=1A$, $V_{CE}=5V$, $T_a=25^\circ C$

Collector Off-State Current | 0.01 | 100 | $\mu A$ | $V_{CE}=36V$

Comparator

Threshold Voltage $V_{TH}$ | 1.225 | 1.250 | 1.275 | V | $T_a=25^\circ C$

| | 1.210 | 1.250 | 1.290 | V | $T_a=-40^\circ C$ to 85°C |

Threshold Voltage Line Regulation $R_{EGLINE}$ | 1.4 | 5 | mV | $V_{CC}=3.0V$ to 36V |

Input Bias Current $I_{IB}$ | -20 | -400 | nA | $V_{TH}=0V$

Total Device

Supply Current $I_{CC}$ | 4 | mA | | $V_{CC}=5.0V$ to 36V, $CT=1nF$, $pin\ 7\ =\ V_{CC}$ $V_{pin5}>V_{TH}$ |

Note 1: Low duty cycle pulse techniques are used during the test program to maintain junction temperature as close to ambient temperature as possible.

Note 2: If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300mA$) and high driver currents ($\geq 30mA$), it may take up to 2.0μs for it to come out of saturation. This condition will shorten the
off time at frequencies above 30KHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

\[
\text{Forced } \beta \text{ of output switch } = \frac{I_{c,\text{Output}}}{I_{c,\text{Driver}} - 7 \text{mA}} \geq 10
\]

* The 100Ω resistor in the emitter of the driver device requires about 7.0mA before the output switch conducts.

**BLOCK DIAGRAM**

![Block Diagram](image)

Fig. 2: SP34063A Block Diagram

**PIN ASSIGNEMENT**

![Pin Assignment](image)

Fig. 3: SP34063A Pin Assignment
**PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch Collector</td>
<td>1</td>
<td>Internal switch transistor collector</td>
</tr>
<tr>
<td>Switch Emitter</td>
<td>2</td>
<td>Internal switch transistor emitter</td>
</tr>
<tr>
<td>Timing Capacitor</td>
<td>3</td>
<td>Timing capacitor to control the switching frequency</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>Ground pin for all internal circuit</td>
</tr>
<tr>
<td>Comparator Inverting Input</td>
<td>5</td>
<td>Inverting input pin for internal comparator</td>
</tr>
<tr>
<td>Vcc</td>
<td>6</td>
<td>Voltage supply</td>
</tr>
<tr>
<td>Ipk Sense</td>
<td>7</td>
<td>Peak Current Sense Input by monitoring the voltage drop across an external I sense resistor to limit the peak current through the switch</td>
</tr>
<tr>
<td>Driver Collector</td>
<td>8</td>
<td>Voltage driver collector</td>
</tr>
</tbody>
</table>

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Packing Quantity</th>
<th>Note 1</th>
<th>Note 2</th>
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<tr>
<td>SP34063AEN-L</td>
<td>-40°C≤T,≤+85°C</td>
<td>NSOIC-8</td>
<td>Bulk</td>
<td>Lead Free</td>
<td></td>
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<tr>
<td>SP34063AEN-L/TR</td>
<td>-40°C≤T,≤+85°C</td>
<td>NSOIC-8</td>
<td>2.5K/Tape &amp; Reel</td>
<td>Lead Free</td>
<td></td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 4: Output Switch On-Off Time vs. Oscillator Timing Capacitor

Fig. 5: Timing Capacitor Waveform

Fig. 6: Oscillator Frequency vs. Timing Capacitor

Fig. 7: Standard Supply Current vs. Supply Voltage

Fig. 8: Emitter Follower Configuration Output Switch Saturation vs. Emitter Current

Fig. 9: Common Emitter Configuration Output Switch Saturation vs. Collector Current
APPLICATION INFORMATION

**Typical Boost Converter Circuit**

This is a typical boost converter configuration. In the steady state, if the resistor divider voltage at pin 5 is greater than the voltage in the non-inverting input, which is 1.25V determined by the internal reference, the output of the comparator will go low. At the next switching period, the output switch will not conduct and the output voltage will eventually drop below its nominal voltage until the divider voltage at pin 5 is lower than 1.25. Then the output of the comparator will go high, the output switch will be allowed to conduct. Since $V_{PINS} = V_{OUT} \times R2/(R1+R2) = 1.25(\text{V})$, the output voltage can be decided by $V_{OUT} = 1.25V\times(R1+R2)/R2(\text{V})$. 

Fig. 10: Current Limit Sense Voltage vs. Temperature
This is a typical buck converter configuration. The working process in the steady state is similar to a boost converter, $V_{PINS} = V_{OUT} \cdot R2/(R1+R2) = 1.25(V)$. The output voltage can be decided by $V_{OUT} = 1.25V \cdot (R1+R2)/R2(V)$.

**Typical Inverting Converter Circuit**

This is a typical boost converter configuration. The working process in the steady state is similar to a boost converter, the difference in this situation is that the voltage at the non-inverting pin of the comparator is equal to $1.25V + V_{OUT}$, then $V_{PINS} = V_{OUT} \cdot R2/(R1+R2) = 1.25V, + V_{OUT}$. The output voltage can be decided by $V_{OUT} = -1.25V \cdot (R1+R2)/R1 (V)$.
PACKAGE SPECIFICATION

8-Pin NSOIC

Unit: mm (inch)
REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>2.0.0</td>
<td>01/16/2009</td>
<td>Reformat of Datasheet</td>
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<tr>
<td>2.0.1</td>
<td>08/24/2010</td>
<td>Pg1, changed operation frequency from 110kHz to 180kHz Fig. 6: Changed title to: Oscillator Frequency vs. Timing Capacitor Pg7, Corrected the inverting converter circuit</td>
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<tr>
<td>2.1.0</td>
<td>02/14/2011</td>
<td>Corrected Power Dissipation value to 780mW under Operating Ratings Added C1=f(Ton) formula on figure 10 graph Updated package specification</td>
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<tr>
<td>2.1.1</td>
<td>02/06/2014</td>
<td>Updated figure 4 and 6 [ECN 1407-07]</td>
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FOR FURTHER ASSISTANCE

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