GENERAL DESCRIPTION

The ST16C2450 (2450) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2450 is an improved version of the ST16C2450 with lower operating voltage and 5 volt tolerant inputs. The 2450 provides enhanced UART functions, a modem control interface and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. Independent programmable baud rate generators are provided to select transmit and receive clock rates up to 1.5 Mbps. An internal loopback capability allows onboard diagnostics. The 2450 is available in a 44-pin PLCC and 48-pin TQFP packages. The 2450 is fabricated in an advanced CMOS process capable of operating from 2.97 volt to 5.5 volt power supply. The devices with a top marking of "A2 YYWW" or newer have 5 volt tolerant inputs.

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

Added feature in devices with top marking "A2 YYWW" and newer:

- 5 Volt Tolerant Inputs

- 2.97 to 5.5 Volt Operation
- Pin-to-pin compatible to Exar's XR16C2450, ST16C2550, XR16L2550, XR16L2750 and XR16C2850
- 2 independent UART channels
  - Up to 1.5 Mbps data rate with a 24 MHz crystal oscillator or external clock frequency
  - 1 byte Transmit FIFO
  - 1 byte Receive FIFO with error tags
  - Status report registers
  - Modem control signals (CTS#, RTS#, DSR#, DTR#, RI#, CD#)
  - Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Crystal oscillator or external clock input
- TTL compatible inputs, outputs
- Industrial temperature ranges
- 48-TQFP and 44-PLCC packages

the product (or products) mentioned in this
data sheet are no longer being manufactured
and may not be ordered (ORs)

FIGURE 1. ST16C2450 BLOCK DIAGRAM

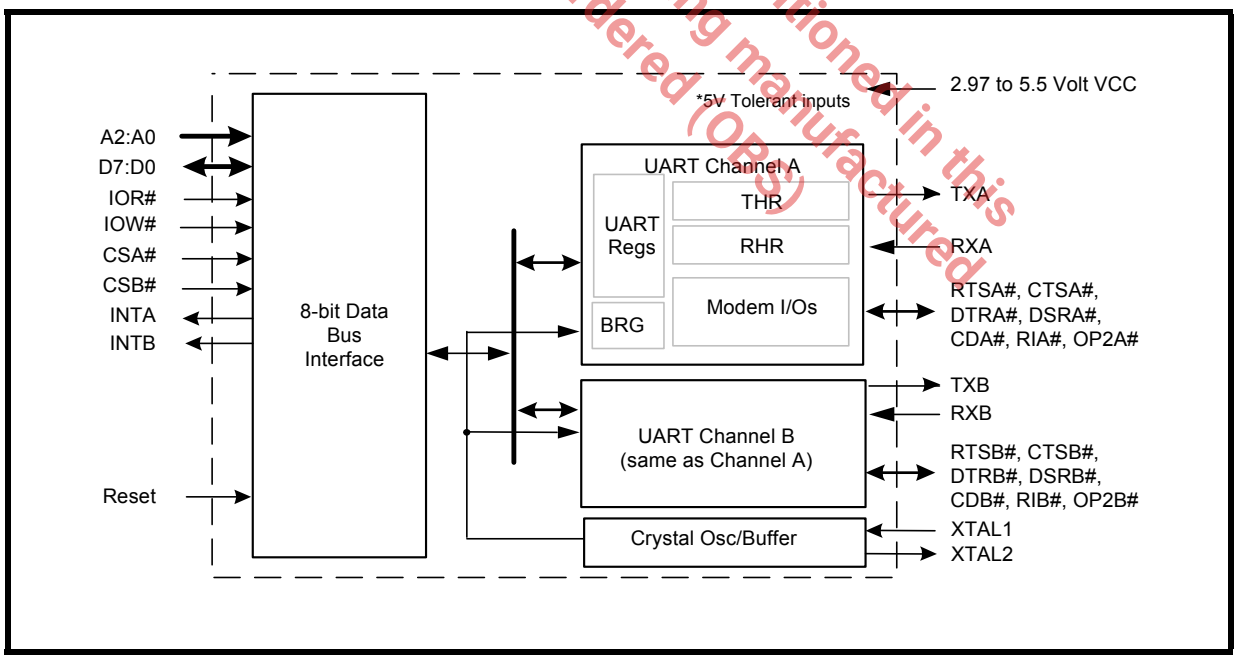
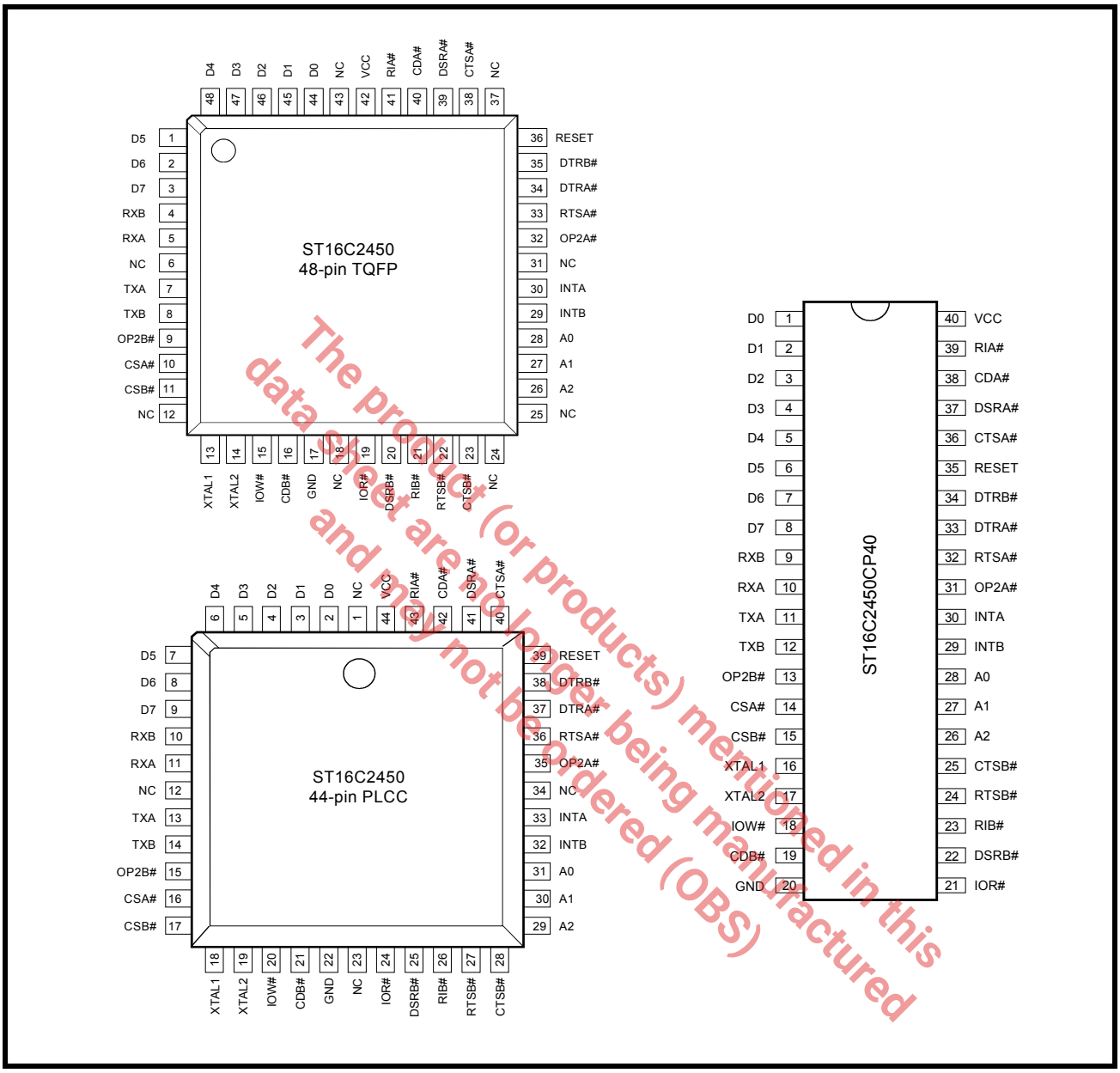


FIGURE 2. PIN OUT ASSIGNMENT



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
ST16C2450CP40	40-Lead PDIP	0°C to +70°C	Active. See the ST16C2450CQ48 for new designs.
ST16C2450CJ44	44-Lead PLCC	0°C to +70°C	Active
ST16C2450CQ48	48-Lead TQFP	0°C to +70°C	Active
ST16C2450IP40	40-Lead PDIP	-40°C to +85°C	Active. See the ST16C2450IQ48 for new designs.
ST16C2450IJ44	44-Lead PLCC	-40°C to +85°C	Active
ST16C2450IQ48	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE				
A2 A1 A0	29 30 31	26 27 28	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	9 8 7 6 5 4 3 2	3 2 1 48 47 46 45 44	IO	Data bus lines [7:0] (bidirectional).
IOR#	24	19	I	Input/Output Read Strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed to by the address lines [A2:A0]. The data byte is placed on the data bus to allow the host processor to read it on the rising edge.
IOW#	20	15	I	Input/Output Write Strobe (active low). The falling edge instigates an internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines.
CSA#	16	10	I	UART channel A select (active low) to enable UART channel A in the device for data bus operation.
CSB#	17	11	I	UART channel B select (active low) to enable UART channel B in the device for data bus operation.
INTA	33	30	O	UART channel A Interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output to a logic 0 when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# to a logic 1 when MCR[3] is set to a logic 0 (default).
INTB	32	29	O	UART channel B Interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTB is set to the active mode and OP2B# output to a logic 0 when MCR[3] is set to a logic 1. INTB is set to the three state mode and OP2B# to a logic 1 when MCR[3] is set to a logic 0 (default).
MODEM OR SERIAL I/O INTERFACE				
TXA	13	7	O	UART channel A Transmit Data. If it is not used, leave it unconnected.
RXA	11	5	I	UART channel A Receive Data. Normal receive data input must idle at logic 1 condition. If it is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSA#	36	33	O	UART channel A Request-to-Send (active low) or general purpose output. If it is not used, leave it unconnected.
CTSA#	40	38	I	UART channel A Clear-to-Send (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.

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Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
DTRA#	37	34	O	UART channel A Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRA#	41	39	I	UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDA#	42	40	I	UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIA#	43	41	I	UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
OP2A#	35	32	O	Output Port 2 Channel A - The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output to a logic 0 when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# to a logic 1 when MCR[3] is set to a logic 0. This output should not be used as a general output else it will disturb the INTA output functionality. If it is not used at all, leave it unconnected.
TXB	14	8	O	UART channel B Transmit Data. If it is not used, leave it unconnected.
RXB	10	4	I	UART channel B Receive Data. Normal receive data input must idle at logic 1 condition. If it is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSB#	27	22	O	UART channel B Request-to-Send (active low) or general purpose output. If it is not used, leave it unconnected.
CTSB#	28	23	I	UART channel B Clear-to-Send (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
DTRB#	38	35	O	UART channel B Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRB#	25	20	I	UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDB#	21	16	I	UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIB#	26	21	I	UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
OP2B#	15	9	O	Output Port 2 Channel B - The output state is defined by the user and through the software setting of MCR[3]. INTB is set to the active mode and OP2B# output to a logic 0 when MCR[3] is set to a logic 1. INTB is set to the three state mode and OP2B# to a logic 1 when MCR[3] is set to a logic 0. This output should not be used as a general output else it will disturb the INTB output functionality. If it is not used, leave it unconnected.

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Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
ANCILLARY SIGNALS				
XTAL1	18	13	I	Crystal or external clock input.
XTAL2	19	14	O	Crystal or buffered clock output.
RESET	39	36	I	Reset (active high) - A longer than 40 ns logic 1 pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period.
VCC	44	42	Pwr	2.97V to 5.5V power supply. All inputs are 5V tolerant for devices with top marking of "A2 YYWW" and newer.
GND	22	17	Pwr	Power supply common, ground.
N.C.	1, 12, 23, 34	6, 12, 18, 24, 25, 31, 37, 43	-	No Connection. These pins are open, but typically, should be connected to GND for good design practice.

Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be offered (OPS)

1.0 PRODUCT DESCRIPTION

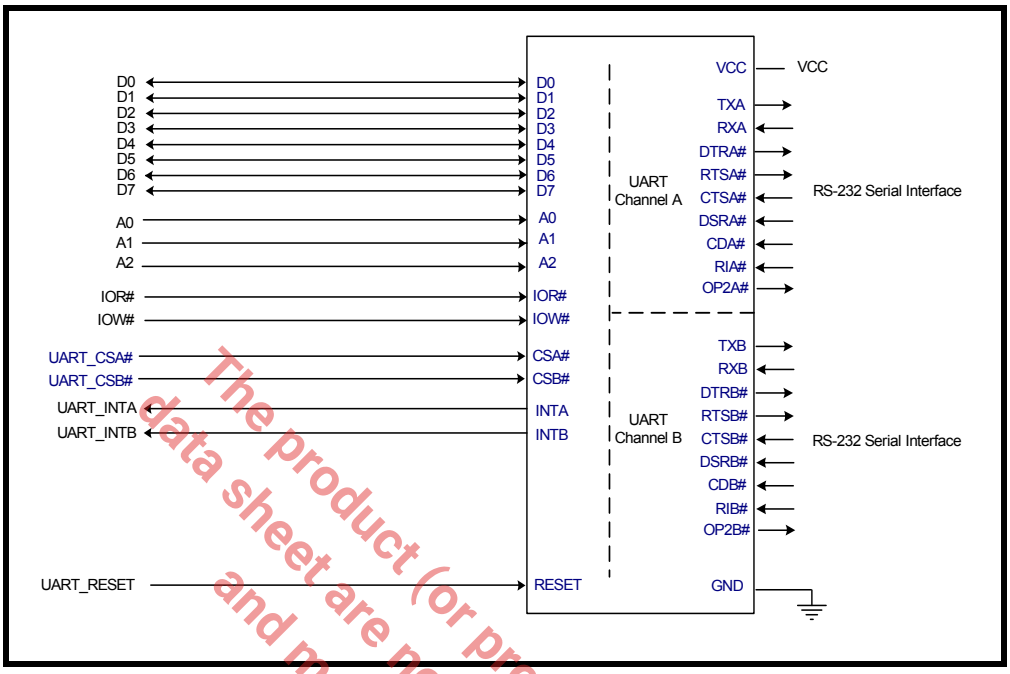
The ST16C2450 (2450) integrates the functions of two 16C450 Universal Asynchrounous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The 2450 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 2450 represents such an integration with greatly enhanced features. The 2450 is fabricated with an advanced CMOS process. The 2450 is capable of operation up to 1.5 Mbps with a 24 MHz clock. With a crystal or external clock input of 14.7456 MHz the user can select data rates up to 921.6 Kbps.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 2450 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C450 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 3.

FIGURE 3. ST16C2450 DATA BUS INTERCONNECTIONS



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 8). An active high pulse of at least 40 ns duration will be required to activate the reset function in the device.

2.3 Channel A and B Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on chip select pins, CSA# or CSB#, allows the user to select UART channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Selecting both UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from both uarts simultaneously. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT

CSA#	CSB#	FUNCTION
1	1	UART de-selected
0	1	Channel A selected
1	0	Channel B selected
0	0	Channel A and B selected

2.4 Channel A and B Internal Registers

Each UART channel in the 2450 has a standard register set for controlling, monitoring and data loading and unloading. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scratch pad register (SPR).

2.5 INTA and INTB Outputs

The INTA and INTB interrupt output changes according to the operating mode and enhanced features setup. Table 2 summarizes the operating behavior for the transmitter and receiver. Also see Figure 12 and Figure 13.

TABLE 2: INTA AND INTB PINS OPERATION FOR TRANSMITTER

	TRANSMITTER	RECEIVER
INTA/B Pin	0 = a byte in THR 1 = THR empty	0 = no data 1 = 1 byte

2.6 Crystal Oscillator or External Clock Input

The 2450 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. See "Programmable Baud Rate Generator" on page 8.

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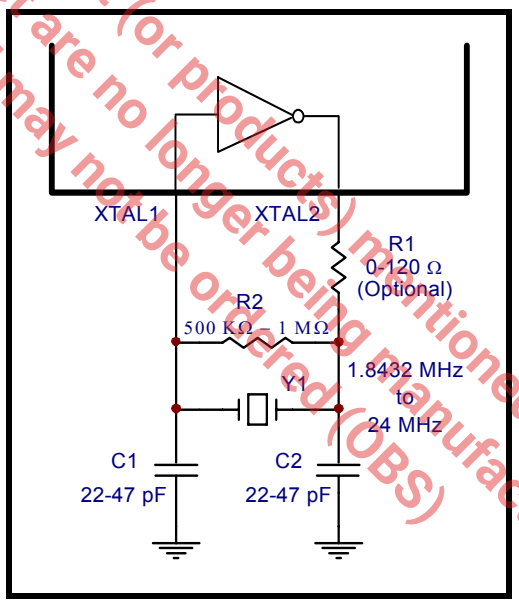
FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 4), with an external 500 kΩ to 1 MΩ resistor across it. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typical oscillator connections are shown in Figure 4. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.7 Programmable Baud Rate Generator

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of operating with a crystal frequency or external clock of up to 24 MHz.

The 2450 divides the basic external clock by 16. The basic 16X clock provides table rates to support standard and custom applications using the same system design. The Baud Rate Generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Table 3 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate. When using a non-standard frequency crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency) / (serial data rate x 16)

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TABLE 3: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

Output Data Rate MCR Bit-7=0	Divisor for 16x Clock (Decimal)	Divisor for 16x Clock (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)	Data Rate Error (%)
400	2304	900	09	00	0
2400	384	180	01	80	0
4800	192	C0	00	C0	0
9600	96	60	00	60	0
19.2k	48	30	00	30	0
38.4k	24	18	00	18	0
76.8k	12	0C	00	0C	0
153.6k	6	06	00	06	0
230.4k	4	04	00	04	0
460.8k	2	02	00	02	0
921.6k	1	01	00	01	0

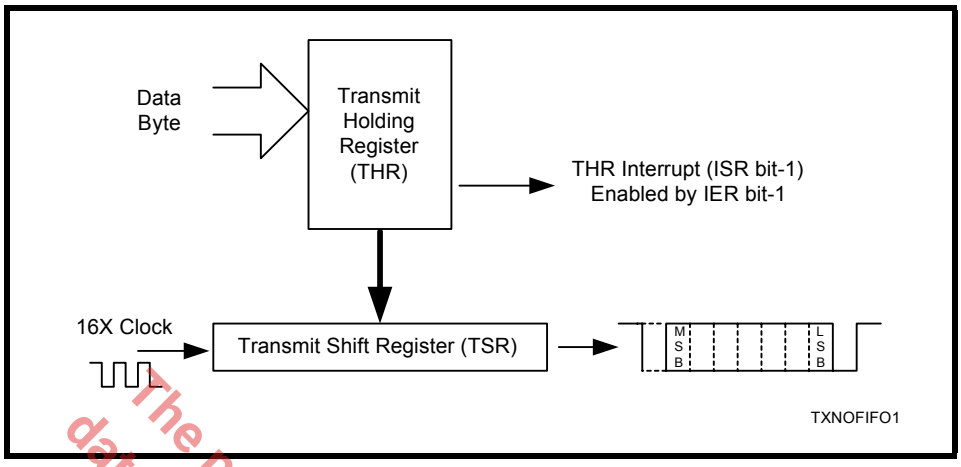
2.8 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 1 byte FIFO or Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

2.8.1 Transmit Holding Register (THR) - Write Only

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 5. TRANSMITTER OPERATION



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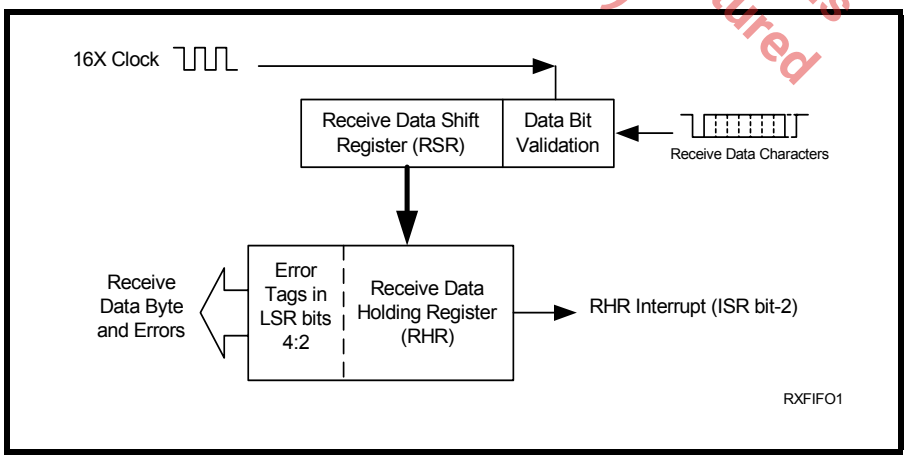
2.9 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 1 byte FIFO or Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Once the data is received, the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR will generate a receive data ready interrupt upon receiving a character if IER bit-0 has been enabled.

2.9.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the 1 byte receive FIFO that is 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. After the RHR is read, LSR bits 2-4 willl immediately be updated to reflect the errors for the next character byte transferred from the RSR.

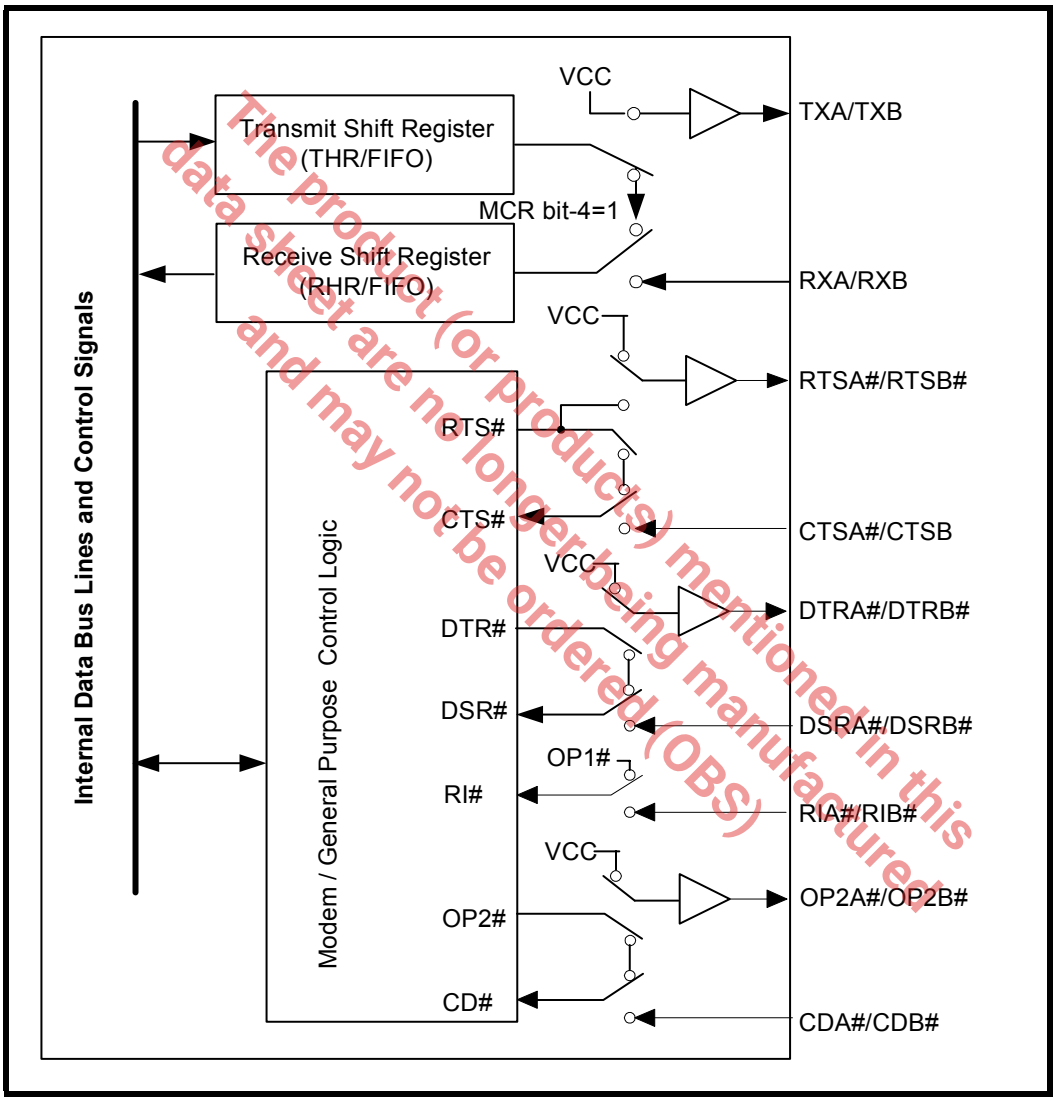
FIGURE 6. RECEIVER OPERATION



2.10 Internal Loopback

The 2450 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 7 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 7. INTERNAL LOOP BACK IN CHANNELS A AND B



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

3.0 UART INTERNAL REGISTERS

Each of the UART channel in the 2450 has its own set of configuration registers selected by address lines A0, A1 and A2 with CSA# or CSB# selecting the channel. The registers are 16C450 compatible. The complete register set is shown on Table 4 and Table 5.

TABLE 4: UART CHANNEL A AND B UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1
0 0 1	DLM - Div Latch High Byte	Read/Write	LCR[7] = 1
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register Reserved	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

.

TABLE 5: INTERNAL REGISTERS DESCRIPTION

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C450 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0	0	0	0	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	LCR[7] = 0
0 1 0	ISR	RD	0	0	0	0	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0	0	0	Internal Loop-back Enable	OP2#/ INT Output Enable	Rsrvd (OP1#)	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	0	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

See “Receiver” on page 9.

4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 8.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 Interrupt Mode Operation

When the receive interrupt (IER BIT-0 = 1) is enabled, the RHR interrupt (see ISR bit-2) status will reflect the following:

A. The receive data available interrupts are issued to the host when there is a character in the RHR. It will be cleared when the character has been read out of the RHR.

B. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the RHR is empty.

4.3.2 Polled Mode Operation

Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in the RHR.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the RHR may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the THR and TSR are empty.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the Transmit FIFO becomes empty. If the Transmit FIFO is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[7:4]: Reserved

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 6, shows the data values (bits 0-3) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by data byte received in RHR.
- TXRDY is by THR empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data out of RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.

TABLE 6: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS				SOURCE OF INTERRUPT
	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	0	TXRDY (Transmit Ready)
4	0	0	0	0	MSR (Modem Status Register)
-	0	0	0	1	None (default)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Table 6).

ISR[7:4]: Reserved

4.5 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 7 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR[5] = logic 0, parity is not forced (default).
- LCR[5] = logic 1 and LCR[4] = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR[5] = logic 1 and LCR[4] = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

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TABLE 7: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors (DLL/DLM) Enable

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.6 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Output

The RTS# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: Reserved

OP1# is not available as an output pin on the 2450. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: OP2# Output / INT Output Enable

This bit enables and disables the operation of INT interrupt output. If INT output is not used, OP2# can be used as a general purpose output.

- Logic 0 = INT (A-B) outputs disabled (three state mode) and OP2# output set to a logic 1 (default).
- Logic 1 = INT (A-B) outputs enabled (active mode) and OP2# output set to a logic 0.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 7.

MCR[7:5]: Reserved

4.7 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register .

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while there is data in the RHR. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the RHR, therefore the data in the RHR is not corrupted by the error. An interrupt will be generated immediately if LSR interrupt is enabled (IER bit-2).

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LSR[2]: Receive Data Parity Error Flag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR. If the LSR interrupt is enabled (IER bit-2), an interrupt will be generated when the character is in the RHR.

LSR[3]: Receive Data Framing Error Flag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR. If the LSR interrupt is enabled (IER bit-2), an interrupt will be generated when the character is in the RHR.

LSR[4]: Receive Break Flag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). The break indication remains until the RX input returns to the idle condition, “mark” or logic 1. If the LSR interrupt is enabled (IER bit-2), an interrupt will be generated when the character is in the RHR.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character.

LSR[7]: Reserved

4.8 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

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MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

Normally this bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.9 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.10 Baud Rate Generator Registers (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to '1'. See "Programmable Baud Rate Generator" on page 8. for more details.

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TABLE 8: UART RESET CONDITIONS FOR CHANNEL A AND B

REGISTERS	RESET STATE
DLM	Bits 7-0 = 0xXX
DLL	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
I/O SIGNALS	**RESET STATE**
TX	Logic 1
OP2#	Logic 1
RTS#	Logic 1
DTR#	Logic 1
INT	Three-State Condition

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (48-TQFP)	theta-ja =59°C/W, theta-jc = 16°C/W
Thermal Resistance (44-PLCC)	theta-ja = 50°C/W, theta-jc = 21°C/W
Thermal Resistance (40-PDIP)	theta-ja = 50°C/W, theta-jc = 22°C/W

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ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: 0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V

SYMBOL	PARAMETER	TOP MARKING "A2 YYWW" AND NEWER								UNITS	CONDITIONS
		LIMITS 3.3V		LIMITS 5.0V		LIMITS 3.3V		LIMITS 5.0V			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{ILCK}	Clock Input Low Level	-0.3	0.6	-0.5	0.6	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock Input High Level	2.4	VCC	3.0	VCC	2.4	5.5	3.0	5.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.5	0.8	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	VCC	2.2	VCC	2.0	5.5	2.2	5.5	V	
V_{OL}	Output Low Voltage		0.4		0.4		0.4		0.4	V V	I_{OL} = 6 mA I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.0		2.4		2.0		2.4		V V	I_{OH} = -6 mA I_{OH} = -1 mA
I_{IL}	Input Low Leakage Current		±10		±10		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5		5		5	pF	
I_{CC}	Power Supply Current		1.3		3		1.3		3	mA	

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: 0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3		LIMITS 5.0		UNIT
		MIN	MAX	MIN	MAX	
-	Crystal Frequency		16		24	MHz
CLK	External Clock Low/High Time	25		21		ns
OSC	External Clock Frequency		20		24	MHz
T_{AS}	Address Setup Time	5		0		ns
T_{AH}	Address Hold Time	10		5		ns
T_{CS}	Chip Select Width	66		50		ns
T_{RD}	IOR# Strobe Width	35		25		ns
T_{DY}	Read Cycle Delay	40		30		ns
T_{RDV}	Data Access Time		35		25	ns
T_{DD}	Data Disable Time	0	25	0	15	ns
T_{WR}	IOW# Strobe Width	40		25		ns
T_{DY}	Write Cycle Delay	40		30		ns
T_{DS}	Data Setup Time	20		15		ns
T_{DH}	Data Hold Time	5		5		ns
T_{WDO}	Delay From IOW# To Output		50		40	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		40		35	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		40		35	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		40	ns
T_{RST}	Reset Pulse Width	40		40		ns
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-
Bclk	Baud Clock	16X of data rate				Hz

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FIGURE 8. CLOCK TIMING

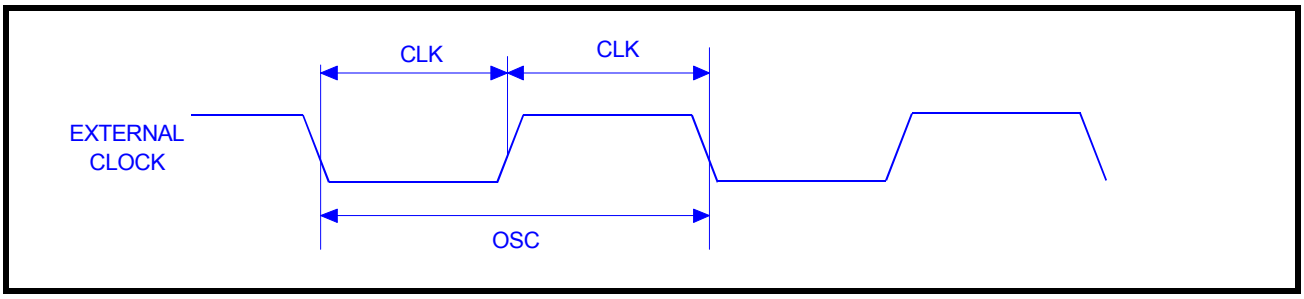

FIGURE 9. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B

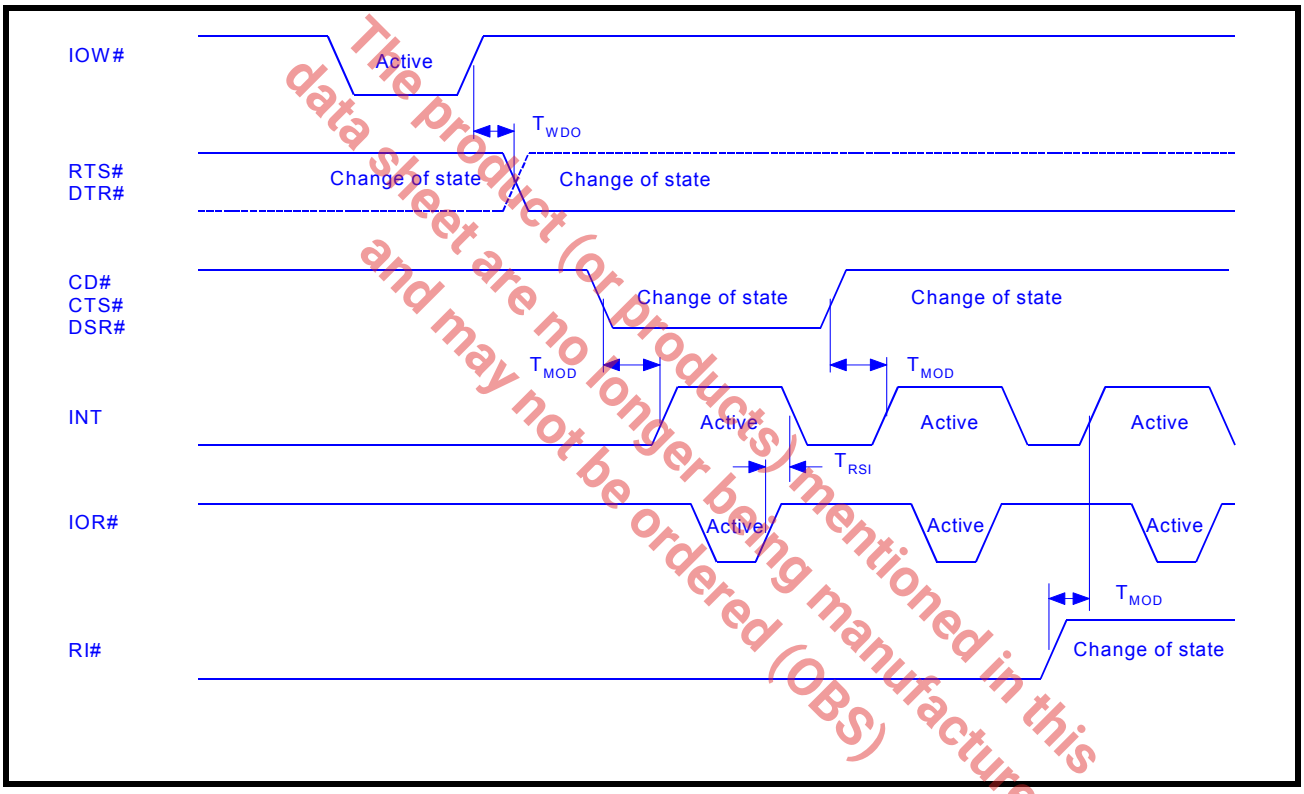

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FIGURE 10. DATA BUS READ TIMING

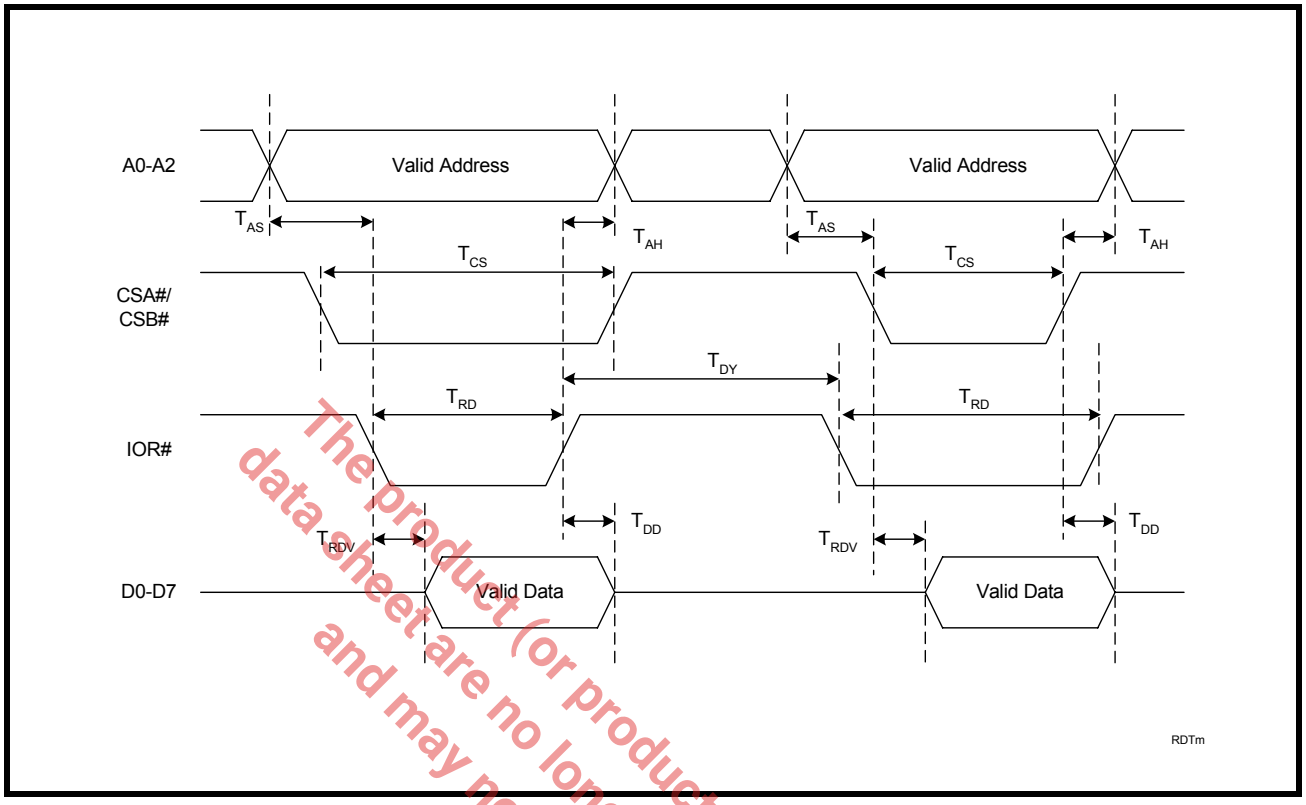

FIGURE 11. DATA BUS WRITE TIMING

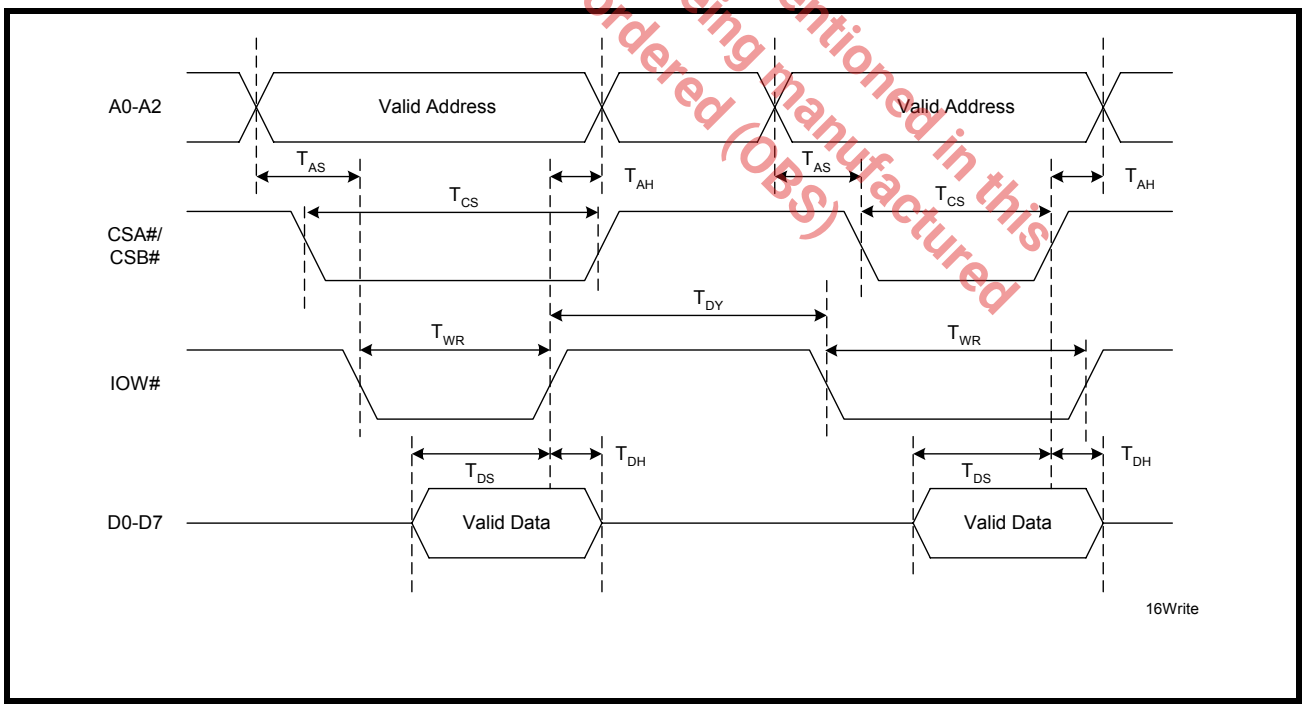

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FIGURE 12. INTERRUPT TIMING FOR CHANNELS A & B

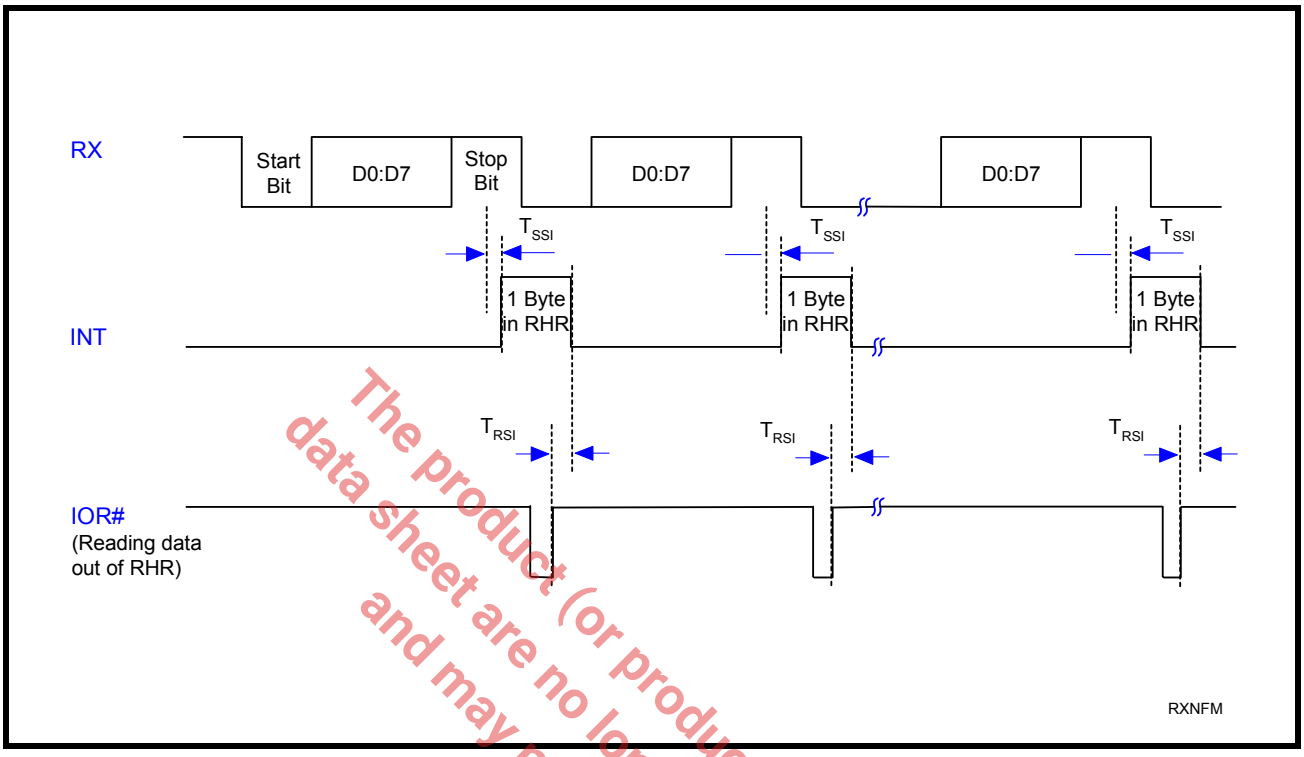

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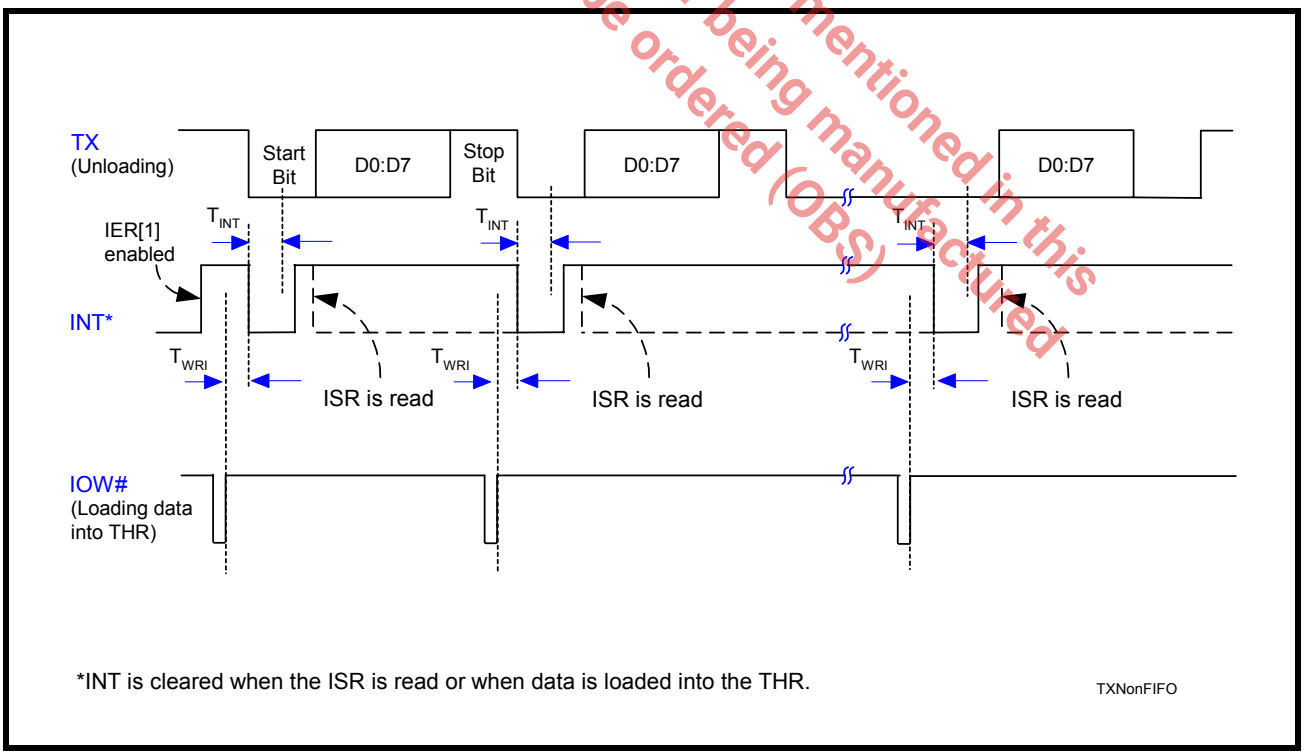
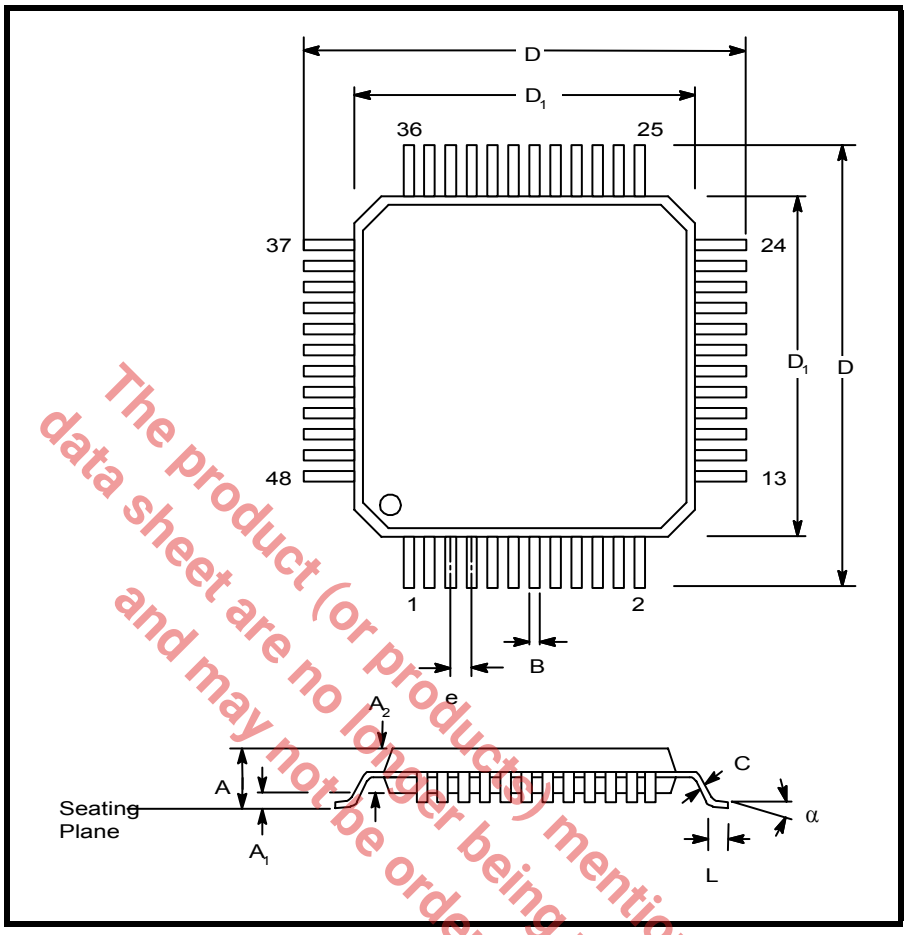
FIGURE 13. INTERRUPT TIMING FOR CHANNELS A & B



PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1 mm)

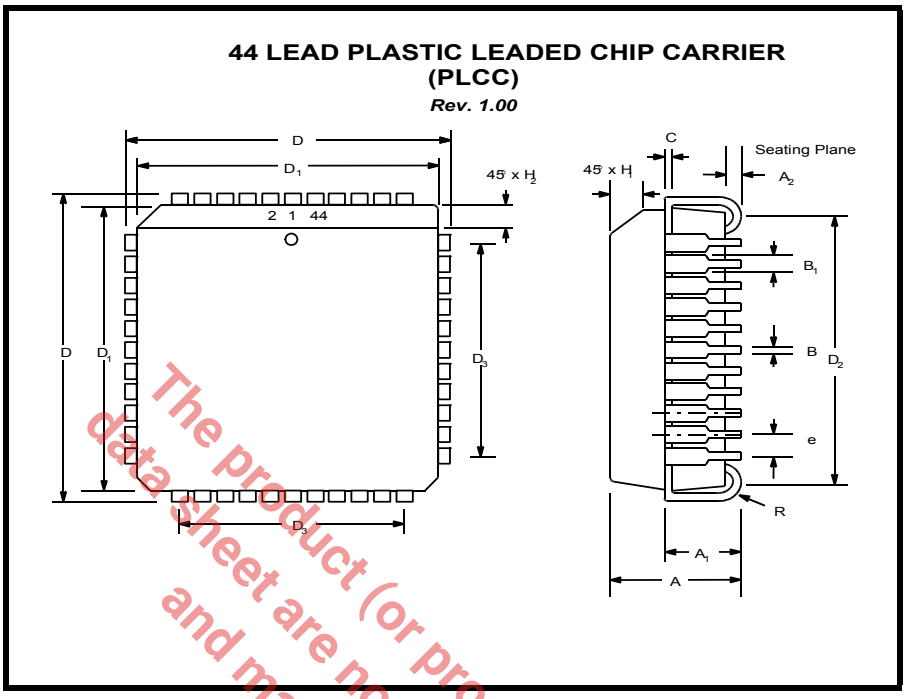


The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A1	0.002	0.006	0.05	0.15
A2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

PACKAGE DIMENSIONS (44 PIN PLCC)



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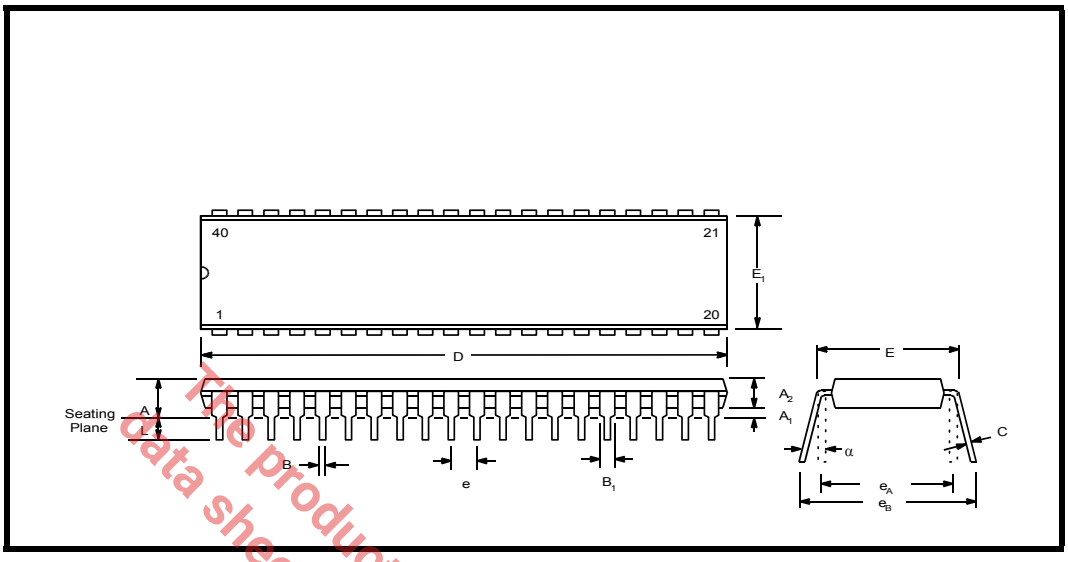
Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

PACKAGE DIMENSIONS (40 PIN PDIP)



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A1	0.015	0.070	0.38	1.78
A2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.98	2.095	50.29	53.21
E	0.600	0.625	15.24	15.88
E1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

REVISION HISTORY

DATE	REVISION	DESCRIPTION
September 2003	4.0.0	Changed to standard style, single-column format. Clarified timing diagrams. Added Device Status to Ordering Information. Devices with top markings of "A2 YYWW" and newer have 5V tolerant inputs. Devices with top markings of "CC YYWW" and older do not have 5V tolerant inputs.
May 2005	4.0.1	Corrected block diagram on page 1.

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