FEATURES

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HCMOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range (+1% to 80%)
- Excellent Temp. Stability, 100 ppm/°C, typ.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

GENERAL DESCRIPTION

The XR-2211A is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211A is available in 14 pin packages specified for commercial temperature ranges.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Package</th>
<th>Operating Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>XR-2211ACP</td>
<td>14 Lead PDIP (0.300&quot;)</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>XR-2211ACD</td>
<td>14 Lead SOIC (Jedec, 0.150&quot;)</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>
Figure 1. XR-2211A Block Diagram
PIN CONFIGURATION

14 Lead PDIP (0.300”)  

14 Lead SOIC (Jedec, 0.150”)  

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_CC</td>
<td></td>
<td>Positive Power Supply.</td>
</tr>
<tr>
<td>2</td>
<td>INP</td>
<td>I</td>
<td>Receive Analog Input.</td>
</tr>
<tr>
<td>3</td>
<td>LDF</td>
<td>O</td>
<td>Lock Detect Filter.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td></td>
<td>Ground Pin.</td>
</tr>
<tr>
<td>5</td>
<td>LDOQN</td>
<td>O</td>
<td>Lock Detect Output Not. This output will be low if the VCO is in the capture range.</td>
</tr>
<tr>
<td>6</td>
<td>LDOQ</td>
<td>O</td>
<td>Lock Detect Output. This output will be high if the VCO is in the capture range.</td>
</tr>
<tr>
<td>7</td>
<td>DO</td>
<td>O</td>
<td>Data Output. Decoded FSK output.</td>
</tr>
<tr>
<td>8</td>
<td>COMP I</td>
<td>I</td>
<td>FSK Comparator Input.</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td>Not Connected.</td>
</tr>
<tr>
<td>10</td>
<td>V_REF</td>
<td>O</td>
<td>Internal Voltage Reference. The value of V_REF is V_CC /2 - 650mV.</td>
</tr>
<tr>
<td>11</td>
<td>LDO</td>
<td>O</td>
<td>Loop Detect Output. This output provides the result of the quadrature phase detection.</td>
</tr>
<tr>
<td>12</td>
<td>TIM R</td>
<td>I</td>
<td>Timing Resistor Input. This pin connects to the timing resistor of the VCO.</td>
</tr>
<tr>
<td>13</td>
<td>TIM C2</td>
<td>I</td>
<td>Timing Capacitor Input. The timing capacitor connects between this pin and pin 14.</td>
</tr>
<tr>
<td>14</td>
<td>TIM C1</td>
<td>I</td>
<td>Timing Capacitor Input. The timing capacitor connects between this pin and pin 13.</td>
</tr>
</tbody>
</table>
## PDC ELECTRICAL CHARACTERISTICS

**Test Conditions:** \( V_{CC} = 12V, T_A = +25^\circ C, R_O = 30K\Omega, C_O = 0.033\mu F \), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>4.5</td>
<td>20</td>
<td></td>
<td>V</td>
<td>( R_0 \geq 10K\Omega ). See Figure 4.</td>
</tr>
<tr>
<td>Supply Current</td>
<td>5</td>
<td>9</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>Oscillator Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency Accuracy</td>
<td>( \pm 3% )</td>
<td>%</td>
<td>Deviation from ( f_O = 1/R_0 C_0 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency Stability</td>
<td>( \pm 100 \text{ ppm}/^\circ C )</td>
<td></td>
<td>See Figure 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td>( \pm 100 \text{ ppm}/^\circ C )</td>
<td></td>
<td>See Figure 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply</td>
<td>0.25</td>
<td>%/V</td>
<td>( V_{CC} = 12 \pm 1V ). See Figure 7.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Upper Frequency Limit</td>
<td>300</td>
<td>kHz</td>
<td></td>
<td>( R_0 = 8.2K\Omega, C_0 = 400pF )</td>
<td></td>
</tr>
<tr>
<td>Lowest Practical</td>
<td>0.01</td>
<td>Hz</td>
<td></td>
<td>( R_0 = 2M\Omega, C_0 = 50\mu F )</td>
<td></td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>5</td>
<td>2000</td>
<td>K\Omega</td>
<td>See Figure 7 and Figure 8.</td>
<td></td>
</tr>
<tr>
<td>Timing Resistor, ( R_O ) - See Figure 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td>5</td>
<td>2000</td>
<td>K\Omega</td>
<td>See Figure 7 and Figure 8.</td>
<td></td>
</tr>
<tr>
<td>Recommended Range</td>
<td>5</td>
<td>100</td>
<td>K\Omega</td>
<td>See Figure 7 and Figure 8.</td>
<td></td>
</tr>
<tr>
<td><strong>Loop Phase Detector Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>( \pm 100 )</td>
<td>( \pm 200 )</td>
<td>( \pm 300 )</td>
<td>( \mu A )</td>
<td>Measured at Pin 11</td>
</tr>
<tr>
<td>Output Offset Current</td>
<td>( \pm 2 )</td>
<td>( \mu A )</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Impedance</td>
<td>1</td>
<td>( M\Omega )</td>
<td>( M\Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Swing</td>
<td>( \pm 4 )</td>
<td>( \pm 5 )</td>
<td>V</td>
<td>Referenced to Pin 10</td>
<td></td>
</tr>
<tr>
<td><strong>Quadrature Phase Detector</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>300</td>
<td>( \mu A )</td>
<td>( \mu A )</td>
<td></td>
<td>Measured at Pin 3</td>
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<tr>
<td>Output Impedance</td>
<td>1</td>
<td>( M\Omega )</td>
<td>( M\Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Swing</td>
<td>11</td>
<td></td>
<td>( V_{PP} )</td>
<td></td>
<td></td>
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<tr>
<td><strong>Input Preampt Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Input Impedance</td>
<td>20</td>
<td>K\Omega</td>
<td></td>
<td></td>
<td>Measured at Pin 2</td>
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<tr>
<td>Input Signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Voltage Required to Cause Limiting</td>
<td>2</td>
<td>mV rms</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

*Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.*

*Bold face parameters* are covered by production test and guaranteed over operating temperature range.
DC ELECTRICAL CHARACTERISTICS (CONT’D)

Test Conditions: \( V_{CC} = 12V \), \( T_A = +25^\circ C \), \( R_O = 30K\Omega \), \( C_O = 0.033\mu F \), unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
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<tr>
<td>Voltage Comparator Section</td>
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<td></td>
<td></td>
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<tr>
<td>Input Impedance</td>
<td>2</td>
<td></td>
<td></td>
<td>M\Omega</td>
<td>Measured at Pins 3 and 8</td>
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<tr>
<td>Input Bias Current</td>
<td>100</td>
<td></td>
<td></td>
<td>nA</td>
<td></td>
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<tr>
<td>Voltage Gain</td>
<td>55</td>
<td>70</td>
<td></td>
<td>dB</td>
<td>( R_L = 5.1K\Omega )</td>
</tr>
<tr>
<td>Output Voltage Low</td>
<td>300</td>
<td>500</td>
<td></td>
<td>mV</td>
<td>( I_O = 3mA )</td>
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<tr>
<td>Output Leakage Current</td>
<td>0.01</td>
<td>10</td>
<td></td>
<td>\mu A</td>
<td>( V_O = 20V )</td>
</tr>
<tr>
<td>Internal Reference</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Level</td>
<td>4.75</td>
<td>5.3</td>
<td>5.85</td>
<td>V</td>
<td>Measured at Pin 10</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>100</td>
<td></td>
<td></td>
<td>\Omega</td>
<td>AC Small Signal</td>
</tr>
<tr>
<td>Maximum Source Current</td>
<td>80</td>
<td></td>
<td></td>
<td>\mu A</td>
<td></td>
</tr>
</tbody>
</table>

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production. Bold face parameters are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

- Power Supply: 20V
- Input Signal Level: 3V rms
- Power Dissipation: 900mW
- Plastic Package: 800mW
- Derate Above \( T_A = 25^\circ C \): 6mW/\(^\circ C\)
- JEDEC SOIC: 390mW
- Derate Above \( T_A = 25^\circ C \): 5mW/\(^\circ C\)

SYSTEM DESCRIPTION

The main PLL within the XR-2211A is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a current controlled oscillator with its normal input current \( f_0 \) set by a resistor \( (R_0) \) to ground and its driving current with a resistor \( (R_1) \) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies (internally connected). When in lock, these frequencies are \( f_{IN} + f_{VCO} \) (2 times \( f_{IN} \) when in lock) and \( f_{IN} - f_{VCO} \) (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times \( f_{IN} \) component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).
PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is AC coupled to this terminal. The internal impedance at pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 3) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, pin 3 can be left open.

Lock Detect Output, Q (Pin 6): The output at pin 6 is at “low” state when the PLL is out of lock and goes to “high” state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V_CC for proper operation. At “low” state, it can sink up to 5mA of load current.

Lock Detect Complement, (Pin 5): The output at pin 5 is the logic complement of the lock detect output at pin 6. This output is also an open collector type stage which can sink 5mA of load current at low or “on” state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V_CC for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at “high” or “off” state for low input frequency, and at “low” or “on” state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F (see Figure 3). The threshold voltage of the comparator is set by the internal reference voltage, V_REF available at pin 10.

Reference Voltage, V_REF (Pin 10): This pin is internally biased at the reference voltage level, V_REF = V_CC/2 - 650mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_0 and C_0 connected to pin 11 (see Figure 11). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_REF. The peak to peak voltage swing available at the phase detector output is equal to 2 x V_REF.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

\[ f_0 = \frac{1}{R_0C_0} \text{ Hz} \]

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see Figure 9).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_REF. The maximum timing current drawn from pin 12 must be limited to ≤ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 6). C_0 must be non-polar, and in the range of 200pF to 10μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at pin 12 (see Figure 10).

VCO Free-Running Frequency, f_0: XR-2211A does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in Figure 3, and applying an alternating bit pattern of O’s and 1’s at the known mark and space frequencies. By adjusting R_0, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_0 value is accurately referenced to the mark and space frequencies.
Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211A

Figure 3. Generalized Circuit Connection for FSK and Tone Detection
DESIGN EQUATIONS

(All resistance in Ω, all frequency in Hz and all capacitance in farads, unless otherwise specified)
(See Figure 3 for definition of components)

1. VCO Center Frequency, \( f_O \):
   \[
   f_O = \frac{1}{R_0 \cdot C_0}
   \]

2. Internal Reference Voltage, \( V_{REF} \) (measured at pin 10):
   \[
   V_{REF} = \left( \frac{V_{CC}}{2} \right) \text{–650mV in volts}
   \]

3. Loop Low-Pass Filter Time Constant, \( \tau \):
   \[
   \tau = C_1 \cdot R_{pp} \text{ (seconds)}
   \]

   where:
   \[
   R_{pp} = \left( \frac{R_1 \cdot R_F}{R_1 + R_F} \right)
   \]

   if \( R_F \) is \( \infty \) or \( C_F \) reactance is \( \infty \), then \( R_{pp} = R1 \)

4. Loop Damping, \( \zeta \):
   \[
   \zeta = \sqrt{\frac{1250 \cdot C_0}{R_1 \cdot C_1}}
   \]

   Note: For derivation/explanation of this equation, please see TAN-011.

5. Loop-tracking bandwidth,
   \[
   \frac{\Delta f}{f_0} = \frac{R_0}{R_1}
   \]

   \[\text{Tracking Bandwidth} \]

   \[\Delta f \]

   \[f_{LL} \quad f_1 \quad f_0 \quad f_2 \quad f_{ LH}\]
6. FSK Data filter time constant, \( \tau_F \):

\[
\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \text{ (seconds)}
\]

7. Loop phase detector conversion gain, \( K_d \): (\( K_d \) is the differential DC voltage across pin 10 and pin11, per unit of phase error at phase detector input):

\[
K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot 2\pi} \left[ \frac{\text{volt}}{\text{radian}} \right]
\]

Note: For derivation/explanation of this equation, please see TAN-011.

8. VCO conversion gain, \( K_0 \): (\( K_0 \) is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

\[
K_0 = \frac{-2\pi}{V_{REF} \cdot C_0 \cdot R_1} = \left( \frac{\text{radian/second}}{\text{volt}} \right)
\]

9. The filter transfer function:

\[
F(s) = \frac{1}{1 + SR_1 \cdot C_1} \text{ at } 0 \text{ Hz. } \quad S = j\omega \text{ and } \omega = 0
\]

10. Total loop gain, \( K_T \):

\[
K_T = K_0 \cdot K_d \cdot F(s) = \left( \frac{R_F}{5,000 \cdot C_0 (R_1 + R_F)} \right) \left[ \frac{1}{\text{seconds}} \right]
\]

11. Peak detector current \( I_A \):

\[
I_A = \frac{V_{REF}}{20,000} \text{ (} V_{REF} \text{ in volts and } I_A \text{ in amps)}
\]

Note: For derivation/explanation of this equation, please see TAN-011.
APPLICATIONS INFORMATION

FSK Decoding

Figure 10 shows the basic circuit connection for FSK decoding. With reference to Figure 3 and Figure 10, the functions of external components are defined as follows: \( R_0 \) and \( C_0 \) set the PLL center frequency, \( R_1 \) sets the system bandwidth, and \( C_1 \) sets the loop filter time constant and the loop damping factor. \( C_F \) and \( R_F \) form a one-pole post-detection filter for the FSK data output. The resistor \( R_B \) from pin 7 to pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Design Instructions:

The circuit of Figure 10 can be tailored for any FSK decoding application by the choice of five key circuit components: \( R_0 \), \( R_1 \), \( C_0 \), \( C_1 \) and \( C_F \). For a given set of FSK mark and space frequencies, \( f_0 \) and \( f_1 \), these parameters can be calculated as follows:

(All resistance in \( \Omega \)'s, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Calculate PLL center frequency, \( f_0 \):

\[
f_0 = \frac{F_1 \cdot F_2}{2}
\]

b) Choose value of timing resistor \( R_0 \), to be in the range of 10K\( \Omega \) to 100K\( \Omega \). This choice is arbitrary. The recommended value is \( R_0 = 20K\Omega \). The final value of \( R_0 \) is normally fine-tuned with the series potentiometer, \( R_X \).

\[
R_0 = R_0 + \frac{R_X}{2}
\]

c) Calculate value of \( C_0 \) from design equation (1) or from Figure 7:

\[
C_0 = \frac{1}{R_0 \cdot f_0}
\]

d) Calculate \( R_1 \) to give the desired tracking bandwidth (See design equation 5).

\[
R_1 = \frac{R_0 \cdot f_0}{(f_1 - f_2)} \cdot 2
\]

e) Calculate \( C_1 \) to set loop damping. (See design equation 4):

Normally, \( \zeta = 0.5 \) is recommended.

\[
C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2}
\]
f) The input to the XR-2211A may sometimes be too sensitive to noise conditions on the input line. Figure 4 illustrates a method of desensitizing the XR-2211A from such noisy line conditions by the use of a resistor, Rx, connected from pin 2 to ground. The value of Rx is chosen by the equation and the desired minimum signal threshold level.

\[ V_{IN \ minimum \ (\text{peak})} = V_a - V_b = \Delta V \pm 2.8mV \ offset = V_{\text{REF}} \frac{20,000}{(20,000 + R_x)} \text{ or } R_x = 20,000 \left( \frac{V_{\text{REF}}}{\Delta V} - 1 \right) \]

\( V_{IN \ minimum \ (\text{peak})} \) input voltage must exceed this value to be detected (equivalent to adjusting \( V \) threshold).

![Figure 4. Desensitizing Input Stage](image)

\[ R_{\text{sum}} = \frac{(R_F + R_t) \cdot R_B}{(R_1 + R_F + R_B)} \]

\[ C_F = \frac{0.25}{(R_{\text{sum}} \cdot \text{Baud Rate})} \quad \text{Baud rate in} \quad \frac{1}{\text{seconds}} \]

Note: All values except \( R_0 \) can be rounded to nearest standard value.
Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)

Figure 6. VCO Frequency vs. Timing Resistor

Figure 7. VCO Frequency vs. Timing Capacitor

Figure 8. Typical fO vs. Power Supply Characteristics

Figure 9. Typical Center Frequency Drift vs. Temperature
Design Example:

1200 Baud FSK demodulator with mark and space frequencies of 1200/2200.

Step 1: Calculate $f_0$: from design instructions

(a) \( f_0 = \sqrt{\frac{1200 \cdot 2200}{2200}} = 1624 \)

Step 2: Calculate $R_0$ : $R_0 = 10K$ with a potentiometer of 10K. (See design instructions (b))

(b) \( R_T = 10 + \left( \frac{10}{2} \right) = 15K \)

Step 3: Calculate $C_0$ from design instructions

(c) \( C_0 = \frac{1}{15000 \cdot 1624} = 39nF \)

Step 4: Calculate $R_1$: from design instructions

(d) \( R_1 = \frac{20000 \cdot 1624 \cdot 2}{(2200 - 1200)} = 51,000 \)

Step 5: Calculate $C_1$: from design instructions

(e) \( C_1 = \frac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF \)

Step 6: Calculate $R_F$ : $R_F$ should be at least five times $R_1$, $R_F = 51,000 \cdot 5 = 255$ KΩ

Step 7: Calculate $R_B$ : $R_B$ should be at least five times $R_F$, $R_B = 255,000 \cdot 5 = 1.2$ MΩ

Step 8: Calculate $R_{SUM}$:

\[
R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240KΩ
\]

Step 9: Calculate $C_F$:

\[
C_F = \frac{0.25}{\left( \frac{R_{SUM} \text{ Baud Rate}}{R_{SUM}} \right)} = 1nF
\]

Note: All values except $R_0$ can be rounded to nearest standard value.
Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability
FSK Decoding with Carrier Detect

The lock detect section of XR-2211A can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 11. The open collector lock detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at “low” state, until there is a carrier within the detection band of the PLL and the pin 6 output goes “high” to enable the data output.

Note: Data Output is “Low” When No Carrier is Present.

The minimum value of the lock detect filter capacitance $C_D$ is inversely proportional to the capture range, $\pm \Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by $C_1$. For most applications, $\Delta f_c > \Delta f / 2$. For $R_D = 470K\Omega$, the approximate minimum value of $C_D$ can be determined by:

$$C_D > \frac{16}{\Delta f} \quad \text{C in } \mu \text{F and } f \text{ in Hz}.$$  

$C$ in $\mu$F and $f$ in Hz.

With values of $C_D$ that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of $C_D$ will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu$F.

Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at “high” and “low” logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink $5mA$ of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors $R_{L2}$ and $R_{L3}$, as shown in Figure 12.

With reference to Figure 3 and Figure 12, the functions of the external circuit components can be explained as follows: $R_0$ and $C_0$ set VCO center frequency; $R_1$ sets the detection bandwidth; $C_1$ sets the low pass-loop filter time constant and the loop damping factor.
Design Instructions:

The circuit of Figure 12 can be optimized for any tone detection application by the choice of the 5 key circuit components: R₀, R₁, C₀, C₁, and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

(All resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Choose value of timing resistor R₀ to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is R₀ = 20KΩ. The final value of R₀ is normally fine-tuned with the series potentiometer, Rₓ.

b) Calculate value of C₀ from design equation (1) or from Figure 7 f_S = f₀:

\[
C₀ = \frac{1}{R₀f_S}
\]

c) Calculate R₁ to set the bandwidth ±Δf (See design equation 5):

\[
R₁ = \frac{R₀f₀·2}{Δf}
\]

Note: The total detection bandwidth covers the frequency range of f₀ ±Δf

d) Calculate value of C₁ for a given loop damping factor:

Normally, ζ = 0.5 is recommended.

\[
C₁ = \frac{1250·C₀}{R₁ζ²}
\]

Increasing C₁ improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

\[
C_D > \frac{16}{Δf} \quad \text{in} \ \mu F
\]

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of ±100Hz:

a) Choose value of timing resistor R₀ to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is R₀ = 20 KΩ. The final value of R₀ is normally fine-tuned with the series potentiometer, Rₓ.

b) Calculate value of C₀ from design equation (1) or from Figure 6 f_S = f₀:

\[
C₀ = \frac{1}{R₀f_S} = \frac{1}{20,000·1,000} = 50nF
\]
c) Calculate $R_1$ to set the bandwidth $\pm \Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

**Note:** The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$

d) Calculate value of $C_0$ for a given loop damping factor:

Normally, $\zeta = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2} = \frac{1250 \cdot 50 \cdot 10^{-9}}{400,000 \cdot 0.5^2} = 6.25pF$$

Increasing $C_1$ improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor $C_D$. To avoid chatter at the logic output, with $R_D = 470K\Omega$, $C_D$ must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing $C_D$ slows down the logic output response time.

f) Fine tune center frequency with 5K$\Omega$ potentiometer, $R_X$.

---

**Figure 13.** Linear FM Detector Using XR-2211A and an External Op Amp.  
(See Section on Design Equation for Component Values.)
Linear FM Detection

XR-2211A can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 13. The demodulated output is taken from the loop phase detector output (pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 13.

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

\[ V_{\text{OUT}} = \frac{R_1 \cdot V_{\text{REF}}}{100 \cdot R_0} \]

where VR is the internal reference voltage (\( V_{\text{REF}} = \frac{V_{\text{CC}}}{2} - 650\text{mV} \)). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see the section on design equations.

**Figure 14. Equivalent Schematic Diagram**
14 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)

Rev. 1.00

**Seating Plane**

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*Note: The control dimension is the inch column.*

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**Figures:**
- XR-2211A 14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)
## 14 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

**Rev. 1.00**

### Symbol and Dimensions

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*Note: The control dimension is the millimeter column.*
Notes
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