General Description

The XR79115 is a 15A synchronous step-down Power Module for point-of-load supplies. A wide 5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V, and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR79115 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, hence simplifying circuit implementation and reducing overall component count. The control loop also provides 0.35% load and 0.1% line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads, thereby significantly increasing the converter efficiency. With a 96% peak efficiency and 90% for loads as low as 100mA, the XR79115 is suitable for applications where low power losses are important.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR79115 is available in a RoHS compliant, green / halogen free space-saving 68-pin 12 x 12 x 4mm QFN package. With integrated controller, drivers, bootstrap diode and capacitor, MOSFETs, inductor, CIN and COUT, this solution allows the smallest possible 15A POL design.

FEATURES

- Controller, drivers, bootstrap diode and capacitor, MOSFETs, inductor, CIN and COUT integrated in one package
- 15A step down module
  - Wide 5V to 22V input voltage range
  - ≥0.6V adjustable output voltage
- Proprietary Constant On-Time control
  - No loop compensation required
  - Stable ceramic output capacitor operation
  - Programmable 200ns to 2µs on-time
  - Constant 400kHz to 600kHz frequency
- Selectable CCM or CCM / DCM
  - CCM / DCM for high efficiency at light-load
  - CCM for constant frequency at light-load
- Programmable hiccup current limit with thermal compensation
- Precision enable and Power Good flag
- Programmable soft-start
- 68-pin 12 x 12 x 4mm QFN package

APPLICATIONS

- Networking and communications
- Fast transient Point-of-Loads
- Industrial and medical equipment
- Embedded high power FPGA

Ordering Information – back page
Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

- \( P_{VIN}, V_{IN} \) : -0.3V to 25V
- \( V_{CC} \) : -0.3V to 6.0V
- \( BST \) : -0.3V to 31V
- \( BST-SW \) : -0.3V to 6V
- \( SW, ILIM \) : -1V to 25V
- All other pins: -0.3V to \( V_{CC} + 0.3V \)
- Storage temperature: -65°C to +150°C
- Junction temperature: 150°C
- Power dissipation: Internally Limited
- Lead temperature (Soldering, 10 sec): 260°C MSL3
- ESD Rating (HBM - Human Body Model): 2kV

Operating Conditions

- \( PV_{IN} \) : -3V to 22V
- \( V_{IN} \) : 4.5V to 22V
- \( V_{CC} \) : 4.5V to 5.5V
- \( SW, ILIM \) : -1V to 22V
- \( PGOOD, V_{CC}, T_{ON}, SS, EN, FB \) : -0.3V to 5.5V
- Switching frequency: 400kHz to 600kHz
- Junction temperature range: -40°C to +125°C
- JEDEC51 Package thermal resistance, \( \theta_{JA} \) : 15.4°C/W
- Package power dissipation at 25°C: 6.5W

Note 1: No external voltage applied.
Note 2: The SW pin’s minimum DC range is -1V, transient is -5V for less than 50ns.
Note 3: Recommended frequency for optimum performance.

Electrical Characteristics

Unless otherwise noted: \( T_J = 25°C \), \( V_{IN} = 12V \), \( BST = V_{CC} \), \( SW = AGND = PGND = 0V \), \( V_{CC} = 4.7\mu F \). Limits applying over the full operating temperature range are denoted by a “*”.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Supply Characteristics</strong></td>
<td></td>
<td>VCC regulating</td>
<td>5</td>
<td>22</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Input voltage range</td>
<td>VCC tied to VIN</td>
<td>4.5</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{VIN} )</td>
<td>VIN input supply current</td>
<td>Not switching, ( V_{IN} = 12V, V_{FB} = 0.7V )</td>
<td>0.7</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{VCC} )</td>
<td>VCC quiescent current</td>
<td>Not switching, ( V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V )</td>
<td>0.7</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{VIN} )</td>
<td>VIN input supply current</td>
<td>( f=500kHz, R_{ON} = 61.9k\Omega, V_{FB} = 0.58V )</td>
<td>17</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Shutdown current</td>
<td>Enable = 0V, ( V_{IN} = 12V )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>Enable and Under-Voltage Lock-Out UVLO</strong></td>
<td></td>
<td>( V_{IH, EN} ) EN pin rising threshold</td>
<td>1.8</td>
<td>1.9</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ENHYS} )</td>
<td>EN pin hysteresis</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{IH, EN} )</td>
<td>EN pin rising threshold for DCM / CCM operation</td>
<td></td>
<td>2.8</td>
<td>3.0</td>
<td>3.1</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ENHYS} )</td>
<td>EN pin hysteresis</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
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</table>
### Symbol Table

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VCC UVLO start threshold, rising edge</td>
<td></td>
<td>4.00</td>
<td>4.25</td>
<td>4.40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCC UVLO hysteresis</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

### Reference Voltage

| V_REF  | Reference voltage                             | VIN = 5V to 22V, VCC regulating                | 0.597 | 0.600 | 0.603 | V     |
|        |                                               | VIN = 4.5V to 5.5V, VCC tied to VIN           | 0.596 | 0.600 | 0.604 | V     |
|        |                                               | VIN = 5V to 22V, VCC regulating                | 0.594 | 0.600 | 0.606 | V     |
|        | DC line regulation                            | CCM, closed loop, VIN = 4.5V - 22V, applies to any COUT | ±0.10 |      |      | %     |
|        | DC load regulation                            | CCM, closed loop, IOUT = 0A - 15A, applies to any COUT | ±0.35 |      |      | %     |

### Programmable Constant On-Time

| T_ON(MIN) | Minimum programmable on-time | R_ON = 6.98kΩ, VIN = 22V | 120 | ns   |
| T_ON2     | On-time 2                      | R_ON = 6.98kΩ, VIN = 12V | * 156 | 192 | 228 ns   |
| T_ON3     | On-time 3                      | R_ON = 16.2kΩ, VIN = 12V | * 341 | 412 | 483 ns   |

### Diode Emulation Mode

| Zero crossing threshold | DC value measured during test | -2 | mV   |

### Soft-start

| SS charge current      |                              | * -14 | -10 | -6 | µA   |
| SS discharge current   |                              | * 1   |     |    | mA   |

### VCC Linear Regulator

| VCC output voltage     | VIN = 6V to 22V, ILOAD = 0 to 30mA | * 4.8 | 5.0 | 5.2 | V     |
| VIN = 5V, ILOAD = 0 to 20mA |                             | * 4.6 | 4.8 |    | V     |

### Power Good Output

| Power Good threshold   |                              | -10  | -7.5 | -5 | %    |
| Power Good hysteresis  |                              | 2    | 4    |    | %    |
| Power Good sink current|                              | 1    |      |    | mA   |

### Protection: OCP, OTP, Short-Circuit

<p>| Hiccup timeout | 110 | ms   |
| ILIM pin source current | 45  | 50  | 55  | µA   |
| ILIM current temperature coefficient | 0.4 |    | %/°C |
| OCP comparator offset | * -8 | 0  | +8  | mV   |</p>
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Current limit blanking</td>
<td>GL rising &gt; 1V</td>
<td></td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown threshold&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Rising temperature</td>
<td></td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Thermal hysteresis&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td>15</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VSCTH feedback pin short-circuit threshold</td>
<td>Percent of VREF, short circuit is active after PGOOD is asserted</td>
<td>• 50</td>
<td>60</td>
<td>70</td>
<td>%</td>
</tr>
</tbody>
</table>

### Output Power Stage

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>R&lt;sub&gt;DSON&lt;/sub&gt;</strong></td>
<td>High-side MOSFET R&lt;sub&gt;DSON&lt;/sub&gt;, I&lt;sub&gt;DS&lt;/sub&gt; = 2A, V&lt;sub&gt;GS&lt;/sub&gt; = 4.5V</td>
<td>8.3</td>
<td>10</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low-side MOSFET R&lt;sub&gt;DSON&lt;/sub&gt;</td>
<td>4.2</td>
<td>5</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td><strong>I&lt;sub&gt;OUT&lt;/sub&gt;</strong></td>
<td>Maximum output current</td>
<td></td>
<td>15</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td><strong>L</strong></td>
<td>Output inductance</td>
<td>0.45</td>
<td>0.56</td>
<td>0.67</td>
<td>uH</td>
</tr>
<tr>
<td></td>
<td><strong>C&lt;sub&gt;N&lt;/sub&gt;</strong></td>
<td>Input capacitance</td>
<td>1</td>
<td></td>
<td></td>
<td>uF</td>
</tr>
<tr>
<td></td>
<td><strong>C&lt;sub&gt;OUT&lt;/sub&gt;</strong></td>
<td>Output capacitance</td>
<td>2.2</td>
<td></td>
<td></td>
<td>uF</td>
</tr>
<tr>
<td></td>
<td><strong>C&lt;sub&gt;BST&lt;/sub&gt;</strong></td>
<td>Bootstrap capacitance</td>
<td>0.1</td>
<td></td>
<td></td>
<td>uF</td>
</tr>
</tbody>
</table>

Note 1: Guaranteed by design
Pin Configuration, Top View
## Pin Assignments

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SS</td>
<td>A</td>
<td>Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.</td>
</tr>
<tr>
<td>2</td>
<td>PGOOD</td>
<td>OD, O</td>
<td>Power-Good output. This open-drain output is pulled low when $V_{OUT}$ is outside the regulation.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>A</td>
<td>Feedback input to feedback comparator. Connect with a set of resistors to $V_{OUT}$ and AGND in order to program $V_{OUT}$.</td>
</tr>
<tr>
<td>4, 67, AGND Pad</td>
<td>AGND</td>
<td>A</td>
<td>Analog ground. Control circuitry of the IC is referenced to this pin.</td>
</tr>
<tr>
<td>5</td>
<td>VIN</td>
<td>PWR</td>
<td>IC supply input. Provides power to the internal LDO.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>PWR</td>
<td>The output of LDO. Bypass with a 4.7µF capacitor to AGND. For operation from a 5VIN rail, VCC should be tied to VIN.</td>
</tr>
<tr>
<td>7, GL pad</td>
<td>GL</td>
<td>O</td>
<td>Driver output for low-side N-channel synchronous MOSFET. It is internally connected to the gate of the FET. Leave this pin floating.</td>
</tr>
<tr>
<td>8</td>
<td>PGND</td>
<td>PWR</td>
<td>Controller low-side driver ground. Connect with a short trace to the closest PGND pins or PGND pad.</td>
</tr>
<tr>
<td>13-23, 54, 55, PGND pads</td>
<td>PGND</td>
<td>PWR</td>
<td>Ground of the power stage. Should be connected to the system’s power ground plane.</td>
</tr>
<tr>
<td>9-12, 24-29, SW Pad</td>
<td>SW</td>
<td>PWR</td>
<td>Switching node. It is internally connected. Use thermal vias and / or sufficient PCB land area in order to heatsink the low-side FET and the inductor.</td>
</tr>
<tr>
<td>30-53, VOUT pads</td>
<td>VOUT</td>
<td>PWR</td>
<td>Output of the power stage. Place the output filter capacitors as close as possible to these pins.</td>
</tr>
<tr>
<td>56-62, PVIN Pad</td>
<td>PVIN</td>
<td>PWR</td>
<td>Power stage input voltage. Place the input filter capacitors as close as possible to these pins.</td>
</tr>
<tr>
<td>63, 64, BST Pad</td>
<td>BST</td>
<td>A</td>
<td>Controller high-side driver supply pin. It is internally connected to SW via a 0.1µF bootstrap capacitor. Leave these pins floating.</td>
</tr>
<tr>
<td>65</td>
<td>ILIM</td>
<td>A</td>
<td>Over-current protection programming. Connect with a short trace to the SW pins.</td>
</tr>
<tr>
<td>66</td>
<td>EN/MODE</td>
<td>I</td>
<td>Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM depending on load.</td>
</tr>
<tr>
<td>68</td>
<td>TON</td>
<td>A</td>
<td>Constant on-time programming pin. Connect with a resistor to AGND.</td>
</tr>
</tbody>
</table>

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain
Functional Block Diagram
Typical Performance Characteristics

Unless otherwise noted: $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $I_{OUT} = 15A$, $f = 500kHz$, $T_A = 25^\circ C$. The schematic is from the application information section.
Typical Performance Characteristics

Unless otherwise noted: $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $I_{OUT} = 15A$, $f = 500kHz$, $T_A = 25^\circ C$. The schematic is from the application information section.

**Figure 7:** $I_{OCP}$ versus $R_{LIM}$

**Figure 8:** $V_{REF}$ versus temperature

**Figure 9:** $I_{LIM}$ versus temperature

**Figure 10:** $T_{ON}$ versus temperature, $R_{ON}=16.2k\Omega$

**Figure 11:** Inductance versus Current

**Figure 12:** Maximum recommended $V_{OUT}$ versus $f$, $V_{IN}=12V$
Typical Performance Characteristics

Unless otherwise noted: $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $I_{OUT} = 15A$, $f = 500kHz$, $T_A = 25^\circ C$. The schematic is from the application information section.

Figure 13: Steady state, CCM, $I_{OUT}=15A$

Figure 14: Steady state, DCM, $I_{OUT}=0A$

Figure 15: Power up, Forced CCM

Figure 16: Power up, DCM/CCM

Figure 17: Load step, Forced CCM, 0A-7.5A-0A

Figure 18: Load step, DCM/CCM, 0A-7.5A-0A
Efficiency and Package Thermal Derating

Unless otherwise noted: $T_{\text{AMBIENT}} = 25^\circ C$, no air flow, $f = 500\text{kHz}$, the schematic is from the application information section.

Figure 19: Efficiency, $V_{\text{IN}}=5\text{V}$

Figure 20: Maximum $T_{\text{AMBIENT}}$ vs $I_{\text{OUT}}$, $V_{\text{IN}}=5\text{V}$

Figure 21: Efficiency, $V_{\text{IN}}=12\text{V}$

Figure 22: Maximum $T_{\text{AMBIENT}}$ vs $I_{\text{OUT}}$, $V_{\text{IN}}=12\text{V}$

Figure 23: Efficiency, $V_{\text{IN}}=19.6\text{V}$

Figure 24: Maximum $T_{\text{AMBIENT}}$ vs $I_{\text{OUT}}$, $V_{\text{IN}}=19.6\text{V}$
**Functional Description**

The XR79115 is a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) module. The on-time, which is programmed via $R_{ON}$, is inversely proportional to $V_{IN}$ and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with the GH signal turning on the high-side (switching) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When $V_{FB}$ drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

**Enable / Mode Input (EN/MODE)**

The EN/MODE pin accepts a tri-level signal that is used to control turn on and turn off. It also selects between two modes of operation: ‘Forced CCM’ and ‘DCM / CCM’. If EN/MODE is pulled below 1.8V, the module shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM mode, which will run the module in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the module in discontinuous conduction at light loads.

**Selecting the Forced CCM Mode**

In order to set the module to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from $V_{IN}$. If $V_{IN}$ is well regulated, use a resistor divider and set the voltage to 2.5V. If $V_{IN}$ varies over a wide range, the circuit shown in Figure 25 can be used to generate the required voltage. Note that at $V_{IN}$ of 5V and 22V, the nominal Zener voltage is 3.8V and 4.7V, respectively. Therefore for $V_{IN}$ in the range of 5V to 22V, the circuit shown in Figure 25 will generate the $V_{EN}$ required for Forced CCM.

**Selecting the DCM / CCM Mode**

In order to set the module operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications
Programming the On-Time

The on-time $T_{ON}$ is programmed via resistor $R_{ON}$ according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON}-(25\times10^{-9})]}{2.85\times10^{-10}}$$

where $T_{ON}$ is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff}$$

Where:

- $f$ is the desired switching frequency at nominal $I_{OUT}$
- $Eff$ is the Module efficiency corresponding to nominal $I_{OUT}$ shown in Figures 19, 21, 23

Substituting for $T_{ON}$ in the first equation we get:

$$R_{ON} = \frac{V_{OUT}}{f \times Eff} - [(25\times10^{-9}) \times V_{IN}]$$

Over-Current Protection (OCP)

If load current exceeds the programmed over-current $I_{OCP}$ for four consecutive switching cycles, then the module enters the hiccup mode of operation. In hiccup mode, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, the hiccup timeout will repeat. The module will remain in hiccup mode until the load current is reduced below the programmed $I_{OCP}$. In order to program the over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

- $RLIM$ is resistor value for programming $I_{OCP}$
- $I_{OCP}$ is the over-current threshold to be programmed
- $RDS$ is the MOSFET rated on-resistance (5mΩ)
- $8mV$ is the OCP comparator maximum offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C (Figure 9). This is meant to roughly match and compensate for the positive temperature coefficient of the synchronous FET. A graph of typical $I_{OCP}$ versus RLIM is shown in Figure 7.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the module will enter hiccup mode. Hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gates of the switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the Application Circuit to program the output voltage $V_{OUT}$.

$$R1 = R2 \times \left( \frac{V_{OUT}}{0.6} - 1 \right)$$

where $R2$ has a nominal value of 2kΩ.

Programming the Soft-start

Place a capacitor CSS between the SS and AGND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left( \frac{10\mu A}{0.6V} \right)$$

Feed-Forward Capacitor ($C_{FF}$)

A feed-forward capacitor ($C_{FF}$) may be necessary, depending on the Equivalent Series Resistance (ESR) of $C_{OUT}$. If only ceramic output capacitors are used for $C_{OUT}$, then a $C_{FF}$ is necessary. Calculate $C_{FF}$ from:

$$C_{FF} = \frac{1}{2 \times \pi \times 80kHz \times R1}$$
where:

R1 is the resistor that C_{FF} is placed in parallel with

80kHz is the location of the Zero formed by R1 and C_{FF}

Note that minimum required C_{OUT} is 140uF when using ceramic capacitors.

When using capacitors with higher ESR, such as the PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 15kHz.
2. The frequency of ESR Zero f_{Zero,ESR} should be at least three times larger than f_{LC}.

As an example the application circuit has f_{LC} = 8.3kHz and f_{Zero,ESR} = 23.4kHz.

Note that the steady-state voltage ripple at feedback pin FB (V_{FB,RIPPLE}) must not exceed 50mV in order for the module to function correctly. If V_{FB,RIPPLE} is larger than 50mV, then C_{OUT} should be increased as necessary in order to keep the V_{FB,RIPPLE} below 50mV.

Feed-Forward Resistor (R_{FF})

Poor PCB layout can cause FET switching noise at the output and may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor R_{FF} in series with C_{FF}. An R_{FF} value up to 2% of R1 is acceptable.
Application Circuit

12VIN

500kHz, 15A@1.2VOUT

R1 2k
R2 2k

PVIN

CVIN 0.1uF

CSS 47nF

VCC 4.7uF

U1 XR79115

R5 10k

V53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30

VOUT PAD 2
VOUT PAD 1

V13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

PGND PAD 1
PGND PAD 2

PVIN PAD

PGND13 PGND14 PGND17 PGND19 PGND20 PGND21 PGND22 PGND54 PGND55

PGND PAD 2

PVIN

PVIN 56 PVIN 57 PVIN 58 PVIN 59 PVIN 60 PVIN 61 PVIN 62

BST 63 BST 64 ILIM 65

EN/MODE 66 AGND 67

TON 68 AGND PAD

BST PAD

VCC

FB

VCC

VCC

SS

PGOOD

FB

AGND

VIN

VCC

GL

PGND

GL PAD

SW PAD

VOUT 30 VOUT 31 VOUT 32 VOUT 33 VOUT 34 VOUT 35 VOUT 36 VOUT 37 VOUT 38

VOUT 39 VOUT 40 VOUT 41 VOUT 42 VOUT 43 VOUT 44 VOUT 45 VOUT 46 VOUT 47

VOUT 48 VOUT 49 VOUT 50 VOUT 51 VOUT 52

VOUT 53

VOUT PAD 1

VOUT PAD 2

Optional

RSNB 1 Ohm

CSNB 1nF

OPTIONAL

R4 10k
R3 38.3k

RON 8.87k
RLIM 2.49k

2x22F

2x22F

0.1uF

4.7uF

22uF

22uF

0.1uF

680uF

3x47uF

500kHz, 15A@1.2VOUT

PVIN
Mechanical Dimensions

TERMINAL AND PAD EDGE DETAILS

NOTE: ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000075
Revision: B
TYPICAL RECOMMENDED LAND PATTERN

TYPICAL RECOMMENDED STENCIL

NOTE: ALL DIMENSIONS ARE IN MILLI METERS, ANGLES ARE IN DEGREES.
Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Lead-Free</th>
<th>Package</th>
<th>Packaging Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>XR79115EL-F</td>
<td>-40°C to +125°C</td>
<td>Yes(2)</td>
<td>12x12mm QFN</td>
<td>Tray</td>
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<tr>
<td>XR79115EVB</td>
<td></td>
<td></td>
<td>XR79115 Evaluation Board</td>
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</table>

NOTE:
1. Refer to www.maxlinear.com/XR79115 for most up-to-date Ordering Information.

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A</td>
<td>December 2014</td>
<td>ECN 1451-09</td>
</tr>
<tr>
<td>1B</td>
<td>January 2015</td>
<td>Corrected schematic on page 1, ECN 1504-06</td>
</tr>
<tr>
<td>1C</td>
<td>June 2018</td>
<td>Update to MaxLinear logo. Update format and Ordering Information format.</td>
</tr>
<tr>
<td>1D</td>
<td>November 2019</td>
<td>Correct block diagram by changing the input gate that connects to the Hiccup Mode block from an AND gate to an OR gate.</td>
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