GENERAL DESCRIPTION

The XRP6141 is a synchronous step-down controller for point-of-load supplies up to 35A. A wide 4.5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XRP6141 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation hence simplifying circuit implementation and reducing overall component count. The control loop also provides exceptional line regulation and maintains constant operating frequency. A selectable power saving mode, allows the user to operate in discontinuous mode (DCM) at light current loads thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XRP6141 is available in RoHS compliant, green/halogen free space-saving 16-pin 3x3 QFN package.

APPLICATIONS

- Networking and Communications
- Fast Transient Point-of-Loads
- Industrial and Medical Equipment
- Embedded High Power FPGA

FEATURES

- **35A Capable Step Down Controller**
  - Wide Input Voltage Range
    - 5V to 22V Single Supply
    - 4.5V to 5.5V Low VIN
  - Integrated high Current 2A/3A Drivers
  - Constant 200kHz-800kHz Frequency
  - Selectable CCM or CCM/DCM Operation

- **Proprietary Constant On-Time Control**
  - No Loop Compensation Required
  - Ceramic Output Cap. Stable operation
  - Programmable 200ns-2µs
  - Selectable CCM or CCM/DCM Operation

- **Programmable hiccup current limit with thermal compensation**
- **Precision Enable and Power-Good Flag**
- **Programmable Soft-start**
- **Integrated Bootstrap diode**
- **16-pin QFN Package**

TYPICAL APPLICATION DIAGRAM

![Fig. 1: XRP6141 Application Diagram](image-url)
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VIN ............................................................ -0.3V to 28V
VCC .......................................................... -0.3V to 6.0V
BST ......................................................... -0.3V to 34V
BST-SW ...................................................... -0.3V to 6V
SW, ILIM .................................................. -5V to 28V
GH................................................... -0.3V to BST+0.3V
GH-SW ........................................................ -0.3V to 6V
ALL other pins ................................... -0.3V to VCC+0.3V

Storage Temperature .............................. -65°C to 150°C
Junction Temperature .......................................... 150°C
Power Dissipation ................................ Internally Limited
Lead Temperature (Soldering, 10 sec) ................... 300°C
ESD Rating (HBM - Human Body Model) ................. 2kV

OPERATING RATINGS

VIN ........................................................... -0.3V to 22V
VCC .......................................................... -0.3V to 5.5V
SW, ILIM ................................................... -1V to 26V
PGOOD, VCC, TON, SS, EN, GL, FB ............ -0.3V to 5.5V
Switching Frequency ............................. 200kHz-800kHz

Junction Temperature Range .................... -40°C to 125°C

Note 1: SW pin’s minimum DC range is -1V, transient is -5V for less than 50ns
Note 2: No external voltage applied
Note 3: Recommended

ELECTRICAL SPECIFICATIONS

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, VIN = 12V, BST=VCC, SW=GND=PGND=0V, CGH=CGL=3.3nF.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN, Input Voltage Range</td>
<td>5</td>
<td>12</td>
<td>22</td>
<td>V</td>
<td>VCC regulating</td>
</tr>
<tr>
<td></td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
<td>VCC tied to V_IN</td>
</tr>
<tr>
<td>I_{VIN}, VIN supply current</td>
<td>0.7</td>
<td>2</td>
<td>mA</td>
<td>•</td>
<td>Not switching, V_IN = 12V, VFB = 0.7V</td>
</tr>
<tr>
<td>I_{VCC}, VCC Quiescent current</td>
<td>0.7</td>
<td>2</td>
<td>mA</td>
<td>•</td>
<td>Not switching, V_CCC = V_IN = 5V, VFB = 0.7V</td>
</tr>
<tr>
<td>I_{VIN}, VIN supply current</td>
<td>11</td>
<td>mA</td>
<td>•</td>
<td>F = 300kHz, RON = 108.8k, VFB = 0.58V</td>
<td></td>
</tr>
<tr>
<td>I_{OFF}, Shutdown current</td>
<td>0.1</td>
<td>μA</td>
<td>•</td>
<td>Enable = 0V, V_IN = 12V</td>
<td></td>
</tr>
<tr>
<td>Enable and Under-Voltage Lock-Out UVLO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IH,EN}, EN Pin Rising Threshold</td>
<td>1.8</td>
<td>1.9</td>
<td>2.0</td>
<td>V</td>
<td>•</td>
</tr>
<tr>
<td>V_{HEN,HSYS, EN Pin Hysteresis}</td>
<td>50</td>
<td>mV</td>
<td>•</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IH,EN}, EN Pin Rising Threshold for DCM/CCM operation</td>
<td>2.9</td>
<td>3.0</td>
<td>3.1</td>
<td>V</td>
<td>•</td>
</tr>
<tr>
<td>V_{HEN,HSYS, EN Pin Hysteresis}</td>
<td>100</td>
<td>mV</td>
<td>•</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC UVLO start threshold, rising edge</td>
<td>4.00</td>
<td>4.25</td>
<td>4.50</td>
<td>V</td>
<td>•</td>
</tr>
<tr>
<td>VCC UVLO Hysteresis</td>
<td>200</td>
<td>mV</td>
<td>•</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{REF}, Reference voltage</td>
<td>0.597</td>
<td>0.600</td>
<td>0.603</td>
<td>V</td>
<td>V_IN = 5V-22V → VCC regulating</td>
</tr>
<tr>
<td></td>
<td>0.596</td>
<td>0.604</td>
<td>V</td>
<td>V_IN = 4.5V-5.5V → tie VCC to V_IN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.594</td>
<td>0.600</td>
<td>0.606</td>
<td>V</td>
<td>•</td>
</tr>
<tr>
<td>DC Line regulation</td>
<td>±0.1</td>
<td>%</td>
<td>•</td>
<td>CCM operation, closed loop, applies to any C_OUT</td>
<td></td>
</tr>
<tr>
<td>DC Load regulation</td>
<td>±0.25</td>
<td>%</td>
<td>•</td>
<td>CCM operation, closed loop, applies to any C_OUT</td>
<td></td>
</tr>
</tbody>
</table>
## Parameter | Min. | Typ. | Max. | Units | Conditions
--- | --- | --- | --- | --- | ---
**Programmable Constant On-Time**
On-Time 1 | 1855 | 2182 | 2509 | ns | RON = 141.2kΩ, VIN = 22V
f corresponding to On-Time 1 | 217 | 250 | 294 | kHz | VIN = 22V, VOUT = 12V
Minimum Programmable On-Time | 109 | ns | | ns | RON = 7.059kΩ, VIN = 22V
On-Time 2 | 170 | 200 | 230 | ns | RON = 7.059kΩ, VIN = 12V
f corresponding to On-Time 2 | 1618 | 1375 | 1196 | kHz | VOUT = 1.0V
f corresponding to On-Time 2 | 490 | 417 | 362 | kHz | VOUT = 3.3V
On-Time 3 | 391 | 460 | 529 | ns | RON = 16.235kΩ, VIN = 12V
Minimum Off-Time | 250 | 350 | ns | | *
**Diode Emulation Mode**
Zero crossing threshold | -4 | -1 | | mV | DC value measured during test
**SoftStart**
SS Charge current | -14 | -10 | -6 | µA | *
SS Discharge current | 1 | | | mA | * Fault present
**VCC Linear Regulator** *(VCC should be tied to VIN, for 4.5V ≤ VIN ≤ 5.5V)*
VCC Output Voltage | 4.8 | 5.0 | 5.2 | V | VIN = 6V to 22V, Iload = 0 to 30mA
Dropout Voltage | 4.51 | 4.7 | | V | VIN = 5V, Iload = 0 to 20mA
**Power Good Output**
Power Good Threshold | -10 | -7.5 | -5 | % | *
Power Good Hysteresis | 2 | 4 | | % | *
Power Good Sink Current | 1 | | | mA | *
**Protection: OCP, OTP, Short-circuit**
Hiccup timeout | 110 | | | ms | *
ILIM pin source current | 45 | 50 | 55 | µA | *
ILIM current temperature coeff. | 0.4 | | | %/°C | *
OCP comparator offset | -8 | 0 | +8 | mV | *
Current limit blanking | 100 | | | ns | GL rising > 1V
Thermal shutdown threshold | 150 | | | °C | Rising temperature
Thermal Hysteresis | 15 | | | °C | *
VSCSTH Feedback pin short-circuit threshold | 50 | 60 | 70 | % | Percent of VREF, short circuit is active After PGGOOD is up
**Output Gate drivers**
GH Pull-Down Resistance | 1.35 | 2.0 | | Ω | IGH = 200mA
GH Pull-up Resistance | 1.8 | 2.8 | | Ω | IGH = 200mA
GL Pull-Down Resistance | 1.35 | 1.9 | | Ω | IGL = 200mA
GL Pull-up Resistance | 1.7 | 2.7 | | Ω | IGL = 200mA
GH and GL pull-down Resistance | 50 | | | kΩ | *
GH and GL rise time | 35 | 50 | | ns | 10% to 90%
GH and GL fall time | 30 | 40 | | ns | 90% to 10%
GL to GH non-overlap time | 20 | 30 | 60 | ns | Measured GL falling edge = 1V to GH rising edge = 1V, BST = VCC, SW = 0V
GH to GL non-overlap time | 15 | 20 | 40 | ns | Measured GH falling edge = 1V to GL rising edge = 1V

Note 1: Guaranteed by design
**BLOCK DIAGRAM**

![BLOCK DIAGRAM](image)

**PIN ASSIGNMENT**

![PIN ASSIGNMENT](image)

---

**XRP6141**

35A Synchronous Step Down COT Controller

---

Fig. 2: XRP6141 Block Diagram

Fig. 3: XRP6141 Pin Assignment
## PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL</td>
<td>1</td>
<td>Driver output for Low-side N-channel synchronous MOSFET.</td>
</tr>
<tr>
<td>NC</td>
<td>2</td>
<td>Internally not connected. Leave this pin floating.</td>
</tr>
<tr>
<td>SW</td>
<td>3</td>
<td>Lower supply rail for high-side gate driver GH. Connect this pin to the junction between the two external N-channel MOSFETs.</td>
</tr>
<tr>
<td>GH</td>
<td>4</td>
<td>Driver output for high-side N-channel switching MOSFET.</td>
</tr>
<tr>
<td>BST</td>
<td>5</td>
<td>High-side driver supply pin. Connect a 0.1uF bootstrap capacitor between BST and SW.</td>
</tr>
<tr>
<td>ILIM</td>
<td>6</td>
<td>Over-current protection programming. Connect with a resistor to the Drain of the low-side MOSFET.</td>
</tr>
<tr>
<td>EN/MODE</td>
<td>7</td>
<td>Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V then the IC will operate in DCM or CCM depending on load.</td>
</tr>
<tr>
<td>TON</td>
<td>8</td>
<td>Constant on-time programming pin. Connect with a resistor to AGND.</td>
</tr>
<tr>
<td>SS</td>
<td>9</td>
<td>Soft-Start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10uA internal source current.</td>
</tr>
<tr>
<td>PGOOD</td>
<td>10</td>
<td>Power-good output. This open-drain output is pulled low when VOUT is outside the regulation.</td>
</tr>
<tr>
<td>FB</td>
<td>11</td>
<td>Feedback input to feedback comparator. Connect with a set of resistors to VOUT and GND in order to program VOUT.</td>
</tr>
<tr>
<td>AGND</td>
<td>12, 13</td>
<td>Analog ground. Control circuitry of the IC is referenced to this pin.</td>
</tr>
<tr>
<td>VIN</td>
<td>14</td>
<td>IC supply input. Provides power to internal LDO.</td>
</tr>
<tr>
<td>VCC</td>
<td>15</td>
<td>The output of LDO. For operation using a 5V rail, VCC should be shorted to VIN.</td>
</tr>
<tr>
<td>PGND</td>
<td>16</td>
<td>Low side driver ground</td>
</tr>
</tbody>
</table>

Exposed Pad
- Thermal pad for heat dissipation. Connect to AGND with a short trace.

## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Lead-Free</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>XRP6141EL-F</td>
<td>-40°C ≤ TJ ≤ +125°C</td>
<td>Yes(2)</td>
<td>3x3mm QFN16</td>
<td>Tray</td>
</tr>
<tr>
<td>XRP6141ELTR-F</td>
<td></td>
<td></td>
<td></td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>XRP6141EVB</td>
<td></td>
<td></td>
<td></td>
<td>XRP6141 Evaluation Board</td>
</tr>
</tbody>
</table>

NOTES:
1. Refer to [www.exar.com/XRP6141](http://www.exar.com/XRP6141) for most up-to-date Ordering Information
2. Visit [www.exar.com](http://www.exar.com) for additional information on Environmental Rating.
TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at $V_{IN} = 12\, \text{V}$, $V_{OUT}=1.2\, \text{V}$, $f=300\, \text{kHz}$, $T_{A} = 25^\circ\text{C}$, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

Fig. 4: Load regulation, $V_{IN} = 12\, \text{V}$

Fig. 5: Line regulation, $I_{OUT} = 25\, \text{A}$

Fig. 6: $V_{OUT}$ ripple is $22\, \text{mV}$ at $25\, \text{A}$, $12\, \text{VIN}$, $1.2\, \text{VOUT}$

Fig. 7: $V_{OUT}$ ripple is $22\, \text{mV}$ at $0\, \text{A}$, DCM, $12\, \text{VIN}$, $1.2\, \text{VOUT}$

Fig. 8: Powerup, Forced CCM, $I_{OUT} = 0\, \text{A}$

Fig. 9: Powerup, Forced CCM, $I_{OUT} = 25\, \text{A}$
Fig. 10: Powerup, DCM/CCM, $I_{OUT} = 0A$

Fig. 11: Powerup, DCM/CCM, $I_{OUT} = 25A$

Fig. 12: Efficiency, $5V_{IN}, 1.8V_{OUT}, 0.47uH, 300kHz$

Fig. 13: Efficiency, $5V_{IN}, 1.2V_{OUT}, 0.47uH, 300kHz$

Fig. 14: Efficiency, $5V_{IN}, 1.0V_{OUT}, 0.47uH, 300kHz$

Fig. 15: Efficiency, $12V_{IN}, 3.3V_{OUT}, 1uH, 300kHz$
Fig. 16: Efficiency, 12V\textsubscript{IN}, 2.5V\textsubscript{OUT}, 1\mu H, 300kHz

Fig. 17: Efficiency, 12V\textsubscript{IN}, 1.8V\textsubscript{OUT}, 1\mu H, 300kHz

Fig. 18: Efficiency, 12V\textsubscript{IN}, 1.2V\textsubscript{OUT}, 0.47\mu H, 300kHz

Fig. 19: Efficiency, 12V\textsubscript{IN}, 1.0V\textsubscript{OUT}, 0.47\mu H, 300kHz

Fig. 20: Enable turn on/turn off, 12V\textsubscript{IN}, 1.2V\textsubscript{OUT}, 25A
Fig. 22: frequency versus $I_{out}$, Forced CCM

Fig. 23: VREF versus temperature

Fig. 24: On-Time versus temperature

Fig. 25: ILIM versus temperature

Fig. 26: Load step, DCM/CCM, 0A-25A-0A

Fig. 27: Load step, Forced CCM, 0A-25A-0A
**Detailed Operation**

XRP6141 is a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) controller. The on-time, which is programmed via RON, is inversely proportional to VIN and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with GH signal turning the high-side (switching) FET for a preprogrammed time. At the end of the on-time the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the minimum off-time the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

**Enable/Mode Input (EN/MODE)**

EN/MODE pin accepts a tri-level signal that is used to control turn on/off. It also selects between two modes of operation: 'Forced CCM' and 'DCM/CCM'. If EN is pulled below 1.9V, the controller shuts down. A voltage between 1.9V and 3.0V selects the Forced CCM mode which will run the converter in continuous conduction at all times. A voltage higher than 3.0V selects the DCM/CCM mode which will run the converter in discontinuous conduction at light loads.

**Selecting the Forced CCM Mode**

In order to set the controller to operate in Forced CCM, a voltage between 1.9V and 3.0V must be applied to the EN/MODE pin. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from VIN. If VIN is well regulated, use a resistor divider and set the voltage to 2.5V. If VIN varies over a wide range, the circuit shown in figure 28 can be used to generate the required voltage. Note that at VIN of 5.5V to 22V the nominal Zener voltage is 4.0V to 5.0V respectively. Therefore, for VIN in the range of 5.5V to 22V, the circuit shown in figure 28 will generate voltage at the EN/MODE pin required for Forced CCM.

**Selecting the DCM/CCM Mode**

In order to set the controller operation to DCM/CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to the EN/MODE pin. In applications where an external control signal is not available, EN/MODE input can be derived from VIN. If VIN is well regulated, use a resistor divider and set the voltage to 4V. If VIN varies over a wide range, the circuit shown in figure 29 can be used to generate the required voltage.

**Programing the On-Time**

The on-time TON is programmed via resistor RON according to following equation:

\[
TON = \frac{(3.4E - 10) \times RON}{V_{IN}}
\]

The required TON for a given application is calculated from:

\[
TON = \frac{V_{OUT}}{V_{IN} \times f}
\]
Note that switching frequency \( f \) will increase somewhat, as a function of increasing load current and increasing losses (see figure 22).

**OVER-CURRENT PROTECTION (OCP)**

If load current exceeds the programmed over-current \( I_{\text{OCP}} \) for four consecutive switching cycles, then IC enters hiccup mode of operation. In hiccup the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The IC will remain in hiccup mode until load current is reduced below the programmed \( I_{\text{OCP}} \). In order to program over-current protection use the following equation:

\[
RLIM = \frac{(I_{\text{OCP}} \times RDS) + 8\text{mV}}{I_{\text{ILIM}}}
\]

Where:
- \( RLIM \) is resistor value for programming \( I_{\text{OCP}} \)
- \( I_{\text{OCP}} \) is the over-current value to be programmed
- \( RDS \) is the MOSFET rated on resistance
- \( 8\text{mV} \) is the OCP comparator offset
- \( I_{\text{ILIM}} \) is the internal current that generates the necessary OCP comparator threshold (use 45\text{uA})

Note that \( I_{\text{ILIM}} \) has a positive temperature coefficient of 0.4%/°C. This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. In order for this feature to be effective the temperature rise of the IC should approximately match the temperature rise of the FET.

**SHORT-CIRCUIT PROTECTION (SCP)**

If the output voltage drops below 60% of its programmed value, the IC will enter hiccup mode. Hiccup will persist until short-circuit is removed. SCP circuit becomes active after PGOOD asserts high.

**OVER-TEMPERATURE PROTECTION (OTP)**

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

**PROGRAMMING THE OUTPUT VOLTAGE**

Use an external voltage divider as shown in figure 1 to program the output voltage \( V_{\text{OUT}} \).

\[
R1 = R2 \times \left( \frac{V_{\text{OUT}}}{0.6} - 1 \right)
\]

R2 recommended range is 2kΩ to 10kΩ.

**PROGRAMMING THE SOFT-START**

Place a capacitor \( CSS \) between the SS and GND pins to program the soft-start. In order to program a soft-start time of \( T_{\text{SS}} \), calculate the required capacitance \( CSS \) from the following equation:

\[
CSS = T_{\text{SS}} \times \frac{10\text{uA}}{0.6V}
\]

**FEED-FORWARD CAPACITOR (\( C_{\text{FF}} \))**

A feed-forward capacitor \( (C_{\text{FF}}) \) may be necessary depending on the Equivalent Series Resistance (ESR) of \( C_{\text{OUT}} \). If only ceramic output capacitors are used then a \( C_{\text{FF}} \) is necessary. Calculate \( C_{\text{FF}} \) from:

\[
C_{\text{FF}} = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}
\]

where:
- \( R1 \) is the resistor that \( C_{\text{FF}} \) is placed in parallel with
- \( f_{LC} \) is the frequency of the output filter double pole
- \( C_{\text{FF}} \) must be less than 15kHz when using ceramic \( C_{\text{OUT}} \). If necessary, increase \( C_{\text{OUT}} \) and/or \( L \) in order to meet this constraint.

When using capacitors with higher ESR such as Panasonic TPE series, \( C_{\text{FF}} \) is not required provided following conditions are met:

1. The frequency of the output LC double pole \( f_{LC} \) should be less than 10kHz.
2. The frequency of ESR zero \( f_{\text{ZERO,ESR}} \) should be at least five times larger than \( f_{LC} \).

Note that if \( f_{\text{ZERO,ESR}} \) is less than 5 \( f_{LC} \), then it is recommended to set the \( f_{LC} \) at less than 2kHz. \( C_{\text{FF}} \) is still not required.

**FEED-FORWARD RESISTOR (\( R_{\text{FF}} \))**

Poor PCB layout and/or extremely fast switching FETs can cause switching noise at the output and may couple to the FB pin via \( C_{\text{FF}} \). Excessive noise at FB will cause poor load regulation. To solve this problem place a resistor \( R_{\text{FF}} \) in series with \( C_{\text{FF}} \). \( R_{\text{FF}} \) value up to 2% of \( R1 \) is acceptable.

**MAXIMUM ALLOWABLE VOLTAGE RIPPLE AT FB PIN**

Note that the steady-state voltage ripple at feedback pin \( (V_{\text{FB,ripp}}) \) must not exceed 50mV in order for the controller to function correctly. If \( V_{\text{FB,ripp}} \) is larger than 50mV then \( C_{\text{OUT}} \) should be increased as necessary in order to keep the \( V_{\text{FB,ripp}} \) below 50mV.
MECHANICAL DIMENSIONS

16 PIN 3X3 QFN

DIMENSION TABLE

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.80</td>
<td>0.90</td>
<td>1.00</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.02</td>
<td>0.05</td>
</tr>
<tr>
<td>A3</td>
<td></td>
<td>0.20</td>
<td>0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>0.25</td>
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TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MD-220.
RECOMMENDED LAND PATTERN AND STENCIL

TYPICAL RECOMMENDED LAND PATTERN

TYPICAL RECOMMENDED STENCIL

Drawing No.: PQD- 0000138
Revision: A
REVISION HISTORY

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<tr>
<th>Revision</th>
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<tr>
<td>1.0.0</td>
<td>12/16/2013</td>
<td>Initial release</td>
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<td>1.0.1</td>
<td>12/20/2013</td>
<td>Specification improvement</td>
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<td>2.0.0</td>
<td>7/31/2005</td>
<td>Modified Functional Block Diagram, Application Circuit, Feed-Forward Capacitor; added “Selecting the Forced CCM Mode”, “Selecting the DCM/CCM Mode”, “Feed-Forward Resistor”, “Maximum Allowable Voltage Ripple at FB Pin” sections.</td>
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<td>2.0.1</td>
<td>11/23/2015</td>
<td>Change VCC Linear Regulator Dropout Voltage from 200mV min and 300mV typ to 200mV typ</td>
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<tr>
<td>2.0.2</td>
<td>5/24/2018</td>
<td>Update to MaxLinear logo. Update format and Ordering Information table. Added Revision History.</td>
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