GENERAL DESCRIPTION

This reference design is a complete five-output power system designed to power a Xilinx Zynq-7020 All Programmable (AP) SoC and associated DDR3 memory in Industrial Ethernet applications. This reference design is focused on Industrial Ethernet applications leveraging HMS’s Anybus IP on Xilinx. Although the power requirements of the core system building blocks remain relatively constant, the flexibility of Exar’s Universal PMICs provides a power solution that can power the wider system requirements, whether a motor control board or human interface module.

The power system provides VCCPINT, VCCINT and VCCBRAM 1.0V, VCCO_DDR programmable to 1.2/1.35/1.5V, VTT 0.60/0.675/0.75V, VCCO programmable from 1.8V to 3.3V, VCCAUX and VCCADC 1.8V. The entire power system fits in less than one square inch. The order and ramp rates for each supply are programmed to accommodate Zynq-7020 sequencing requirements. All power supply operations can be controlled over an I2C interface. Faults, output voltages and currents can also be monitored. 4 GPIO signals are available and can be programmed to provide the status of power good signals, enables, and faults. The board is supported by PowerArchitect™ 4.x and connects to the Exar Communications Module (XR77XXEVB-XCM-V80).

FEATURES

- **Xilinx Zynq-7020 All Programmable SoC Power System**
  - 4 Channel Power System using XRP7714 Programmable Digital PWM Switching Controller
  - VCCPINT, VCCINT and VCCBRAM 1.0V
  - VCCO_DDR programmable to 1.2/1.35/1.5V
  - VTT 0.60/0.675/0.75V
  - VCCO programmable to from 1.8V to 3.3V
  - VCCAUX and VCCADC 1.8V

- **I2C Interface**
  - Programming
  - Monitoring
  - Control
ZYNQ-7020 AP SOC Power Solution

The Zynq-7020 AP SoC power reference design provides 4 output voltages. The order and ramp rates for each output are programmed to accommodate Zynq-7020 AP SoC sequencing requirements.

The power system was designed to operate at 650kHz as a good trade-off between space and efficiency.

Output 1/Channel 1 Configuration

Channel 1 is designed to provide 1V to VCCINT, VCCBRAM and VCCPINT Zynq-7020 AP SoC rails at 2.0A. However, the hardware is capable of supporting output currents up to 3Amps.

Output 2/Channel 2 Configuration

Channel 2 provides 1.5V to the DDR3 SDRAM subsystem as well as the DDR3 block inside the Zynq-7020 AP SoC. In addition, it sources the XRP2997 DDR Bus Termination Regulator which provides termination voltage for the DDR3 SDRAM signals. The channel is configured for a 2.0A output, but the hardware is capable of supporting up to a 3Amp load.

Output 3/Channel 3 Configuration

Channel 3 provides 2.5V to Zynq-7020 AP SoC IO banks (VCCO) and peripherals in the system. The channel is configured for a 1.5A output, but the hardware is capable of supporting up to a 2Amp load.

Output 4/Channel 4 Configuration

Channel 4 is designed to provide 1.8V to VCCAUX and VCCADC Zynq-7020 AP SoC rails at 0.5A. The channel is configured for a 0.5A output, but the hardware is capable of supporting up to a 1.5Amp load.
LDOOUT

LDOOUT is routed to XRP2997 control pin enabling the device.

CHANNEL SEQUENCING

The XRP7714 sequencing has been designed to meet the Zynq-7020 AP SoC power up sequencing requirements.

Power-On Sequencing

1. **1.0V** supply with 0.077V/msec ramp rate
2. **1.8V** supply with 0.12V/msec ramp rate
3. **1.5V and 2.5V supplies** - the 1.5V supply with 0.115V/msec ramp rate reaching the target level at the same time as the 2.5V supply with 0.192V/msec ramp rate.

Power-Down Sequencing

1. **1.5V and 2.5V supplies** – the 1.5V supply following 0.1875V/msec ramp down rate; the 2.5V supply following 0.3125V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.
2. **1.0V and 1.8V supplies** – the 1.0V supply following 0.125V/msec ramp down rate; the 1.8V supply following 0.225V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.
ZYNQ-7020 AP SoC POWER ON RESET

XRP7714 will generate a power on reset signal on GPIO3 to the Zynq-7020 AP SoC 400ms after the last rail is in regulation.

POWERING UP THE BOARD

The board hardware is provided capable of supporting an input voltage range of 5.5V to 15V with power connected directly to J5 (VIN) and J6 (GND).

I2C Interface

The Zynq-7020 AP SoC power reference design schematic shows an I2C interface connector (HDR2) to connect the Exar Communications Module (XR77XXEVB-XCM-V80 which has its own users guide available). This provides an interface with PowerArchitect™ 4.x allowing programming of the board.

Ensure the XCM is configured to use the on board pull-up resistors (check jumper settings).

If communication between Zynq-7020 AP SoC and XRP7714 is desired, ensure that the Zynq-7020 AP SoC system board has pull-up resistors installed.

For more information how to implement power subsystem control and monitoring via I2C bus refer to ANP-31.

Configuring the Board

The board is typically delivered with a XRP7714 which has not yet had its OTP memory burned with a specific configuration. This allows the user to select a different VIO voltage or DDR memory voltage than the one used in the default configuration file available from Exar’s web site.

https://www.exar.com/products/zynq-7020
TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at \( V_{IN} = 12V, f_{SW} = 650kHz, T_J = T_A = 25^\circ C \), unless otherwise specified

- Fig. 1: Channel 1, 1.0V Efficiency
- Fig. 2: Channel 2, 1.5V Efficiency
- Fig. 3: Channel 3, 2.5V Efficiency
- Fig. 4: Channel 4, 1.8V Efficiency
- Fig. 5: Channel 1, 1.0V Load Regulation
- Fig. 6: Channel 2, 1.5V Load Regulation
Fig. 13: Channel 1, 1.0V Full Load Output Ripple

Fig. 14: Channel 2, 1.5V Full Load Output Ripple

Fig. 15: Channel 3, 2.5V Full Load Output Ripple

Fig. 16: Channel 4, 1.8V Full Load Output Ripple

Fig. 17: Input Cap Ripple
Notes:
1) Meets all Zynq seq and dependency constraints
2) All higher value ceramics can be built out of multiples of 22uF to decrease cost.
3) All system requirements (eg Seq, O/C, O/V, O/T, enables, power good, etc) are configurable
4) Realtime readout of Vin, Vout, Iout, etc available via I2C
5) Output current can be programmed up to approx 3.5A/ch
6) Vout options programmable
7) PS_POR_B is correctly timed.
## BILL OF MATERIAL

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Qty</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Size</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td>1</td>
<td>Exar</td>
<td>146-6730-01</td>
<td>XRP7714EVB_IND_V09_VER2</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>Exar</td>
<td>XR7714ILB-F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U2</td>
<td>1</td>
<td>Exar</td>
<td>XRP29971DBTR-F</td>
<td>SOICD B08</td>
<td>2A, DDR I/II/II Bus Term. Regulator</td>
</tr>
<tr>
<td>Q1,Q2,Q4</td>
<td>3</td>
<td>Diodes, Inc.</td>
<td>DMN2050LFDB</td>
<td>U-DFN2020-6</td>
<td>Dual N-Ch. MOSFET, 20V,4.5A, 45mOhm</td>
</tr>
<tr>
<td>Q3</td>
<td>1</td>
<td>Diodes, Inc.</td>
<td>DMN2300UFL4</td>
<td>X2-DFN1310-6</td>
<td>Dual N-Ch. MOSFET, 20V,2.11A, 195mOhm</td>
</tr>
<tr>
<td>D1,D2,D3,D4</td>
<td>4</td>
<td>Diodes, Inc.</td>
<td>SD101AWS</td>
<td>SOD-323</td>
<td>SMT Barrier Diode, 60V, 15mA</td>
</tr>
<tr>
<td>L1,L2</td>
<td>2</td>
<td>Wurth Elektronik</td>
<td>7440620015</td>
<td>6.8X6.8MM</td>
<td>SMD Inductor 1.5uH, 4.3A, 14.0 mOhm</td>
</tr>
<tr>
<td>L3,L4</td>
<td>2</td>
<td>Wurth Elektronik</td>
<td>74408943047</td>
<td>4.8X4.8MM</td>
<td>SMD Inductor 4.7uH, 2.2A, 45.0 mOhm</td>
</tr>
<tr>
<td>C2,C9,C22</td>
<td>3</td>
<td>MURATA</td>
<td>GRM31CR60J107ME39L</td>
<td>1206</td>
<td>CERAMIC CAP. 100uF, 6.3V, X5R, 20%</td>
</tr>
<tr>
<td>C10, C12, C15, C19</td>
<td>4</td>
<td>MURATA</td>
<td>GRM31CR61A476KE15L</td>
<td>1206</td>
<td>CERAMIC CER. 47uF, 10V, X5R, 10%</td>
</tr>
<tr>
<td>C1,C7,C18,C21</td>
<td>4</td>
<td>MURATA</td>
<td>GRM31CR71H475KA12L</td>
<td>1206</td>
<td>CERAMIC CAP., 4.7uF, 50V, X7R, 10%</td>
</tr>
<tr>
<td>C4,C5,C8,C17</td>
<td>4</td>
<td>MURATA</td>
<td>GRM21BR71E475KA73L</td>
<td>0805</td>
<td>CERAMIC CAP., 4.7uF, 25V, X7R, 10%</td>
</tr>
<tr>
<td>C3,C13,C14</td>
<td>3</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
<td>0805</td>
<td>CERAMIC CAP., 2.2uF, 16V, X7R, 10%</td>
</tr>
<tr>
<td>C6,C11,C16,C20</td>
<td>4</td>
<td>MURATA</td>
<td>GRM155R71E104KE14D</td>
<td>0402</td>
<td>CERAMIC CAP., 0.1uF, 25V, X7R, 10%</td>
</tr>
<tr>
<td>R1,R2</td>
<td>2</td>
<td>PANASONIC</td>
<td>ERA-3AEB104V</td>
<td>0603</td>
<td>Resistor 100.0K Ohm, 0.1% 1/10W, SMD</td>
</tr>
<tr>
<td>R3</td>
<td>1</td>
<td>PANASONIC</td>
<td>ERJ-3EKF6802V</td>
<td>0603</td>
<td>Resistor 68.0K Ohm, 1/10W,1%,SMD</td>
</tr>
<tr>
<td>R4</td>
<td>1</td>
<td>PANASONIC</td>
<td>ERJ-3RQF1R0V</td>
<td>0603</td>
<td>Resistor 1.0 Ohm, 1/10W,1%,SMD</td>
</tr>
<tr>
<td>J7,J9,J10,J13,J16,J15</td>
<td>12</td>
<td>Vector Electronics</td>
<td>Vector Electronics</td>
<td>.042” Hole</td>
<td>PCB Pin</td>
</tr>
<tr>
<td>TP1,TP0,TP3,TP4,TP2</td>
<td>5</td>
<td>Wurth Electronics</td>
<td>61300111121</td>
<td>Test Point</td>
<td>Test Point</td>
</tr>
<tr>
<td>1-SCL,GND,SDA</td>
<td>1</td>
<td>Wurth Electronics</td>
<td>61300311121</td>
<td>Test Point</td>
<td>3 PIN HEADER</td>
</tr>
</tbody>
</table>
EVALUATION BOARD LAYOUT (FOR REFERENCE)

Figure 3: Component Placement Top Side

Figure 4: Top Layer
Figure 7: Mid-Layer 2

Figure 8: Mid-Layer 3
Figure 9: Bottom Layer